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4H-SiC MIS Capacitors and MISFETs With Deposited SiNₓ/SiO₂ Stack-Gate Structures

Masato Noborio, Student Member, IEEE, Jun Suda, and Tsunenobu Kimoto, Senior Member, IEEE

Abstract—SiNₓ/SiO₂ stack-gate structures, followed by N₂O annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality.

Index Terms—Channel mobility, deposited insulator, interface trap density, metal–insulator–semiconductor (MIS), MOSFET, silicon carbide (SiC), silicon nitride (SiNₓ), silicon oxynitride (SiOₓ·Nᵧ).

I. INTRODUCTION

Silicon carbide (SiC) is an attractive wide-band-gap semiconductor that has superior properties, such as high breakdown field, high thermal conductivity, and high saturation electron drift velocity [1]. Among many SiC polytypes, 4H-SiC is the polytype suitable for high-power devices in the next generation due to its high bulk mobility and its small anisotropy. Recent progress in SiC growth and device technology has led to the commercial release of high-voltage 4H-SiC Schottky rectifiers [2], [3], and SiC MOSFETs have been regarded as a promising candidate for low-loss and fast power devices in advanced electronic systems [4]. Although 4H-SiC MOSFETs have great potential for high-power switches, the fabricated MOSFETs with thermal oxide grown in dry O₂ ambient exhibit a low channel mobility below 10 cm²/V·s because of its high SiO₂/SiC interface trap density. In order to overcome this problem, various methods have been investigated. For example, wet reoxidation or “nitridation” of the SiC MOS interface [5]–[8] and the usage of 4H-SiC (0001) or (1120) face [9], [10] are effective processes to increase the channel mobility of SiC MOSFETs. These investigations on SiC MOS technology have mainly focused on thermal oxide. However, the interfacial transition layer, which contains carbon atoms or carbon cluster in the SiO₂, is detected between pure SiO₂ grown by thermal oxidation and SiC [11], [12]. Although the origin of interface traps has not fully been understood, the thickness of interfacial transition layer is correlated with the channel mobility. (The thick transition layer at the SiO₂/SiC interface may reduce the channel mobility [12].) On the other hand, the transition layer at the interface will hardly be formed when the gate insulator is deposited. Therefore, the deposited insulator/SiC interface may be abrupt and can be expected to show better characteristics than the thermal oxide/SiC interface. The deposited insulators also have other advantages: 1) superior reliability (when adequately processed) [13]; 2) reduction of process time; and 3) isotropic formation of oxide on the trench sidewalls. From these advantages, deposited insulators are one of the attractive candidates for the gate insulators of SiC metal–insulator–semiconductor (MIS) devices.

A few groups have started to investigate SiC MOS structures with deposited insulator [14]–[16]. SiC MOSFETs with deposited SiO₂ followed by N₂O annealing [17] and low-temperature deposited Al₂O₃ [18] have already demonstrated a higher channel mobility than the MOSFETs with thermal oxide. In this paper, the authors adopt SiNₓ/ SiO₂ stack-gate structures deposited by plasma-enhanced chemical vapor deposition (PECVD), followed by N₂O annealing. In the proposed structure, by inserting other dielectrics between SiC and SiO₂, an adverse impact of near-interface traps located at E_C = 2.77 eV in SiO₂ [19] may be minimized. In addition, the deposited insulator may suppress the formation of the interfacial transition layer, as previously mentioned. The authors have succeeded in reducing the density of interface traps and enhancing the channel mobility, compared to N₂O oxidation, in SiC MISFETs fabricated with a deposited SiNₓ/ SiO₂ stack-gate structure annealed in N₂O.

II. DEVICE FABRICATION

For the fabrication of MIS capacitors, n-type 4H-SiC (0001) epilayers with a donor concentration of 1 × 10¹⁶ cm⁻³, purchased from Cree, were prepared. The gate formation procedure used in this study is shown in Fig. 1. Fig. 1(a) and (b) shows the process to form SiNₓ/ SiO₂ stack-gate structures. After RCA cleaning with final hydrofluoric acid dip, the SiNₓ layer was deposited by PECVD with SiH₄ and NH₃ as source gases. The thickness of deposited SiNₓ was varied from...
Fig. 1. Experimental procedure for stack-gate MIS structures annealed in (a) \( N_2 \) and (b) \( N_2O \) and MOS structures with (c) deposited oxide and (d) thermal oxide. MOS structures with oxide (without SiN\(_x\)) layer were fabricated as a reference.

2 to 10 nm. Then, subsequent SiO\(_2\) deposition was carried out. In the SiO\(_2\) deposition, SiH\(_4\) and N\(_2\)O were used as source gases. The deposited thickness of SiO\(_2\) was about 50 nm. The typical deposition temperature of SiN\(_x\) and SiO\(_2\) was 400 °C. After the PECVD process, thermal annealing was performed in dry N\(_2\)O (10% diluted in N\(_2\)) and N\(_2\) ambient at 1300 °C. N\(_2\)O-annealing time was varied, ranging from 30 min to 2 h [Fig. 1(b)]. During N\(_2\)O annealing, a portion of the SiN\(_x\) layer was oxidized and converted to the SiO\(_2\)N\(_y\) layer. Some of the samples were not annealed in N\(_2\)O [Fig. 1(a)]. MOS structures deposited by PECVD, with SiH\(_4\) and N\(_2\)O as source gases [Fig. 1(c)], and formed by direct oxidation of SiC in dry N\(_2\)O (10% diluted in N\(_2\)) ambient at 1300 °C [Fig. 1(d)] [12] were also prepared as a reference. The reference samples have a SiO\(_2\)/SiC interface (without the SiN\(_x\) layer). The equivalent oxide thickness (EOT) calculated from the accumulation capacitance was about 60 nm. Al was evaporated on the backside and annealed at 600 °C for 10 min. The circular gate metal was Al, with a diameter of 520 µm for capacitance–voltage (C–V) measurements and 180 µm for current–voltage (I–V) measurements.

The authors have also fabricated n-channel MISFETs on p-type 4H-SiC (0001) epilayers with an acceptor concentration of \( 8 \times 10^{15} \) cm\(^{-3} \) and on p-type 4H-SiC (0001) epilayers with an acceptor concentration of \( 6 \times 10^{15} \) cm\(^{-3} \), purchased from Cree. The source–drain regions were formed by high-dose \( (5 \times 10^{15} \) cm\(^{-2} \) \( P^+ \) implantation at 300 °C. After ion implantation, high-temperature annealing was performed at 1600 °C for 15 min in Ar with a carbon cap to suppress surface roughening [21]. The formation of gate insulators was the same process as that previously mentioned. Ti/Al and Al annealed at 600 °C for 10 min were used as the backside and source–drain contacts, respectively. The gate metal was Al. The typical channel length \( L \) and width \( W \) were in the range of 25–100 µm and 200 µm, respectively. In order to estimate exact channel mobility and suppress short-channel effects [20], the authors adopted the design of long-channel lateral MOSFETs.

III. EXPERIMENTAL RESULT AND DISCUSSION

Quasi-static and high-frequency (1 MHz) C–V characteristics \( (C_{QS} \) and \( C_{HF} \), respectively) were measured by using a simultaneous C–V system at room temperature under dark conditions. From the C–V curves, interface trap density was calculated by a high–low method.

The density of interface traps determined by a high–low method for stack-gate MIS capacitors with a deposited SiN\(_x\)/SiO\(_2\) thickness of 10 nm/55 nm is represented in Fig. 2. The stack-gate MIS capacitors were annealed in N\(_2\) or N\(_2\)O ambient for 30 min. Fig. 2 also shows the interface trap density for a MOS capacitor with thermal oxide grown in the N\(_2\) ambient (“Ther. Ox.”). The density of interface traps for the stack-gate MIS capacitor annealed in N\(_2\)O (“SiN\(_x\)/SiO\(_2\) + N\(_2\)O (30 min)”) is lower than that for the stack-gate MIS capacitor annealed in N\(_2\) (“SiN\(_x\)/SiO\(_2\) + N\(_2\)”). N\(_2\)O annealing is more effective in reducing the interface trap than N\(_2\) annealing for the SiN\(_x\)/SiO\(_2\) stack-gate structure. Compared with thermal oxide, the stack-gate structure, followed by N\(_2\)O annealing, exhibits low interface trap density near the conduction band edge. The high density of the interface trap in the shallow energy region causes electron trapping, leading to low channel mobility in 4H-SiC MOSFETs [22].

Fig. 3 shows the results of the secondary ion mass spectrometry measurement for the stack-gate MIS capacitor, followed by N\(_2\)O annealing for 30 min (the same device as “SiN\(_x\)/SiO\(_2\) + N\(_2\)O (30 min)” shown in Fig. 2). The depth profiles of Si, C, N, and O atoms were measured. The depth resolution was about 3 nm. From Fig. 3, the oxygen atoms are clearly detected even between SiO\(_2\) and SiC, indicating that the initial-SiN\(_x\) layer was oxidized during N\(_2\)O annealing. Nitrogen atoms are accumulated at the SiC/SiN\(_x\) interface, and the concentration of nitrogen atoms at the interface is about \( 1 \times 10^{22} \) cm\(^{-3} \).

The C–V characteristics of stack-gate MIS capacitors annealed in N\(_2\)O ambient for (a) 30 min and (b) 2 h with a deposited SiN\(_x\)/SiO\(_2\) thickness of 10 nm/50 nm are represented in Fig. 4. The accumulation capacitance was reduced by increasing the N\(_2\)O-annealing time, which means that the SiN\(_x\) layer is oxidized during N\(_2\)O annealing and becomes an SiO\(_2\)N\(_y\) layer, as shown in Fig. 3. The MIS capacitor annealed...
The effective fixed charge density at the MIS interface of the large negative flat-band voltage shift (about \( C \)) annealed for 2 h, the high-frequency curve for 30 min shows a small difference between quasi-static and HF curves. On the other hand, in the MIS capacitor annealed for 2 h, the high-frequency \( C-V \) curve is exactly similar to the quasi-static \( C-V \) curve [Fig. 4(b)], although a large negative flat-band voltage shift (about \(-15 \text{ V}\)) is observed. The effective fixed charge density at the MIS interface of the stack-gate MIS capacitor annealed in \( \text{N}_2\text{O} \) for 30 min and 2 h is about \( 2 \times 10^{11} \text{ cm}^{-2} \) (positive) and \( 6 \times 10^{12} \text{ cm}^{-2} \) (positive), respectively. The stack-gate MIS capacitor, followed by \( \text{N}_2\text{O} \) annealing for 2 h, exhibits significant increase of effective fixed charge. Fig. 5 represents the interface trap density of stack-gate MIS capacitors annealed in \( \text{N}_2\text{O} \) for 30 min, 1 h, and 2 h (open circles, open squares, and closed circles, respectively, in Fig. 5), demonstrating that the interface trap density could significantly be reduced by extending the \( \text{N}_2\text{O} \)-annealing time.

The stack-gate MIS capacitors, followed by \( \text{N}_2\text{O} \) annealing for 30 min and 1 h, show a slight decrease of interface trap density at the shallow energy region from the conduction band edge. The interface trap density of the stack-gate MIS capacitor annealed for 2 h is lower than that of thermal oxide at any energy levels investigated in this study, which are as low as \( 1 \times 10^{11} \text{ cm}^{-2} \text{eV}^{-1} \) or below.

The \( I-V \) measurement was also performed. Fig. 6 shows the typical current density-electric field characteristics for the fabricated stack-gate MIS capacitors and MOS capacitors. The stack-gate MIS capacitors showed in Fig. 6 have a deposited \( \text{SiN}_x/\text{SiO}_2 \) thickness of 10 nm/50 nm. The oxide field was corrected by taking account of the flat-band-shift voltage. The typical ramp rate for \( I-V \) measurements was about 0.05 V/s. The gate current was drastically increased, leading to oxide breakdown, after the last point plotted in Fig. 6. The stack-gate MIS capacitor, followed by \( \text{N}_2 \) annealing (“\( \text{SiN}_x/\text{SiO}_2 + \text{N}_2 \)”), and the MOS capacitor with deposited oxide (“Depo. Ox.”) show a low breakdown field of about 7 MV/cm. On the other hand, the thermal oxide (“Ther. Ox.”) and stack-gate structure, followed by \( \text{N}_2\text{O} \) annealing (“\( \text{SiN}_x/\text{SiO}_2 + \text{N}_2\text{O} \)”), exhibit higher breakdown field than other samples. The stack-gate MIS capacitor annealed in \( \text{N}_2\text{O} \) for 2 h demonstrates low leakage current and high breakdown field. It has been reported that deposited insulators, such as ONO stack films formed by chemical vapor deposition (CVD) [13] and CVD oxide [23] on 4H-SiC, exhibit high dielectric reliability compared with thermal oxide. The MIS structure formed by \( \text{SiN}_x/\text{SiO}_2 \) deposition, followed by \( \text{N}_2\text{O} \) annealing, has high dielectric strength compared with thermal oxide.
These MISFETs have a deposited SiN/MIS structure, with the SiO2 layer directly deposited on SiC by PECVD, followed by NO annealing, may be one of the attractive approaches to improve the interface and dielectric characteristics.

Fig. 7 exhibits the field-effect mobility of MISFETs with N2O-annealed SiNx/SiO2 stack-gate structure on the (0001)Si face. Open circles, open squares, and closed circles correspond to the MISFETs annealed for 30 min, 1 h, and 2 h, respectively. The horizontal axis of Fig. 7 is the gate oxide field, which is defined as Vg/EOT. The field-effect mobility increases with extending N2O-annealing time. The increase of field-effect mobility can be correlated with the reduction of interface trap density, as shown in Fig. 5. As predicted from its low interface trap density, a high channel mobility over 30 cm2/V·s is obtained when the N2O-annealing time was 2 h. However, the MISFET annealed for 2 h shows a considerably shifted threshold voltage of −15 V, which agrees with the large negative shift of the flat-band voltage obtained in the MIS capacitor shown in Fig. 4(b).

In the stack-gate MIS structures, the SiNx layer is oxidized during N2O annealing, and a portion of the SiNx layer is converted to the SiO2Ny layer, as shown in Fig. 3. Then, the MIS structure is changed from a SiC/SiNx/SiO2 stack-gate structure to a SiC/thin-SiNx/SiO2Ny/SiO2 one. The influence of traps inside the SiNx layer may be decreased by thinning the residual SiNx layer. Thus, the lower interface trap density may be obtained by extending the N2O-annealing time. In the MIS structure annealed in N2O for 2 h, the SiNx layer may be completely oxidized and converted to the SiO2Ny layer, and the stack-gate structure becomes the SiC/SiO2Ny/SiO2 structure, in which traps inside the SiNx layer may be decreased by thinning the residual SiNx layer. The influence of traps inside the SiNx layer may be decreased by thinning the residual SiNx layer. Thus, the lower interface trap density may be obtained by extending the N2O-annealing time. In the MIS structure annealed in N2O for 2 h, the SiNx layer may be completely oxidized and converted to the SiO2Ny layer, and the stack-gate structure becomes the SiC/SiO2Ny/SiO2 structure, in which traps inside the SiNx layer may be decreased by thinning the residual SiNx layer. Thus, the lower interface trap density may be obtained by extending the N2O-annealing time.

In order to reduce the large negative shift (positive charge), the initial thickness of the deposited SiNx layer was decreased to 2 nm. The authors fabricated the stack-gate MIS capacitors and MISFETs, followed by N2O annealing for 5 min. In order to completely oxidize the SiNx layer, the short N2O-annealing time was selected because of the very thin SiNx layer. The optimum N2O-annealing time depends on the initial-SiNx layer thickness (a thinner initial-SiNx layer needs a shorter N2O-annealing time). The C–V curves for the MIS capacitor with a SiNx/SiO2 thickness of 2 nm/58 nm. The closed circles denote the stack-gate MIS capacitor. The dashed line denotes the MOS capacitor with thermal oxide, and the solid line denotes that with deposited oxide.
MIS capacitor with the thin SiN_x layer. Although the interface trap density for the MIS capacitor with a SiN_x thickness of 2 nm is higher than $1 \times 10^{11} \text{ cm}^{-2} \text{eV}^{-1}$, as shown by the closed circles in Fig. 5, it is still significantly lower than that for the MOS capacitor, with the thermal oxide grown in N_2O. Compared with the deposited oxide, followed by N_2O annealing, the stack-gate structure with the thin SiN_x layer shows a slightly low density of the interface trap in the deep energy region.

Fig. 10 shows the N_2O-annealing time dependence of effective channel mobility $\mu_{eff}$ at the gate oxide field of 3 MV/cm and effective fixed charge $Q_{eff}$ calculated from the difference between the theoretical and experimental threshold voltages. The MISFETs have a SiN_x/SiO_2 thickness of 2 nm/50 nm or 10 nm/50 nm. In the case of a SiN_x thickness of 10 nm, the effective mobility is increased by increasing the N_2O-annealing time, whereas the mobility decreases with increasing N_2O-annealing time in the MIS capacitor with a thin SiN_x thickness of 2 nm. In the MIS structures with the thin-SiN_x layer (2 nm), the time to completely oxidize the SiN_x layer is shorter than that for the MIS structures with a SiN_x thickness of 10 nm. Thus, the optimum N_2O-annealing time may be shorter.

Fig. 11 shows the subthreshold characteristics (log $I_D-V_G$/EOT characteristics) and the gate characteristics ($I_D-V_G$/EOT characteristics), and the field-effect mobility calculated from the gate characteristics is represented in Fig. 12, where the mobility of MOSFETs with thermal oxide and deposited oxide is also shown. The MISFET on the 4H-SiC (0001)Si face has a SiN_x/SiO_2 thickness of 2 nm/50 nm annealed for 5 min. The authors have also fabricated the MISFETs on the 4H-SiC (0001)C face with an acceptor concentration of $6 \times 10^{15} \text{ cm}^{-3}$. In the C-face MISFET, the gate insulator was a SiN_x/SiO_2 (2 nm/50 nm) stack structure annealed for 5 min, which is the same as that in the Si-face MISFET shown in Figs. 11 and 12. The threshold voltage obtained from the extrapolation of gate characteristics is 5.3 V for the MISFET on the Si face and 2.7 V for that on the C face, indicating the reduction of a large positive charge, as observed in Fig. 7. In Fig. 11, the MISFETs on the C face exhibits a steep slope in the subthreshold region of the log $I_D-V_G$/EOT plots, and the subthreshold slope of the MISFETs on the C face was 182 mV/dec. On the other hand, the drain-current of the MISFETs on the Si face gradually increases from a gate oxide field of ~0.5 MV/cm, and the subthreshold slope was 556 mV/dec. These results imply that the interface trap density of the C-face MISFETs is still lower than that of the Si-face MISFETs. While the MOSFETs with thermal oxide and deposited oxide show a channel mobility of 20 and 25 cm^2/V·s, respectively, a relatively high field-effect mobility of 32 cm^2/V·s is achieved in the stack-gate MISFETs on the (0001)Si face. This result indicates about 50% improvement in mobility. The channel mobility of MISFETs on the (0001)C face is 40 cm^2/V·s, suggesting a promise of the C face for MIS-based device application, as previously reported by using wet oxidation [9].
IV. Conclusion

In this study, SiN$_x$/SiO$_2$ stack-gate structures deposited by PECVD and annealed in N$_2$O were investigated for 4H-SiC MIS devices. The interface characteristics for the MIS capacitor with a SiN$_x$ thickness of 10 nm was significantly improved by extending the N$_2$O-annealing time to 2 h. During N$_2$O annealing, the deposited SiN$_x$ layer is oxidized, and the influence of traps inside the SiN$_x$ layer may be reduced. The MIS capacitor with a SiN$_x$/SiO$_2$ thickness of 10 nm/50 nm, followed by N$_2$O annealing for 2 h, exhibits a low interface trap density below $1 \times 10^{11}$ cm$^{-2}$eV$^{-1}$. However, this MIS capacitor showed a large negative shift of the flat-band voltage, which indicates that positive charge exists in the oxidized SiN$_x$ layer (SiO$_x$N$_y$ layer) or at the SiO$_2$/SiC interface. Compared with thermal oxide, the dielectric properties were also improved in the stack-gate structure annealed in N$_2$O. In order to suppress the large negative shift of the flat-band voltage, the initial thickness of the SiN$_x$ layer was decreased to 2 nm. The fabricated MISFETs with a SiN$_x$/SiO$_2$ layer of 2 nm/50 nm annealed in N$_2$O for 5 min demonstrated a high channel mobility of 32 cm$^2$/V·s on the (0001)Si face and 40 cm$^2$/V·s on the (0001)C face, as well as “normally off” operation. The optimum N$_2$O-annealing time for the MIS capacitor depends on the initial-SiN$_x$ thickness, because the time to completely oxidize the SiN$_x$ layer is different for these MIS capacitors. The deposited SiN$_x$/SiO$_2$ stack-gate structure annealed in N$_2$O ambient is one of the promising candidates for the gate insulator of 4H-SiC MIS devices.

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From 1992 to 1997, he worked on the growth of ZnSe-based semiconductors by molecular-beam epitaxy and the characterization of ZnMgSSe strained quantum well structures for optoelectronic applications. In 1997, he began research on group-III nitride semiconductors (III-N) and SiC as a Research Associate at Kyoto University. He is currently an Associate Professor with the Department of Electronics Science and Engineering, Kyoto University. He is the author or coauthor of more than 55 publications in peer-reviewed journals and international conference proceedings. His research interests include heteroepitaxial growth of III-N, functional integration of III-N and SiC materials by precise control of the heterointerface, design of wide-band-gap semiconductor devices, and characterization of device structure by scanning-probe microscopy.

Tsunenobu Kimoto (M’03–SM’06) received the B.E. and M.E. degrees in electrical engineering and the Ph.D. degree, based on his work on SiC epitaxial growth, characterization, and high-voltage diodes, from Kyoto University, Kyoto, Japan, in 1986, 1988, and 1996, respectively.

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