4H-SiC MIS Capacitors and MISFETs With Deposited SiN_x/SiO_2 Stack-Gate Structures

Masato Noborio, *Student Member, IEEE*, Jun Suda, and Tsunenobu Kimoto, *Senior Member, IEEE*

***Abstract*—SiN_x/SiO_2 stack-gate structures, followed by N_2O annealing, have been investigated to improve the 4H-SiC metal–insulator–semiconductor (MIS) interface quality. Capacitance–voltage measurements on fabricated stack-gate MIS capacitors have indicated that the interface trap density is reduced by post-deposition annealing in N_2O at 1300 °C. When the MIS capacitor with a SiN_x/SiO_2 thickness of 10 nm/50 nm was annealed in N_2O for 2 h, the interface trap density at $E_C - 0.2$ eV is below 1×10^{11} cm^{-2}eV^{-1}. Oxidation of SiN_x during N_2O annealing has resulted in the improvement of SiC MIS interface characteristics, as well as dielectric properties. The fabricated MISFETs with SiN_x/SiO_2 stack-gate structure annealed in N_2O demonstrate a reasonably high channel mobility of 32 cm^2/V · s on the (0001)Si face and 40 cm^2/V · s on the $(000\bar{1})$C face.**

***Index Terms*—Channel mobility, deposited insulator, interface trap density, metal–insulator–semiconductor (MIS), MOSFET, silicon carbide (SiC), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y).**

I. Introduction

SILICON carbide (SiC) is an attractive wide-band-gap semiconductor that has superior properties, such as high breakdown field, high thermal conductivity, and high saturation electron drift velocity [1]. Among many SiC polytypes, 4H-SiC is the polytype suitable for high-power devices in the next generation due to its high bulk mobility and its small anisotropy. Recent progress in SiC growth and device technology has led to the commercial release of high-voltage 4H-SiC Schottky rectifiers [2], [3], and SiC MOSFETs have been regarded as a promising candidate for low-loss and fast power devices in advanced electronic systems [4].

Although 4H-SiC MOSFETs have great potential for high-power switches, the fabricated MOSFETs with thermal oxide grown in dry O_2 ambient exhibit a low channel mobility below 10 cm^2/V · s because of its high SiO_2/SiC interface trap density. In order to overcome this problem, various methods have been investigated. For example, wet reoxidation or "nitridation" of the SiC MOS interface [5]–[8] and the usage of 4H-SiC $(000\bar{1})$ or $(11\bar{2}0)$ face [9], [10] are effective processes to increase the channel mobility of SiC MOSFETs. These investigations on SiC MOS technology have mainly focused on thermal oxide. However, the interfacial transition layer, which contains carbon atoms or carbon cluster in the SiO_2, is detected between pure SiO_2 grown by thermal oxidation and SiC [11], [12]. Although the origin of interface traps has not fully been understood, the thickness of interfacial transition layer is correlated with the channel mobility. (The thick transition layer at the SiO_2/SiC interface may reduce the channel mobility [12].) On the other hand, the transition layer at the interface will hardly be formed when the gate insulator is deposited. Therefore, the deposited insulator/SiC interface may be abrupt and can be expected to show better characteristics than the thermal oxide/SiC interface. The deposited insulators also have other advantages: 1) superior reliability (when adequately processed) [13]; 2) reduction of process time; and 3) isotropic formation of oxide on the trench sidewalls. From these advantages, deposited insulators are one of the attractive candidates for the gate insulators of SiC metal–insulator–semiconductor (MIS) devices.

A few groups have started to investigate SiC MOS structures with deposited insulator [14]–[16]. SiC MOSFETs with deposited SiO_2 followed by N_2O annealing [17] and low-temperature deposited Al_2O_3 [18] have already demonstrated a higher channel mobility than the MOSFETs with thermal oxide. In this paper, the authors adopt SiN_x/SiO_2 stack-gate structures deposited by plasma-enhanced chemical vapor deposition (PECVD), followed by N_2O annealing. In the proposed structure, by inserting other dielectrics between SiC and SiO_2, an adverse impact of near-interface traps located at $E_C - 2.77$ eV in SiO_2 [19] may be minimized. In addition, the deposited insulator may suppress the formation of the interfacial transition layer, as previously mentioned. The authors have succeeded in reducing the density of interface traps and enhancing the channel mobility, compared to N_2O oxidation, in SiC MISFETs fabricated with a deposited SiN_x/SiO_2 stack-gate structure annealed in N_2O.

II. Device Fabrication

For the fabrication of MIS capacitors, n-type 4H-SiC (0001) epilayers with a donor concentration of 1×10^{16} cm^{-3}, purchased from Cree, were prepared. The gate formation procedure used in this study is shown in Fig. 1. Fig. 1(a) and (b) shows the process to form SiN_x/SiO_2 stack-gate structures. After RCA cleaning with final hydrofluoric acid dip, the SiN_x layer was deposited by PECVD with SiH_4 and NH_3 as source gases. The thickness of deposited SiN_x was varied from

Manuscript received December 6, 2007; revised March 21, 2008. This work was supported in part by a Grant-in-Aid for Scientific Research (Grant 18206032) from the Japan Society for the Promotion of Science and in part by the Global COE Program (C09) from the Ministry of Education, Culture, Sports and Technology, Japan. The work of M. Noborio was supported by a Grant-in-Aid for Research Fellow from the Japan Society for the Promotion of Science. The review of this paper was arranged by Editor J. Zhao.

M. Noborio and J. Suda are with the Department of Electronic Science and Engineering, Kyoto University, Kyoto 615-8510, Japan (e-mail: noborio@semicon.kuee.kyoto-u.ac.jp).

T. Kimoto is with the Department of Electronic Science and Engineering and the Photonics and Electronics Science and Engineering Center, Kyoto University, Kyoto 615-8510, Japan.

Digital Object Identifier 10.1109/TED.2008.926644

0018-9383/$25.00 © 2008 IEEE

Authorized licensed use limited to: Kyoto University. Downloaded on June 29, 2009 at 02:11 from IEEE Xplore. Restrictions apply.

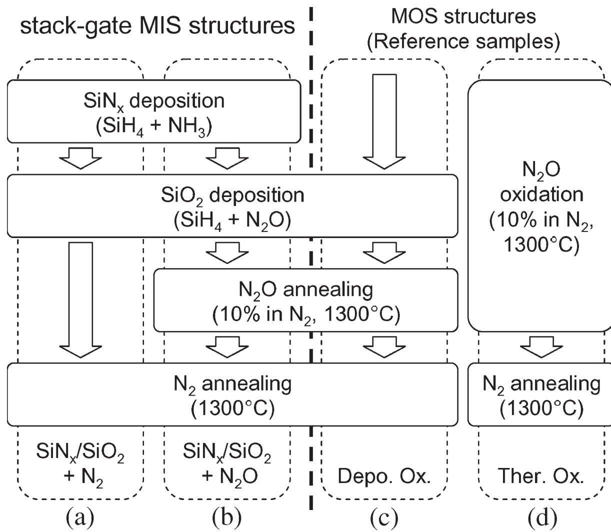

Fig. 1. Experimental procedure for stack-gate MIS structures annealed in (a) N_2 and (b) N_2O and MOS structures with (c) deposited oxide and (d) thermal oxide. MOS structures with oxide (without SiN_x layer) were fabricated as a reference.

2 to 10 nm. Then, subsequent SiO_2 deposition was carried out. In the SiO_2 deposition, SiH_4 and N_2O were used as source gases. The deposited thickness of SiO_2 was about 50 nm. The typical deposition temperature of SiN_x and SiO_2 was 400 °C. After the PECVD process, thermal annealing was performed in dry N_2O (10% diluted in N_2) and N_2 ambient at 1300 °C. N_2O-annealing time was varied, ranging from 30 min to 2 h [Fig. 1(b)]. During N_2O annealing, a portion of the SiN_x layer was oxidized and converted to the SiO_xN_y layer. Some of the samples were not annealed in N_2O [Fig. 1(a)]. MOS structures deposited by PECVD, with SiH_4 and N_2O as source gases [Fig. 1(c)], and formed by direct oxidation of SiC in dry N_2O (10% diluted in N_2) ambient at 1300 °C [Fig. 1(d)] [12] were also prepared as a reference. The reference samples have a SiO_2/SiC interface (without the SiN_x layer). The equivalent oxide thickness (EOT) calculated from the accumulation capacitance was about 60 nm. Al was evaporated on the backside and annealed at 600 °C for 10 min. The circular gate metal was Al, with a diameter of 520 μm for capacitance–voltage (C–V) measurements and 180 μm for current–voltage (I–V) measurements.

The authors have also fabricated n-channel MISFETs on p-type 4H-SiC (0001) epilayers with an acceptor concentration of 8×10^{15} cm^{-3} and on p-type 4H-SiC $(000\bar{1})$ epilayers with an acceptor concentration of 6×10^{15} cm^{-3}, purchased from Cree. The source–drain regions were formed by high-dose (5×10^{15} cm^{-2}) P^+ implantation at 300 °C. After ion implantation, high-temperature annealing was performed at 1600 °C for 15 min in Ar with a carbon cap to suppress surface roughening [21]. The formation of gate insulators was the same process as that previously mentioned. Ti/Al and Al annealed at 600 °C for 10 min were used as the backside and source–drain contacts, respectively. The gate metal was Al. The typical channel length L and width W were in the range of 25–100 μm and 200 μm, respectively. In order to estimate exact channel mobility and suppress short-channel effects [20], the authors adopted the design of long-channel lateral MOSFETs.

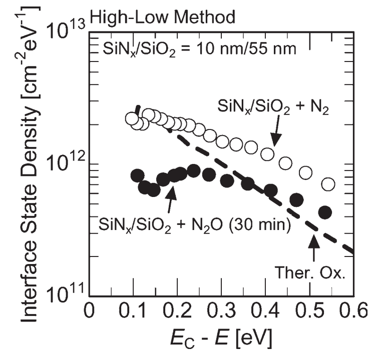

Fig. 2. Interface trap density of the SiN_x/SiO_2 stack-gate MIS capacitor annealed in N_2 and N_2O. The open and closed circles denote the MIS capacitors annealed in N_2 and N_2O, respectively. The SiN_x/SiO_2 stack-gate structure is 10 nm/50 nm. The dashed line represents the MOS capacitor with thermal oxide.

III. Experimental Result and Discussion

Quasi-static and high-frequency (1 MHz) C–V characteristics (C_{QS} and C_{HF}, respectively) were measured by using a simultaneous C–V system at room temperature under dark conditions. From the C–V curves, interface trap density was calculated by a high–low method.

The density of interface traps determined by a high–low method for stack-gate MIS capacitors with a deposited SiN_x/SiO_2 thickness of 10 nm/55 nm is represented in Fig. 2. The stack-gate MIS capacitors were annealed in N_2 or N_2O ambient for 30 min. Fig. 2 also shows the interface trap density for a MOS capacitor with thermal oxide grown in the N_2O ambient ("Ther. Ox."). The density of interface traps for the stack-gate MIS capacitor annealed in N_2O ("$SiN_x/SiO_2 + N_2O$ (30 min)") is lower than that for the stack-gate MIS capacitor annealed in N_2 ("$SiN_x/SiO_2 + N_2$"). N_2O annealing is more effective in reducing the interface trap than N_2 annealing for the SiN_x/SiO_2 stack-gate structure. Compared with thermal oxide, the stack-gate structure, followed by N_2O annealing, exhibits low interface trap density near the conduction band edge. The high density of the interface trap in the shallow energy region causes electron trapping, leading to low channel mobility in 4H-SiC MOSFETs [22].

Fig. 3 shows the results of the secondary ion mass spectrometry measurement for the stack-gate MIS capacitor, followed by N_2O annealing for 30 min (the same device as "$SiN_x/SiO_2 +$ N_2O (30 min)" shown in Fig. 2). The depth profiles of Si, C, N, and O atoms were measured. The depth resolution was about 3 nm. From Fig. 3, the oxygen atoms are clearly detected even between SiO_2 and SiC, indicating that the initial-SiN_x layer was oxidized during N_2O annealing. Nitrogen atoms are accumulated at the SiC/SiN_x interface, and the concentration of nitrogen atoms at the interface is about 1×10^{22} cm^{-3}.

The C–V characteristics of stack-gate MIS capacitors annealed in N_2O ambient for (a) 30 min and (b) 2 h with a deposited SiN_x/SiO_2 thickness of 10 nm/50 nm are represented in Fig. 4. The accumulation capacitance was reduced by increasing the N_2O-annealing time, which means that the SiN_x layer is oxidized during N_2O annealing and becomes an SiO_xN_y layer, as shown in Fig. 3. The MIS capacitor annealed

Authorized licensed use limited to: Kyoto University. Downloaded on June 29, 2009 at 02:11 from IEEE Xplore. Restrictions apply.

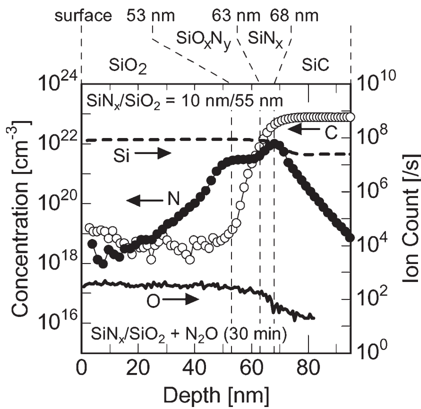

Fig. 3. Results of SIMS measurement for the stack-gate MIS capacitor with a $\mathrm{SiN}_x/\mathrm{SiO}_2$ thickness of 10 nm/55 nm annealed in N_2O for 30 min. The open and closed circles mean the concentration of carbon and nitrogen atoms, respectively. The dashed line denotes silicon-ion counts, and the solid line denotes oxygen-ion counts.

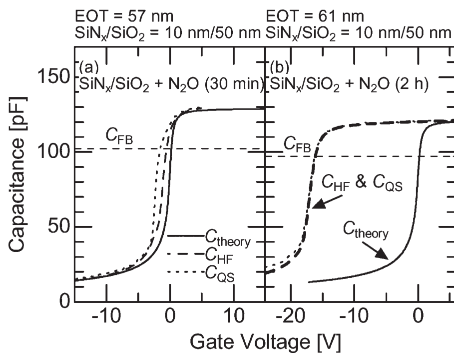

Fig. 4. High-frequency (C_{HF}) and quasi-static (C_{QS}) C–V curves for the $\mathrm{SiN}_x/\mathrm{SiO}_2$ stack-gate MIS capacitors annealed in N_2O for (a) 30 min and (b) 2 h. The thickness of the $\mathrm{SiN}_x/\mathrm{SiO}_2$ stack structure is 10 nm/50 nm. The theoretical C–V curve (C_{theory}) is also shown.

for 30 min shows a small difference between quasi-static and HF C–V curves. On the other hand, in the MIS capacitor annealed for 2 h, the high-frequency C–V curve is exactly similar to the quasi-static C–V curve [Fig. 4(b)], although a large negative flat-band voltage shift (about -15 V) is observed. The effective fixed charge density at the MIS interface of the stack-gate MIS capacitor annealed in N_2O for 30 min and 2 h is about $2 \times 10^{11}\ \mathrm{cm}^{-2}$ (positive) and $6 \times 10^{12}\ \mathrm{cm}^{-2}$ (positive), respectively. The stack-gate MIS capacitor, followed by N_2O annealing for 2 h, exhibits significant increase of effective fixed charge. Fig. 5 represents the interface trap density of stack-gate MIS capacitors annealed in N_2O for 30 min, 1 h, and 2 h (open circles, open squares, and closed circles, respectively, in Fig. 5), demonstrating that the interface trap density could significantly be reduced by extending the N_2O-annealing time. The stack-gate MIS capacitors, followed by N_2O annealing for 30 min and 1 h, show a slight decrease of interface trap density at the shallow energy region from the conduction band edge. The interface trap density of the stack-gate MIS capacitor annealed for 2 h is lower than that of thermal oxide at any energy levels investigated in this study, which are as low as $1 \times 10^{11}\ \mathrm{cm}^{-2}\mathrm{eV}^{-1}$ or below.

The I–V measurement was also performed. Fig. 6 shows the typical current density-electric field characteristics for the

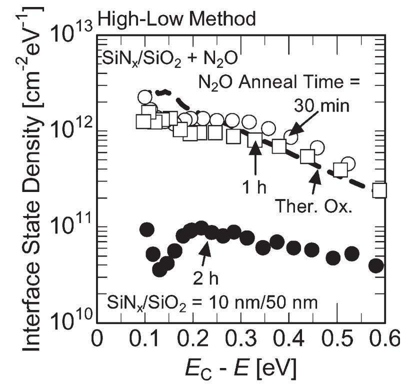

Fig. 5. Interface trap density of the $\mathrm{SiN}_x/\mathrm{SiO}_2$ stack-gate MIS capacitor annealed in N_2O. The open circles, open squares, and closed circles denote the MIS capacitors annealed for 30 min, 1 h, and 2 h, respectively. The $\mathrm{SiN}_x/\mathrm{SiO}_2$ stack-gate structure is 10 nm/50 nm. The dashed line corresponds to the MOS capacitor with thermal oxide.

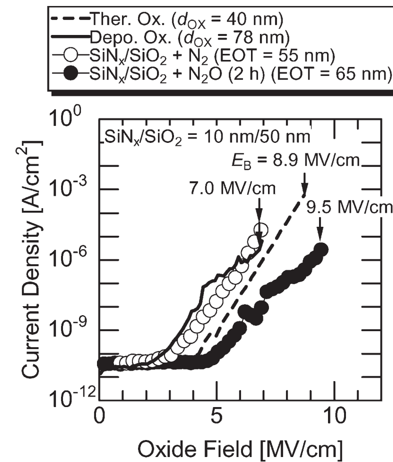

Fig. 6. Current density-electric field characteristics for the stack-gate MIS capacitors and MOS capacitors. The closed and open circles mean the characteristics of the stack-gate MIS capacitors annealed in N_2 and N_2O, respectively. The stack-gate structures have a $\mathrm{SiN}_x/\mathrm{SiO}_2$ thickness of 10 nm/50 nm. The dashed and solid lines denote the current density of MOS capacitors with thermal oxide and deposited oxide, respectively.

fabricated stack-gate MIS capacitors and MOS capacitors. The stack-gate MIS capacitors shown in Fig. 6 have a deposited $\mathrm{SiN}_x/\mathrm{SiO}_2$ thickness of 10 nm/50 nm. The oxide field was corrected by taking account of the flat-band-shift voltage. The typical ramp rate for I–V measurements was about 0.05 V/s. The gate current was drastically increased, leading to oxide breakdown, after the last point plotted in Fig. 6. The stack-gate MIS capacitor, followed by N_2 annealing ("$\mathrm{SiN}_x/\mathrm{SiO}_2 + \mathrm{N}_2$"), and the MOS capacitor with deposited oxide ("Depo. Ox.") show a low breakdown field of about 7 MV/cm. On the other hand, the thermal oxide ("Ther. Ox.") and stack-gate structure, followed by N_2O annealing ("$\mathrm{SiN}_x/\mathrm{SiO}_2 + \mathrm{N}_2\mathrm{O}$"), exhibit higher breakdown field than other samples. The stack-gate MIS capacitor annealed in N_2O for 2 h demonstrates low leakage current and high breakdown field. It has been reported that deposited insulators, such as ONO stack films formed by chemical vapor deposition (CVD) [13] and CVD oxide [23] on 4H-SiC, exhibit high dielectric reliability compared with thermal oxide. The MIS structure formed by $\mathrm{SiN}_x/\mathrm{SiO}_2$ deposition, followed by N_2O

Authorized licensed use limited to: Kyoto University. Downloaded on June 29, 2009 at 02:11 from IEEE Xplore. Restrictions apply.

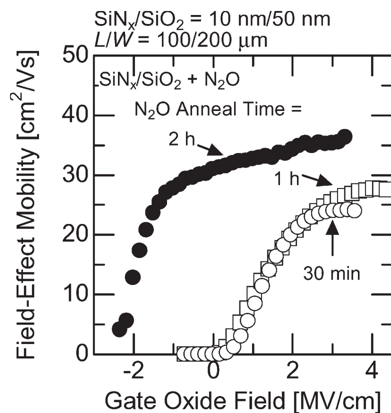

Fig. 7. Field-effect mobility of stack-gate MISFETs annealed in N_2O. The open circles, open squares, and closed circles correspond to the MISFETs annealed for 30 min (EOT = 56 nm), 1 h (57 nm), and 2 h (60 nm), respectively. These MISFETs have a deposited SiN_x/SiO_2 thickness of 10 nm/50 nm.

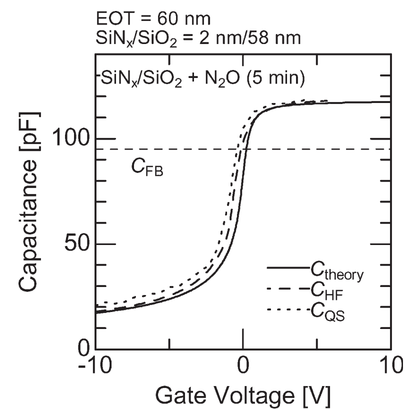

Fig. 8. C–V characteristics for the stack-gate MIS capacitor with a thin SiN_x thickness of 2 nm, followed by N_2O annealing for 5 min. The solid, dashed, and dotted lines denote the theoretical characteristics, high-frequency characteristics, and quasi-static characteristics, respectively.

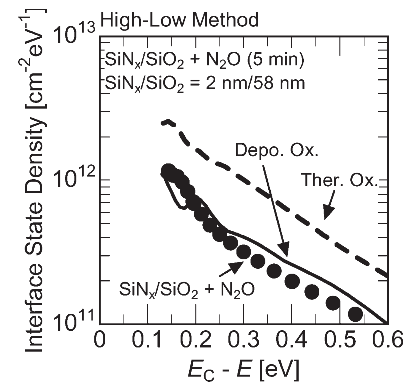

Fig. 9. Interface trap density for the N_2O-annealed stack-gate MIS capacitor with a SiN_x/SiO_2 thickness of 2 nm/58 nm. The closed circles denote the stack-gate MIS capacitor. The dashed line denotes the MOS capacitor with thermal oxide, and the solid line denotes that with deposited oxide.

annealing, may be one of the attractive approaches to improve the interface and dielectric characteristics.

Fig. 7 exhibits the field-effect mobility of MISFETs with N_2O-annealed SiN_x/SiO_2 stack-gate structure on the (0001)Si face. Open circles, open squares, and closed circles correspond to the MISFETs annealed for 30 min, 1 h, and 2 h, respectively. The horizontal axis of Fig. 7 is the gate oxide field, which is defined as V_G/EOT. The field-effect mobility increases with extending N_2O-annealing time. The increase of field-effect mobility can be correlated with the reduction of interface trap density, as shown in Fig. 5. As predicted from its low interface trap density, a high channel mobility over 30 $cm^2/V \cdot s$ was obtained when the N_2O-annealing time was 2 h. However, the MISFET annealed for 2 h shows a considerably shifted threshold voltage of -15 V, which agrees with the large negative shift of the flat-band voltage obtained in the MIS capacitor shown in Fig. 4(b).

In the stack-gate MIS structures, the SiN_x layer is oxidized during N_2O annealing, and a portion of the SiN_x layer is converted to the SiO_xN_y layer, as shown in Fig. 3. Then, the MIS structure is changed from a SiC/SiN_x/SiO_2 stack-gate structure to a SiC/thin-$SiN_x/SiO_xN_y/SiO_2$ one. The influence of traps inside the SiN_x layer may be decreased by thinning the residual SiN_x layer. Thus, the lower interface trap density may be obtained by extending the N_2O-annealing time. In the MIS structure annealed in N_2O for 2 h, the SiN_x layer may be completely oxidized and converted to the SiO_xN_y layer, and the stack-gate structure becomes the SiC/SiO_xN_y/SiO_2 structure, in which traps inside the SiN_x film disappeared, leading to the improvement of interface characteristics. The SiO_xN_y layer directly deposited on SiC by PECVD, followed by NO annealing, has already been investigated for the gate insulator of 4H-SiC MOS devices [24]. Compared with the previous report, the interface characteristics was significantly improved in the MIS structure, with the SiO_xN_y layer formed by oxidizing the SiN_x layer in this study. However, the stack-gate MIS structure annealed in N_2O for 2 h exhibits a large negative shift of the threshold voltage. Although the origin of this negative shift of the threshold voltage is unclear, a large positive charge should exist in the SiO_xN_y or at the SiO_xN_y/SiC interface [25]. In the case of the MIS capacitor, which was annealed for 1 h or shorter, it is possible that the negative charge (electrons) trapped at the interface traps compensates the positive charge located in the SiO_xN_y or at the SiO_xN_y/SiC interface. The MIS capacitor annealed for 2 h exhibits low interface trap density, and the negative charge captured at the interface traps is negligible, leading to a large negative shift of the flat-band voltage because of a large number of positive charges near the interface.

In order to reduce the large negative shift (positive charge), the initial thickness of the deposited SiN_x layer was decreased to 2 nm. The authors fabricated the stack-gate MIS capacitors and MISFETs, followed by N_2O annealing for 5 min. In order to completely oxidize the SiN_x layer, the short N_2O-annealing time was selected because of the very thin SiN_x layer. The optimum N_2O-annealing time depends on the initial-SiN_x layer thickness (a thinner initial-SiN_x layer needs a shorter N_2O-annealing time). The C–V curves for the MIS capacitor with a 2-nm-thick initial-SiN_x layer are shown in Fig. 8. The large negative shift of the flat-band voltage was not observed, and the flat-band voltage shift and effective fixed charge are very small, i.e., -0.3 V and 1.2×10^{11} cm^{-2}, respectively. Fig. 9 represents the density of the interface traps for the stack-gate

Authorized licensed use limited to: Kyoto University. Downloaded on June 29, 2009 at 02:11 from IEEE Xplore. Restrictions apply.

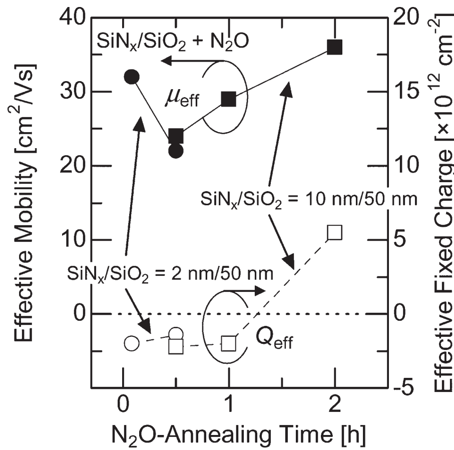

Fig. 10. N_2-annealing time dependence of effective mobility at the gate oxide field of 3 MV/cm and effective fixed charge calculated from the difference between the threshold voltages theoretically and experimentally obtained. The closed and open symbols mean the channel mobility and effective fixed charge, respectively. The circles denote the MISFETs with a SiN_x/SiO_2 thickness of 2 nm/50 nm, and the squares denote those with a SiN_x/SiO_2 thickness of 10 nm/50 nm.

MIS capacitor with the thin SiN_x layer. Although the interface trap density for the MIS capacitor with a SiN_x thickness of 2 nm is higher than 1×10^{11} $cm^{-2}eV^{-1}$, as shown by the closed circles in Fig. 5, it is still significantly lower than that for the MOS capacitor, with the thermal oxide grown in N_2O. Compared with the deposited oxide, followed by N_2O annealing, the stack-gate structure with the thin SiN_x layer shows a slightly low density of the interface trap in the deep energy region.

Fig. 10 shows the N_2O-annealing time dependence of effective channel mobility $\mu_{\rm eff}$ at the gate oxide field of 3 MV/cm and effective fixed charge $Q_{\rm eff}$ calculated from the difference between the theoretical and experimental threshold voltages. The MISFETs have a SiN_x/SiO_2 thickness of 2 nm/50 nm or 10 nm/50 nm. In the case of a SiN_x thickness of 10 nm, the effective mobility is increased by increasing the N_2O-annealing time, whereas the mobility decreases with increasing N_2O-annealing time in the MIS capacitor with a thin SiN_x thickness of 2 nm. In the MIS structures with the thin-SiN_x layer (2 nm), the time to completely oxidize the SiN_x layer is shorter than that for the MIS structures with a SiN_x thickness of 10 nm. Thus, the optimum N_2O-annealing time may be shorter.

Fig. 11 shows the subthreshold characteristics (log $I_D - V_G/$EOT characteristics) and the gate characteristics ($I_D - V_G/$EOT characteristics), and the field-effect mobility calculated from the gate characteristics is represented in Fig. 12, where the mobility of MOSFETs with thermal oxide and deposited oxide is also shown. The MISFET on the 4H-SiC (0001)Si face has a SiN_x/SiO_2 thickness of 2 nm/50 nm annealed for 5 min. The authors have also fabricated the MISFETs on the 4H-SiC $(000\bar{1})$C face with an acceptor concentration of 6×10^{15} cm^{-3}. In the C-face MISFET, the gate insulator was a SiN_x/SiO_2 (2 nm/50 nm) stack structure annealed for 5 min, which is the same as that in the Si-face MISFET shown in Figs. 11 and 12. The threshold voltage obtained from the extrapolation of gate characteristics is 5.3 V for the MISFET on the Si face and 2.7 V for that on the C face,

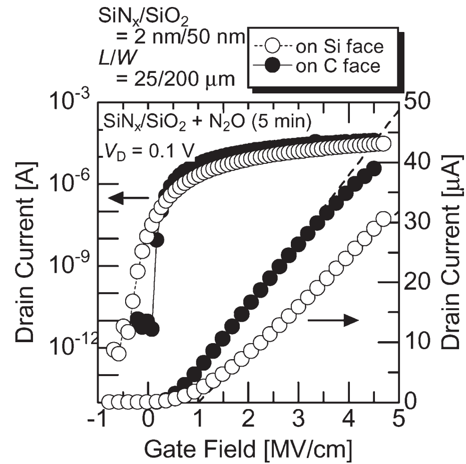

Fig. 11. Subthreshold and gate characteristics for stack-gate MISFETs annealed in N_2O for 5 min with a SiN_x/SiO_2 thickness of 2 nm/50 nm. The open and closed circles denote the MISFETs on the (0001)Si face and on the $(000\bar{1})$C face, respectively. (Both MISFETs have an EOT of 53 nm.)

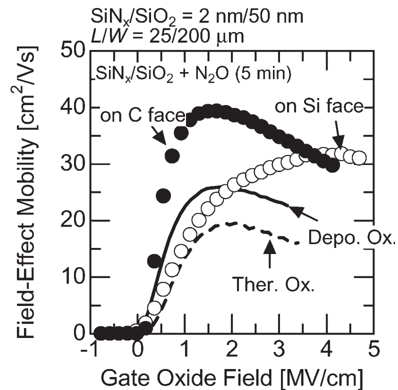

Fig. 12. Field-effect mobility for the stack-gate MISFETs annealed in N_2O for 5 min with a SiN_x/SiO_2 thickness of 2 nm/50 nm. The open and closed circles depict the mobility of MISFETs on the (0001)Si face and on the $(000\bar{1})$C face, respectively. These MISFETs have an EOT of 53 nm. The dashed line represents the mobility of the MOSFET with thermal oxide, and the solid line represents that with deposited oxide. The MOSFET with thermal oxide has an EOT of 97 nm, and that with deposited oxide has an EOT of 88 nm.

indicating the reduction of a large positive charge, as observed in Fig. 7. In Fig. 11, the MISFETs on the C face exhibits a steep slope in the subthreshold region of the log $I_D - V_G/$EOT plots, and the subthreshold slope of the MISFETs on the C face was 182 mV/dec. On the other hand, the drain–current of the MISFETs on the Si face gradually increases from a gate oxide field of -0.5 MV/cm, and the subthreshold slope was 556 mV/dec. These results imply that the interface trap density of the C-face MISFETs is still lower than that of the Si-face MISFETs. While the MOSFETs with thermal oxide and deposited oxide show a channel mobility of 20 and 25 $cm^2/V \cdot s$, respectively, a relatively high field-effect mobility of 32 $cm^2/V \cdot s$ is achieved in the stack-gate MISFETs on the (0001)Si face. This result indicates about 50% improvement in mobility. The channel mobility of MISFETs on the $(000\bar{1})$C face is 40 $cm^2/V \cdot s$, suggesting a promise of the C face for MIS-based device application, as previously reported by using wet oxidation [9].

Authorized licensed use limited to: Kyoto University. Downloaded on June 29, 2009 at 02:11 from IEEE Xplore. Restrictions apply.

IV. Conclusion

In this study, SiN_x/SiO_2 stack-gate structures deposited by PECVD and annealed in N_2O were investigated for 4H-SiC MIS devices. The interface characteristics for the MIS capacitor with a SiN_x thickness of 10 nm was significantly improved by extending the N_2O-annealing time to 2 h. During N_2O annealing, the deposited SiN_x layer is oxidized, and the influence of traps inside the SiN_x layer may be reduced. The MIS capacitor with a SiN_x/SiO_2 thickness of 10 nm/50 nm, followed by N_2O annealing for 2 h, exhibits a low interface trap density below 1×10^{11} $cm^{-2}eV^{-1}$. However, this MIS capacitor showed a large negative shift of the flat-band voltage, which indicates that positive charge exists in the oxidized SiN_x layer (SiO_xN_y layer) or at the SiO_xN_y/SiC interface. Compared with thermal oxide, the dielectric properties were also improved in the stack-gate structure annealed in N_2O. In order to suppress the large negative shift of the flat-band voltage, the initial thickness of the SiN_x layer was decreased to 2 nm. The fabricated MISFETs with a SiN_x/SiO_2 layer of 2 nm/50 nm annealed in N_2O for 5 min demonstrated a high channel mobility of 32 $cm^2/V \cdot s$ on the (0001)Si face and 40 $cm^2/V \cdot s$ on the $(000\bar{1})$C face, as well as "normally off" operation. The optimum N_2O-annealing time for the MIS capacitor depends on the initial-SiN_x thickness, because the time to completely oxidize the SiN_x layer is different for these MIS capacitors. The deposited SiN_x/SiO_2 stack-gate structure annealed in N_2O ambient is one of the promising candidates for the gate insulator of 4H-SiC MIS devices.

Acknowledgment

The authors would like to thank Prof. S. Noda of the Department of Electronic Science and Engineering, Kyoto University, for allowing the use of the PECVD system.

References

[1] H. Matsunami and T. Kimoto, "Step-controlled epitaxial growth of SiC: High quality homoepitaxy," *Mater. Sci. Eng.*, vol. R20, no. 3, pp. 125–166, 1997.
[2] [Online]. Available: http://www.infineon.com
[3] [Online]. Available: http://www.cree.com
[4] J. A. Cooper, Jr., M. R. Melloch, R. Singh, A. Agarwal, and J. W. Palmour, "Status and prospects for SiC Power MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 4, pp. 658–664, Apr. 2002.
[5] R. Kosugi, S. Suzuki, M. Okamoto, S. Harada, J. Senzaki, and K. Fukuda, "Strong dependence of the inversion mobility of 4H and 6H SiC(0001) MOSFETs on the water content in pyrogenic re-oxidation annealing," *IEEE Electron Device Lett.*, vol. 23, no. 3, pp. 136–138, Mar. 2002.
[6] P. Jamet, S. Dimitrijev, and P. Tanner, "Effects of nitridation in gate oxides grown on 4H-SiC," *J. Appl. Phys.*, vol. 90, no. 10, pp. 5058–5063, Nov. 2001.
[7] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, R. A. Weller, S. T. Pantelides, L. C. Feldman, O. W. Holland, M. K. Das, and J. W. Palmour, "Improved inversion channel mobility for 4H-SiC MOSFETs following high temperature anneals in nitric oxide," *IEEE Electron Device Lett.*, vol. 22, no. 4, pp. 176–178, Apr. 2001.
[8] L. A. Lipkin, M. K. Das, and J. W. Palmour, "N_2O processing improves the 4H-SiC: SiO_2 interface," *Mater. Sci. Forum*, vol. 389–393, pp. 985–988, 2002.
[9] K. Fukuda, M. Kato, K. Kojima, and J. Senzaki, "Effect of gate oxidation method on electrical properties of metal-oxide-semiconductor field-effect transistors fabricated on 4H-SiC $C(000\bar{1})$ face," *Appl. Phys. Lett.*, vol. 84, no. 12, pp. 2088–2090, Mar. 2004.
[10] H. Yano, H. Hirao, T. Kimoto, H. Matsunami, K. Asano, and Y. Sugawara, "High channel mobility in inversion layers of 4H-SiC MOSFETs by utilizing $(11\bar{2}0)$ face," *IEEE Electron Device Lett.*, vol. 20, no. 12, pp. 611–613, Dec. 1999.
[11] K. C. Chang, N. T. Nuhfer, and L. M. Porter, "High-carbon concentrations at the silicon dioxide-silicon carbide interface identified by electron energy loss spectroscopy," *Appl. Phys. Lett.*, vol. 77, no. 14, pp. 2186–2188, Oct. 2000.
[12] T. Kimoto, Y. Kanzaki, M. Noborio, H. Kawano, and H. Matsunami, "Interface properties of metal-oxide-semiconductor structures on 4H-SiC(0001) and $(11\bar{2}0)$ Formed by N_2O oxidation," *Jpn. J. Appl. Phys.*, vol. 44, no. 3, pp. 1213–1218, 2005.
[13] S. Tanimoto, "Impact of dislocations on gate oxide in SiC MOS devices and high reliability ONO dielectrics," *Mater. Sci. Forum*, vol. 527–529, pp. 955–960, 2006.
[14] G. Y. Chung, J. R. Williams, T. Isaacs-Smith, F. Ren, K. McDonald, and L. C. Feldman, "Nitrogen passivation of deposited oxide on n 4H-SiC," *Appl. Phys. Lett.*, vol. 81, no. 22, pp. 4266–4268, Nov. 2000.
[15] H. Yano, T. Hatayama, Y. Uraoka, and T. Fuyuki, "Characterization of 4H-SiC MOSFETs with NO-annealed CVD oxide," *Mater. Sci. Forum.*, vol. 527–529, pp. 971–974, 2006.
[16] M. Avice, U. Grossner, I. Pintilie, B. G. Svensson, M. Servidori, R. Nipoti, O. Nilsen, and H. Fjellvag, "Electrical properties of Al_2O_3/4H-SiC structures grown by atomic layer chemical vapor deposition," *J. Appl. Phys.*, vol. 102, no. 5, pp. 054 513-1–054 513-7, Sep. 2007.
[17] T. Kimoto, H. Kawano, M. Noborio, J. Suda, and H. Matsunami, "Improved dielectric and interface properties of 4H-SiC MOS structures processed by oxide deposition and N_2O annealing," *Mater. Sci. Forum*, vol. 527–529, pp. 987–990, 2006.
[18] S. Hino, T. Hatayama, N. Miura, T. Oomori, and E. Tokumitsu, "Fabrication and characterization of 4H-SiC MOSFET with MOCVD-grown Al_2O_3 gate insulator," *Mater. Sci. Forum*, vol. 556–557, pp. 787–790, 2007.
[19] G. Pensl, M. Bassler, F. Ciobanu, V. Afanas'ev, H. Yano, T. Kimoto, and H. Matsunami, "Traps at the SiC/SiO_2-interface," in *Proc. Mater. Res. Soc. Symp.*, 2001, vol. 640, pp. H3.2.1–H3.2.11.
[20] M. Noborio, Y. Kanzaki, J. Suda, and T. Kimoto, "Experimental and theoretical investigations on short-channel effects in 4H-SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 1954–1962, Sep. 2005.
[21] Y. Negoro, K. Katsumoto, T. Kimoto, and H. Matsunami, "Electronic behaviors of high-dose phosphorus-ion implanted 4H-SiC (0001)," *J. Appl. Phys.*, vol. 96, no. 1, pp. 224–228, Jul. 2004.
[22] N. S. Saks, *Silicon Carbide—Recent Major Advances*, W. J. Choyke, H. Matsunami, and G. Pensl, Eds. Berlin, Germany: Springer-Verlag, 2003, pp. 387–410.
[23] K. Fujihira, S. Yoshida, N. Miura, Y. Nakao, M. Imaizumi, T. Takami, and T. Oomori, "TDDB measurement of gate SiO_2 on 4H-SiC formed by chemical vapor deposition," presented at the Int. Conf. Silicon Carbide and Related Materials, Otsu, Japan, 2007, Paper We-3A-4.
[24] H. Yano, T. Hatayama, Y. Uraoka, and T. Fuyuki, "High temperature NO annealing of deposited SiO_2 and SiON Films on n-type 4H-SiC," *Mater. Sci. Forum*, vol. 483–485, pp. 685–688, 2005.
[25] F. H. P. M. Habraken and A. E. T. Kuiper, "Silicon nitride and oxynitride films," *Mater. Sci. Eng.*, vol. R12, no. 3, pp. 123–175, 1994.

Masato Noborio (S'06) was born in Nara, Japan, in 1981. He received the B.E. and M.E. degrees in electrical and electronic engineering from Kyoto University, Kyoto, Japan, in 2004 and 2006, respectively. He is currently working toward the Ph.D. degree in the Department of Electronic Science and Engineering, Kyoto University.

His research interests include short-channel effects in SiC MOSFETs, device simulation for SiC devices, designing and fabrication of SiC lateral power MOSFETs, and device processes.

Authorized licensed use limited to: Kyoto University. Downloaded on June 29, 2009 at 02:11 from IEEE Xplore. Restrictions apply.

Jun Suda was born in Ashikaga, Japan, in 1969. He received the B.E., M.E., and Ph.D. degrees from Kyoto University, Kyoto, Japan.

From 1992 to 1997, he worked on the growth of ZnSe-based semiconductors by molecular-beam epitaxy and the characterization of ZnMgSSe strained quantum well structures for optoelectronic applications. In 1997, he began research on group-III nitride semiconductors (III-N) and SiC as a Research Associate at Kyoto University. He is currently an Associate Professor with the Department of Electronics Science and Engineering, Kyoto University. He is the author or coauthor of more than 55 publications in peer-reviewed journals and international conference proceedings. He is the holder of 12 pending patents. His research interests include heteroepitaxial growth of III-N, functional integration of III-N and SiC materials by precise control of the heterointerface, design of wide-band-gap semiconductor devices, and characterization of device structure by scanning-probe microscopy.

Tsunenobu Kimoto (M'03–SM'06) received the B.E. and M.E. degrees in electrical engineering and the Ph.D. degree, based on his work on SiC epitaxial growth, characterization, and high-voltage diodes, from Kyoto University, Kyoto, Japan, in 1986, 1988, and 1996, respectively.

In April 1988, he joined Sumitomo Electric Industries, Ltd., Osaka, Japan, where he conducted research on amorphous Si solar cells and semiconducting diamond material. In 1990, he started his academic carrier as a Research Associate at Kyoto University. From September 1996 to August 1997, he was a Visiting Scientist with Linköping University, Linköping, Sweden, where he was involved in fast epitaxy of SiC and high-voltage Schottky diodes. He is currently a Professor with the Department of Electronic Science and Engineering and the Photonics and Electronics Science and Engineering Center, Kyoto University. He has also been involved in nanoscale Si devices and novel materials for nonvolatile memory. He has published more than 250 papers in scientific journals and international conference proceedings. His research interests include SiC epitaxial growth, optical and electrical characterization, ion implantation, MOS physics, and high-voltage devices.

Dr. Kimoto is a member of the Japan Society of Applied Physics; Institute of Electronics, Information, and Communication Engineering; and Institute of Electrical Engineering.

Authorized licensed use limited to: Kyoto University. Downloaded on June 29, 2009 at 02:11 from IEEE Xplore. Restrictions apply.