Evaluation of High Frequency Switching Capability of SiC Schottky Barrier Diode, Based on Junction Capacitance Model

Tsuyoshi Funaki, *Member, IEEE*, Tsunenobu Kimoto, *Senior Member, IEEE*, and Takashi Hikihara, *Member, IEEE*

***Abstract*—An SiC power device possesses features like high breakdown voltage, fast switching capability, and high temperature operation, and is expected to be superior to conventional Si power devices. This paper clarifies the switching capability of an SiC Schottky barrier diode (SBD) in rectification of high frequency ac voltage. The dynamic behavior of the SiC SBD for switching operation is modeled based on semiconductor physics and device structure, and is characterized by its dc current-voltage (I-V) and ac capacitance-voltage (C-V) characteristics. A C-V characterization system, which measures capacitance using a dc bias voltage corresponding to the maximum rated voltage of the SiC SBD, is developed. The C-V characteristics are evaluated through experiments over the rated voltage range. These results explain the punch-through structure and device parameters. The dynamic behavior of the proposed model is validated through experiments on half-wave rectification of ac voltages over a wide frequency range. As a relational expression of voltage, current, and frequency of an applied ac sinusoidal voltage, the performance criterion of the device is established for rectification. The model also quantitatively assesses the switching capability of SiC SBDs. The model and performance criteria are beneficial for circuit design and device evaluation.**

***Index Terms*—Capacitance-voltage characteristics, device modeling, operation criterion, SiC Schottky barrier diode, switching.**

I. Introduction

As a semiconductor material, silicon carbide (SiC) possesses several characteristics that are superior to silicon (Si) [1]–[3]. Its wide bandgap properties include high temperature and voltage operational capabilities [4]–[8]. The high breakdown electric field of 4H-SiC ($2.2–4 \times 10^6$ V/cm) allows fabrication of devices with a higher breakdown voltage, and thinner and higher doped voltage-blocking layer [9]. Although the electron mobility of 4H-SiC is slightly lower than that of Si (1140 cm^2/V.s for SiC and 1360 cm^2/V.s for Si, respectively, at low doping concentrations), a higher switching speed is expected, as the carrier-transit time is less in the case of thin blocking layer. This expectation is applicable to a majority carrier device [10], such as an SiC Schottky barrier diode (SBD). Fast switching capability is also expected for a minority carrier device, because a short carrier lifetime in high impurity concentrations and the thin voltage-blocking layer result in a lower minority carrier storage effect. Many papers have highlighted the fast switching capability of SiC devices [11]–[17], and demonstrated that the switching characteristics are theoretically and experimentally superior to those of conventional Si fast recovery devices. SiC devices can operate at a higher switching frequency, but the practical upper limit of the switching frequency has not been accurately determined.

The thinner and higher impurity concentration in the voltage-blocking layer of the SiC device may induce a junction capacitance larger than that in an Si device. The junction capacitance of a semiconductor device affects its switching operation, but this effect is not completely understood for high voltage SiC power devices. Therefore, the authors focused on the modeling and characterization of the junction capacitance, and its voltage dependency, in high voltage SiC power devices, and have developed a system for measuring the voltage dependency of the junction capacitance of a high voltage power device over its entire rated voltage range [18][19] and clarified the punch-through device structure of SiC SBDs, based on the measured capacitance-voltage (C-V) characteristics [18]. SiC SBD is a majority carrier device and does not need to take into consideration the minority carrier storage effect. Thus, this paper takes the C-V characteristics of the device into account while discussing the dynamic behavior of SiC SBD switching operation. The operation of SiC SBD for sinusoidal ac voltage rectification is used to study the switching operation and facilitate the characteristics evaluation in this discussion. This paper experimentally characterizes the device behavior and evaluates it, theoretically and numerically, with an established SiC SBD model. In addition, the criterion for SiC SBD rectification is derived, based on the SiC SBD model, and a quantitative index for the characterized device is provided.

This paper is organized as follows: Section II describes the punch-through structure of the SiC SBD and the C-V characteristics for the blocking condition; Section III characterizes and models the SiC SBD; Section IV evaluates its dynamic behavior in high frequency ac rectification; and Section V gives its criterion of switching performance. Finally, Section VI provides the conclusions drawn from this work.

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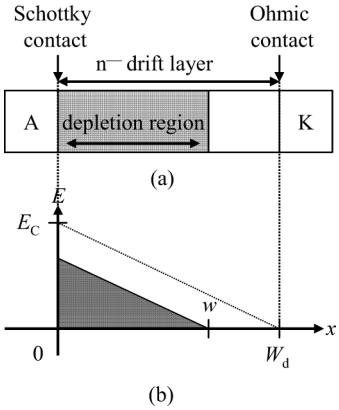

Fig. 1. Non punch-through Schottky barrier diode. (a) Structure, (b) Electric field distribution.

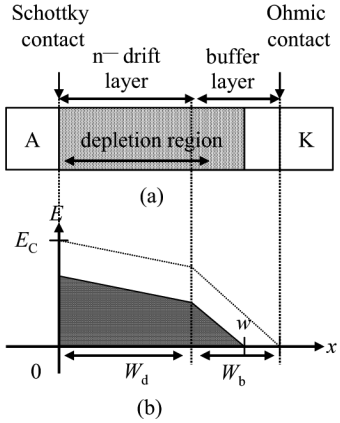

Fig. 2. Punch-through Schottky barrier diode. (a) Structure, (b) Electric field distribution.

II. The Punch-Through Structure and Capacitance-Voltage Characteristics

The P-N junction, or Schottky barrier, in a diode is what gives the diode its rectification property. The carriers are extracted from the doped impurities in the semiconductor around the junction in accordance with the applied reverse voltage, thus, forming a depletion region. A diode has capacitive characteristics at blocking conditions. The punch-through structure, when applied to an SiC SBD, is expected to affect the expansion of the depletion region by the application of reverse voltage. The reverse voltage dependency of the junction capacitance of the SiC SBD with a punch-through structure is derived and modeled in this section. The punch-through voltage is evaluated for a device with optimally designed dimensions and parameters, to estimate the voltage required for characterizing the punch-through phenomena in the measurement.

A. C-V Characteristics for Non Punch-Through SBD

The junction capacitance of the SBD at the blocking conditions is related to the amount of depleted charge. The applied junction voltage of the SBD results from the electric field distribution across the depleted region. The one-dimensional structure and electric field distribution of a simple non punch-through SBD, at a reverse voltage blocking condition, are given in Fig. 1(a) and (b). The left side of the device is the Schottky metal that behaves as an anode, and the depletion region expands from the Schottky junction toward the right of the drift region, in accordance with the applied reverse voltage, which corresponds to the shaded area in Fig. 1(b).

The relation between the depletion region width w and the applied reverse voltage $V_{\rm ka}$ to the SBD is given by (1), [20].

$$w = \sqrt{\frac{2\varepsilon_{\rm s}}{eN_{\rm d}}}\sqrt{V_{\rm ka}+V_{\rm bi}} \cong \sqrt{\frac{2\varepsilon_{\rm s}}{eN_{\rm d}}}\sqrt{V_{\rm ka}} \tag{1}$$

Here, $V_{\rm bi}$ is the diffusion potential, which is negligible for high $V_{\rm ka}$, ε_s is the dielectric constant of the SiC semiconductor, e is the unit electron charge, $N_{\rm d}$ is the impurity concentration in the drift region, and the drift region is assumed to be uniformly doped for simplicity of analysis.

The total depleted charge $Q(V_{\rm ka})$ corresponding to the applied reverse voltage $V_{\rm ka}$, is expressed as the product of the charge density at drift region $eN_{\rm d}$, depletion width w, and junction area A. Then, the differential capacitance of junction $C(V_{\rm ka})$ to the variation in applied voltage is derived as a function of $V_{\rm ka}$ in (2).

$$\begin{cases} Q(V_{\rm ka}) = eN_{\rm d}wA \cong A\sqrt{2\varepsilon_{\rm s}eN_{\rm d}}\sqrt{V_{\rm ka}} \\ C(V_{\rm ka}) = \frac{d}{dV_{\rm ka}}Q(V_{\rm ka}) \cong A\sqrt{\frac{\varepsilon_{\rm s}eN_{\rm d}}{2}}\frac{1}{\sqrt{V_{\rm ka}}} \end{cases} \tag{2}$$

The relations between the maximum depletion width, the breakdown voltage, and the impurity concentration of the drift layer are given in the Appendix.

B. C-V Characteristics for a Punch-Through SBD

The resistance of the drift layer $R_{\rm d}$ for a non punch-through SBD increases with the square of the device breakdown voltage $V_{\rm bd}$, as given in (A2). The rising voltage drop, from the product of the resistance and conduction current, becomes unacceptable for a high voltage power device. The punch-through structure of the device, depicted in Fig. 2(a), was introduced to improve the tradeoff between breakdown voltage and the drift layer resistance [20]. The structure consists of a low impurity concentration drift layer, and a high concentration buffer (field stop) layer. The electric field distribution in the depleted region, and the depletion region expansion for a punch-through SBD, differ from that of a non punch-through SBD. This subsection compares the C-V characteristics of these two types of SBDs. We assume a punch-through SBD having the same breakdown voltage as the non punch-through SBD, and design the device geometry to satisfy this condition.

Initially, the depletion region expands from the Schottky junction into the drift region when the reverse bias voltage is applied to a punch-through SBD. The punch-through occurs when the depletion region reaches the end of the drift layer ($w = W_{\rm d}$) while increasing the reverse voltage applied to the punch-through voltage $V_{\rm pt}$. $V_{\rm pt}$ is calculated from (1) with a drift layer width $w = W_{\rm d}$, as shown in (3).

$$V_{\rm pt} = \frac{eN_{\rm d}W_{\rm d}^2}{2\varepsilon_{\rm s}} \tag{3}$$

The characteristics of the punch-through SBD, related to the depletion in the drift layer, are same as those of the non punch-through SBD prior to the punch-through ($w < W_{\rm d}$). After

punch through ($W_{\rm d} < w$), the depletion region expands into the buffer layer, but the expansion rate degrades abruptly. The electric field distribution $E(x)$ for the punch-through condition ($W_{\rm d} < w$) is obtained from Poisson's equation to the respective layer and the boundary conditions of $E(w) = 0$, and the continuity of electric field at $x = W_{\rm d}$ as (4). Here, $N_{\rm b}$ is the impurity concentration at the buffer layer, which is some order higher than $N_{\rm d}$.

The electric field distribution for punch through is shown in Fig. 2(b). The relation between the applied reverse voltage $V_{\rm ka}$ and the depletion width w for punch-through is calculated from (4), as shown in (5).

$$V_{\rm ka} \cong \frac{e}{2\varepsilon_{\rm s}}\left[(N_{\rm d}-N_{\rm b})W_{\rm d}^2 + N_{\rm b}w^2\right] \tag{5}$$

Then, the depletion width w for the punch-through condition is obtained as a function of the applied reverse voltage $V_{\rm ka}$ in (6).

$$w \cong \sqrt{\frac{2\varepsilon_{\rm s}}{eN_{\rm b}}V_{\rm ka} + \left(1-\frac{N_{\rm d}}{N_{\rm b}}\right)W_{\rm d}^2} \tag{6}$$

The maximum depletion width, $W_{\rm d} + W_{\rm b}$, for a punch-through SBD is obtained as a function of the critical electric field $E_{\rm c}$ for the maximum electric field at $x = 0$, from (4), as shown in (7).

$$W_{\rm d} + W_{\rm b} = \frac{N_{\rm b}-N_{\rm d}}{N_{\rm b}}W_{\rm d} + \frac{\varepsilon_{\rm s}}{eN_{\rm b}}E_{\rm c} \tag{7}$$

Here, $W_{\rm b}$ is the maximum depletion width in the buffer layer.

The breakdown voltage of a punch-through SBD is also calculated from (4). It can be expressed as a function of the doping concentrations $N_{\rm b}$ and $N_{\rm d}$, the drift layer width $W_{\rm d}$, and the critical electric field $E_{\rm c}$, as in (8).

$$\begin{aligned} V_{\rm bd} &= \frac{e}{2\varepsilon_{\rm s}}\left\{W_{\rm d}^2 N_{\rm d}\left(-1+\frac{N_{\rm d}}{N_{\rm b}}\right)\right. \\ &\quad \left. + W_{\rm d}2(N_{\rm b}-N_{\rm d})\frac{\varepsilon_{\rm s}E_{\rm c}}{eN_{\rm b}} + \frac{\varepsilon_{\rm s}^2E_{\rm c}^2}{e^2N_{\rm b}}\right\} \\ &\cong \frac{e}{2\varepsilon_{\rm s}}\left\{-W_{\rm d}^2N_{\rm d} + 2W_{\rm d}\frac{\varepsilon_{\rm s}E_{\rm c}}{e}\right\} \end{aligned} \tag{8}$$

Here, for approximation it is assumed that $N_{\rm d} \ll N_{\rm b}$.

The charge depleted from the junction can be obtained as a function of the applied voltage $V_{\rm ka}$, as in (9).

The differential capacitance of the junction $C(V_{\rm ka})$ is derived for the punch-through SBD as a function of the applied voltage $V_{\rm ka}$, as shown in (10).

$$\begin{cases} C(V_{\rm ka}) \cong A\sqrt{\frac{\varepsilon_{\rm s}eN_{\rm d}}{2V_{\rm ka}}} & 0 \le V_{\rm ka} \le V_{\rm pt} \\ C(V_{\rm ka}) \cong A\sqrt{\frac{\varepsilon_{\rm s}^2eN_{\rm b}}{2\varepsilon_{\rm s}V_{\rm ka}+(N_{\rm b}-N_{\rm d})eW_{\rm d}^2}} & V_{\rm pt} < V_{\rm ka} \le V_{\rm bd} \end{cases} \tag{10}$$

The impurity concentration in the drift region can be estimated from (8) as a function of the breakdown voltage $V_{\rm bd}$, as shown in (11).

$$N_{\rm d} = \frac{2\varepsilon_{\rm s}}{eW_{\rm d}^2}(W_{\rm d}E_{\rm c} - V_{\rm bd}) \tag{11}$$

The combined resistance for the drift and buffer layers is expressed as a function of the impurity concentrations $N_{\rm d}$ and $N_{\rm b}$ and layer width $W_{\rm d}$, $W_{\rm b}$, as in (12).

$$\begin{aligned} R_{\rm d} &= \frac{W_{\rm d}}{e\mu N_{\rm d}A} + \frac{W_{\rm b}}{e\mu N_{\rm b}A} \\ &= \frac{W_{\rm d}^3}{\mu 2\varepsilon_{\rm s}(W_{\rm d}E_{\rm c}-V_{\rm bd})A} + \frac{W_{\rm b}}{e\mu N_{\rm b}A} \end{aligned} \tag{12}$$

The difference in the doped impurity concentrations between the drift and buffer layer $N_{\rm d} \ll N_{\rm b}$ makes the first term in (12) govern the resistance $R_{\rm d}$. The resistance $R_{\rm d}$ gives a minimum value $R_{\rm d-min}$ at a drift layer width of $W_{\rm d-min}$, when $(d/dW_{\rm d})R_{\rm d} = 0$, as given by (13).

$$\begin{cases} W_{d-\min} = \frac{3V_{\rm bd}}{2E_{\rm c}} \\ R_{d-\min} = \frac{27}{8}\frac{V_{\rm bd}^2}{\mu\varepsilon_{\rm s}AE_{\rm c}^3} \end{cases} \tag{13}$$

The minimized resistance $R_{\rm d-min}$ of a punch-through SBD with an optimized drift layer width from (13) becomes 84% of that of the non punch-through SBD, with the same breakdown voltage as in (A2). The punch-through voltage for the optimized drift layer width $V_{\rm pt-opt}$ is derived as in (14), by substituting (11) and (13) into (3).

$$\begin{aligned} V_{\rm pt-opt} &= \frac{eW_{\rm d-min}^2}{2\varepsilon_{\rm s}}\frac{2\varepsilon_{\rm s}}{eW_{\rm d}^2}(W_{d-\min}E_{\rm c} - V_{\rm bd}) \\ &= W_{\rm d-min}E_{\rm c} - V_{\rm bd} \\ &= \frac{3V_{\rm bd}}{2E_{\rm c}}E_{\rm c} - V_{\rm bd} = \frac{1}{2}V_{\rm bd} \end{aligned} \tag{14}$$

$$\begin{cases} E(x) = -\frac{e}{\varepsilon_{\rm s}}[N_{\rm d}(x-W_{\rm d}) + N_{\rm b}(W_{\rm d}-w)] & 0 \le x \le W_{\rm d} \\ E(x) = -\frac{e}{\varepsilon_{\rm s}}N_{\rm b}(x-w) & W_{\rm d} < x \le w \end{cases} \tag{4}$$

$$\begin{cases} Q(V_{\rm ka}) = eN_{\rm d}wA \cong A\sqrt{2\varepsilon_{\rm s}eN_{\rm d}V_{\rm ka}} & 0 \le V_{\rm ka} \le V_{\rm pt} \\ Q(V_{\rm ka}) = eN_{\rm d}W_{\rm d}A + eN_{\rm b}(w-W_{\rm d})A \\ \cong A(N_{\rm d}-N_{\rm b})eW_{\rm d} + A\sqrt{(N_{\rm b}-N_{\rm d})N_{\rm b}e^2W_{\rm d}^2 + 2\varepsilon_{\rm s}eN_{\rm b}V_{\rm ka}} & V_{\rm pt} < V_{\rm ka} \le V_{\rm bd} \end{cases} \tag{9}$$

The punch-through voltage for an optimally designed device is half of the breakdown voltage. Thus, it is necessary to apply more than 50% of the breakdown voltage to observe the punch-through phenomena in the experiment.

The next section characterizes the C-V properties of the studied punch-through structure in SiC SBDs, and discusses the modeling of junction capacitance.

III. C-V Characterization and Modelling of SiC SBD

A. C-V Characterization Setup

The previous section derived the characteristic equations for the differential capacitance of a punch-through SBD as a function of the applied reverse bias voltage, and estimated the punch-through voltage for the optimally designed device. These equations indicate that it is possible to observe the punch-through phenomena in the C-V characteristic measurements, and evaluate the parameters and geometries of the device from the measured results. This subsection gives a description of the C-V characterization setup, which allows to measure the differential capacitance of the device using a small ac signal by applying a reverse biasing voltage up to the device's high rated voltage.

The basic specifications of the studied SiC SBD, which has a punch-through structure, are given in Table I. The rated voltage is 600 V, and the breakdown voltage of the device is expected to be higher than 600 V. When the impurity concentration and the width of the drift layer are optimally designed and fabricated, punch-through occurs at half of the breakdown voltage. Therefore, the C-V characterization system must be able to impose a reverse biasing voltage exceeding 300 V on the device to induce the punch-through phenomena. The developed C-V characterization system can apply and automatically sweep dc reverse bias voltage from 0 to 600 V. Fig. 3 shows the circuit configuration of the dc bias fixture for the measurement.

The C-V characterization system utilizes an LCR meter (HIOKI 3522) to measure the capacitance, and the fixture prevents the dc bias voltage from imposing itself on the LCR meter without disturbing the measurement accuracy. The basic circuit topology is referred to in [21], but the configuration details have been refined to cope with the high dc voltage. The C-V characteristics are generally evaluated using a 1-MHz ac signal. However, the self-resonant frequency of the capacitors (polypropylene film type), which were used to block the high voltage, is lower than 1 MHz. Therefore, 100 kHz was chosen as the ac characterization signal. The measured results obtained from the measurement setup were validated in [18].

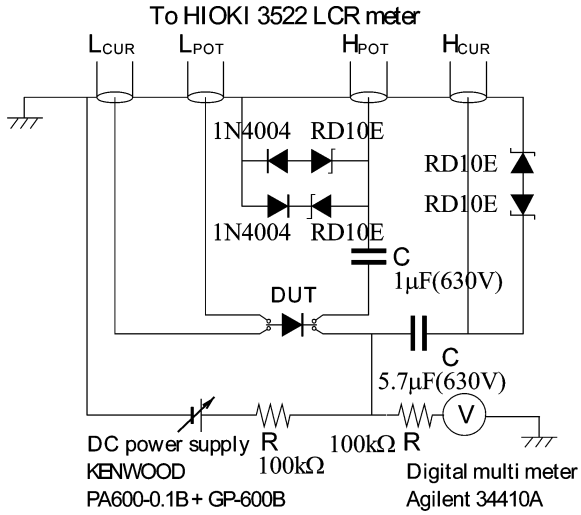

Fig. 3. Circuit configuration of high dc voltage bias fixture for C-V characterization.

TABLE I
SPECIFICATIONS OF STUDIED SiC SBD

Type	SDP06S60
Rated voltage	600 V
Rated current	6 A
Total capacitive charge	21 nC
Active area	1.191 mm^2
Manufacturer	Infineon

B. C-V Characterization and Modeling of SiC SBD

The differential capacitance of SiC SBD relative to the reverse dc bias voltage $V_{\rm ka}$ is measured in this section. The geometry of the punch-through structure is assessed from the measured results. Fig. 4(a) shows the measured capacitance as a function of the reverse dc bias voltage, which is swept from 0 V to the rated voltage of 600 V with 1 V step. The capacitance at zero bias voltage is 264 pF, which decreases as the reverse dc biasing voltage increases. The capacitance almost saturates at 26 pF, around 200 V. This saturation indicates an end in the expansion of the depletion region, which is induced by the punch-through phenomenon. The differential capacitance obtained in (10) introduces the punch-through effect in the device. However, it is difficult to identify the parameters of the device model from these characterized results. Therefore, (10) is transformed to a function of the applied reverse dc bias voltage $V_{\rm ka}$ by taking the reciprocal of the squared capacitance, as given in (15). Here, $C_{\rm j0}$ is the capacitance at zero bias, $V_{\rm bipt}$ is the effective built-in potential for the punch-through condition, and $C_{\rm jpt}$ is the zero bias capacitance for the punch-through condition.

This equation shows that the $(1/C^2) - V$ characteristics, before and after punch-through, can be expressed as a linear function of the applied dc bias voltage. Fig. 4(b) shows that the measured result is redrawn as $(1/C^2) - V$ characteristics. It is clearly seen that the result can be divided into two parts, and

$$\begin{cases} \frac{1}{C(V_{\rm ka})^2} = \frac{1}{C_{\rm j0}^2}(V_{\rm ka} + V_{\rm bi}) \cong \frac{2}{\varepsilon_{\rm s} e N_{\rm d} A^2} V_{\rm ka} & 0 \le V_{\rm ka} \le V_{\rm pt} \\ \frac{1}{C(V_{\rm ka})^2} = \frac{1}{C_{\rm jpt}^2}(V_{\rm ka} + V_{\rm bipt}) \cong \frac{2}{\varepsilon_{\rm s} e N_{\rm b} A^2} V_{\rm ka} + \frac{(N_{\rm b} - N_{\rm d}) W_{\rm d}^2}{\varepsilon_{\rm s}^2 N_{\rm b} A^2} & V_{\rm pt} < V_{\rm ka} \le V_{\rm bd} \end{cases} \tag{15}$$

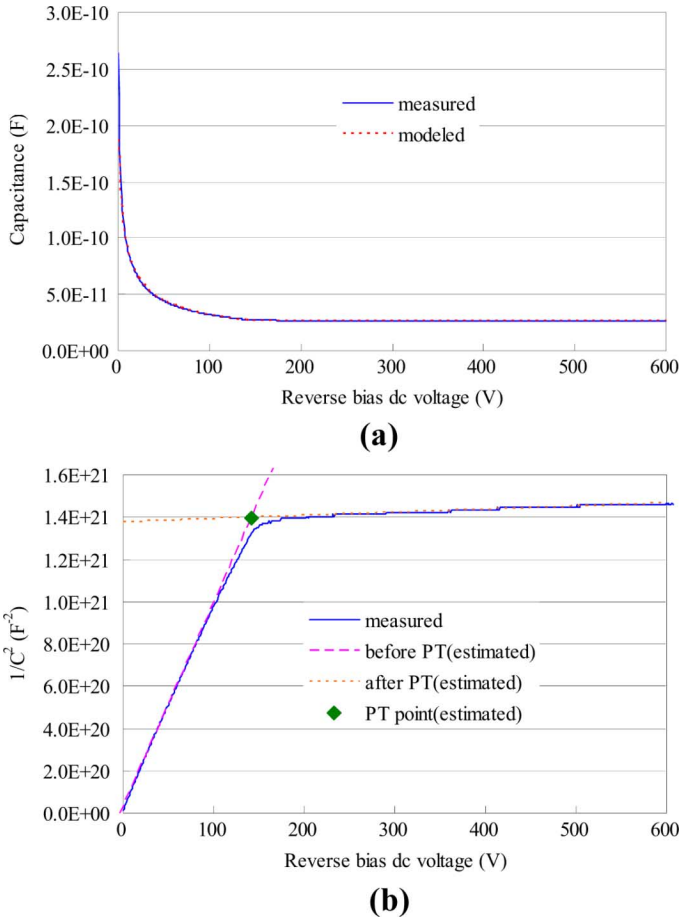

Fig. 4. Measured C-V characteristics. (a) C-V characteristics, (b) $C^{-2} - V$ characteristics.

TABLE II
EXTRACTED DEVICE PARAMETERS OF STUDIED SIC SBD

R_s	0.090 Ω
n	1.008
I_s	3.536×10^{-16} A
V_{pt}	142.3 V
C_{j0}	322 pF
V_{bipt}	9215 V
C_{j0pt}	2589 pF

expresses the characteristics given in (15). The depletion layer expands through the drift region, from the Schottky junction boundary toward the buffer layer, as the reverse dc bias voltage increases from 0 to 150 V. It eventually reaches the buffer layer, and gradually penetrates it during the second phase when the voltage exceeds 150 V. Before and after the punch-through phenomenon, the coefficients of the linear equation in (15) are approximated by the linear least means square method. The extracted values are given in Table II. The punch-through voltage can be estimated as the intersection of the extrapolated equation from (15), which becomes 142 V as shown in Fig. 4(b). Then, the n^- drift layer width and the donor concentrations are respectively estimated as $W_d = 3.8\ \mu$m, $N_d = 1.1 \times 10^{16}$ cm^{-3}, and $N_b = 6.9 \times 10^{17}$ cm^{-3}.

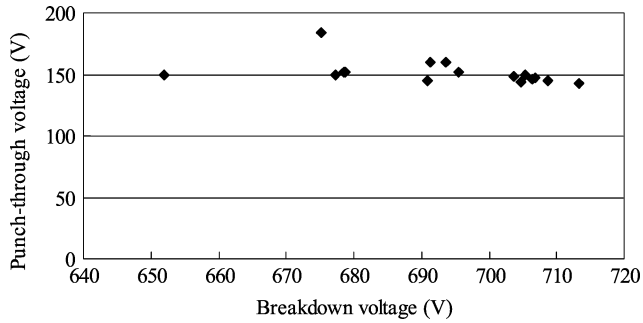

Fig. 5. Cross correlation between breakdown and punch-through voltage.

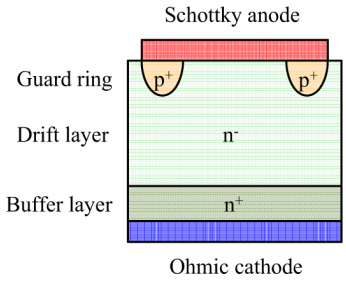

Fig. 6. Cross section of punch through SiC SBD.

The last section shows that a optimally designed punch-through structure to minimize the resistance gives a punch-through voltage at half of the breakdown voltage. Therefore, the studied SiC SBD has a lower punch-through voltage than the optimum value of 300 V (=600/2 V). That is, the studied device has a lower impurity concentration, or thinner drift layer than the optimum value from (13), which results in higher resistance.

Fig. 5 shows a cross-correlation of the measured punch through and breakdown voltage for 16 devices with identical specifications. The breakdown voltage of the SiC SBD was measured with a Tektronix 371B curve tracer. The punch-through voltage is approximately 150 V, with a small variance, which means that the drift layer in the devices are uniformly fabricated. However, the breakdown voltage scatters over a wide range. This indicates that either the punch-through and breakdown voltages do not cross correlate, or the breakdown voltage is independent of the punch-through voltage, which would suggest that the breakdown occurs in a part other than the Schottky junction, e.g., the guard ring around the anode, as shown in Fig. 6. Therefore, the SiC SBD drift layer can withstand higher voltages, and the width of the drift layer and impurity concentration can be improved to further reduce the resistance.

IV. DYNAMIC BEHAVIOR OF THE SIC SBD

The previous section characterizes and models the punch-through phenomenon in the SiC SBD. The devices were evaluated based on the measured differential capacitance at the junction related to the applied reverse bias dc voltage. This section focuses on the dynamic behavior of the SiC SBD in its switching response to a large signal. This experiment studies the high frequency switching capability of the SiC SBD in a half-wave rectification circuit with a non-inductive resistance load, and validates the device model.

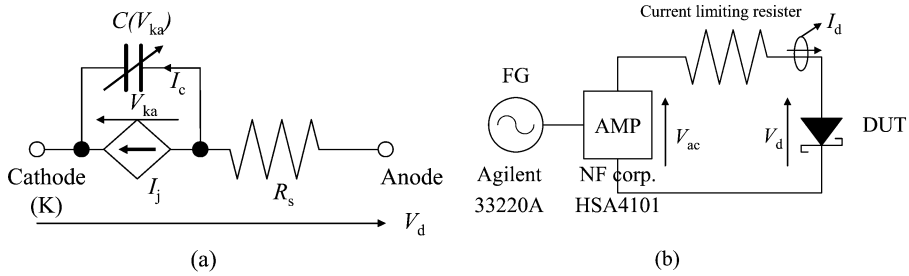

Fig. 7. SiC SBD model and experimental circuit. (a) SiC SBD model, (b) Experimental circuit.

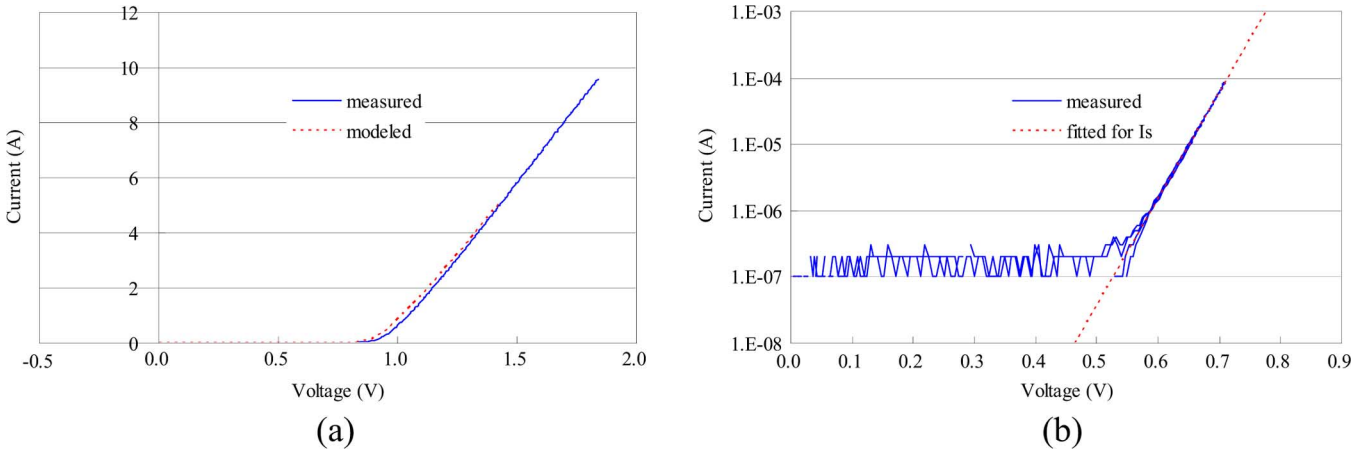

Fig. 8. I-V characteristics of SiC SBD. (a) Large current region (linear plot), (b) Small current region (semi-log plot).

A. SiC SBD Model for Analyzing Dynamic Behavior

Fig. 7(a) depicts an SiC SBD model for analyzing the dynamic behavior. The controlled-current source and the series-connected resistance $R_{\rm s}$ give the I-V static characteristics of the device. The variable capacitance $C(V_{\rm ka})$ in the circuit represents the junction capacitance of the SiC SBD, considering the punch-through phenomena, from (10). The junction capacitance maintains its value at $V_{\rm ka} = 0$ under forward conduction conditions, and behaves as a diffusion capacitance. The circuit equation of the SiC SBD model is expressed as in (16).

$$\begin{cases} I_{\rm j} = I_{\rm s}\left[\exp\left(\frac{-qV_{\rm ka}}{nkT}\right) - 1\right] \\ V_{\rm d} = -V_{\rm ka} + R_{\rm s}\left(I_{\rm j} + I_{\rm c}\right) = -V_{\rm ka} + R_{\rm s}I_{\rm d} \\ \frac{d}{dt}V_{\rm ka} = \frac{-1}{C(V_{\rm ka})}I_{\rm c} \end{cases} \tag{16}$$

Here, n is the ideality factor, k is the Boltzman's constant, T is the temperature (K), and $I_{\rm s}$ is the saturation current.

The current $I_{\rm j}$ and resistance $R_{\rm s}$ are determined from the measured I-V characteristics. These I-V characteristics, shown in Fig. 8, are measured using Tektronix 370B and 371B curve tracers for the small and large current regions. The resistance $R_{\rm s}$ and ideality factor n are extracted from the large current region, where the variation of $V_{\rm ka}$ is insensitive to changes in $I_{\rm j}$. The saturation current $I_{\rm s}$ is estimated from the small current region by subtracting the series resistance voltage drop from the measured value. The extracted parameters are given in Table II.

B. Experimental Study of Rectification Performance of the SiC SBD

An SiC power device is used for high frequency switching. The switching performance of the diode is generally evaluated by its transient recovery time $(t_{\rm rr})$, induced by the accumulated minority carrier in the drift region. The SiC SBD is a majority carrier device, and the minority carriers do not accumulate in the drift region, thus, there is no reverse recovery effect at turn-off. The displacement current, which charges or discharges the junction capacitance of the diode, dominates the dynamic behavior in switching operations. The dynamic behavior of the diode is commonly evaluated for switching operations induced by commutation in a converter circuit. This test can apply a reverse voltage on the diode with a high $\mathrm{d}v/\mathrm{d}t$, but it is inconvenient for sweeping the test parameters to give the performance criteria. This paper evaluates the switching performance of SiC SBD for the half-wave rectification of a sinusoidal voltage with a non-inductive resistive load. Fig. 7(b) shows the experimental setup for evaluating the rectification performance of the SiC SBD. The function generator produces sinusoidal waveforms at the desired frequency and the high frequency bipolar amplifier boosts the output of the function generator. The SiC SBD, which is shown as the device under test (DUT), rectifies the sinusoidal voltage and supplies half-wave sinusoidal current to the non-inductive resistance load.

Fig. 9 gives the measured applied ac voltage $(V_{\rm ac})$, the terminal voltage of the SiC SBD $(V_{\rm d})$, and the device current $(I_{\rm d})$ in the experiment. Figs. 9(a)–(c) give the results of the half-wave rectification of a sinusoidal voltage at 100 kHz, 1 MHz, and 10 MHz, respectively. Fig. 9(a) shows that a small negative current flows at the instant when the applied ac voltage becomes negative, which results from carrier extraction while depleting the junction. This current corresponds to the displacement current that charges the junction capacitance. The reverse current continues to flow in accordance with the reverse bias voltage applied to the SiC SBD, but is negligible. However, the reverse

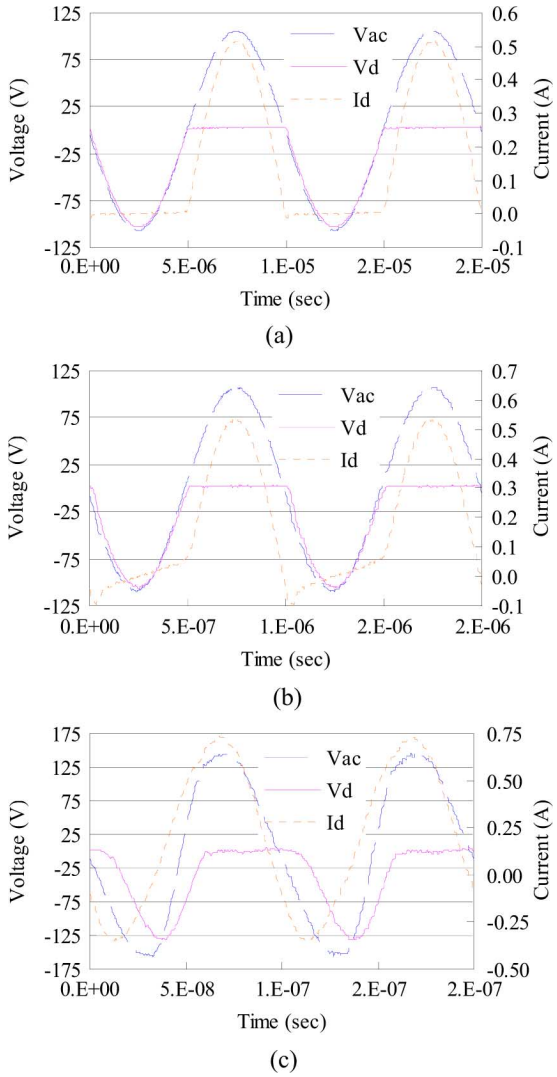

Fig. 9. Experimental result of high frequency ac rectification by SiC SBD. (a) 100 KHz, (b) 1 MHz, (c) 10 MHz.

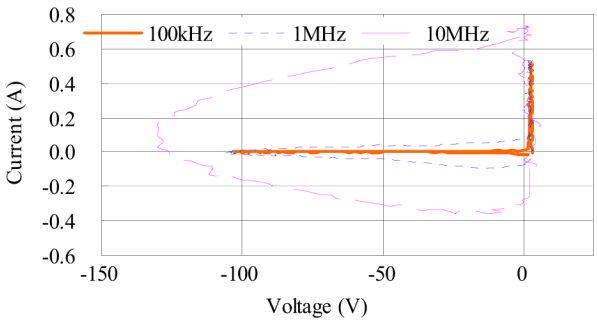

Fig. 10. Lissajeous plot as I-V characteristics for rectification operation of SiC SBD.

current becomes substantial to the increment of the applied ac frequency. Fig. 9(b) shows the result at 1 MHz. There is a significant reverse current flow for more than half the duration of the reverse voltage condition. Fig. 9(c) indicates that the displacement current flowing through the SiC SBD becomes significant in rectifying 10 MHz ac. Therefore, the use of SiC SBD is worthless as a rectifier in this condition.

Fig. 10 gives the I-V characteristics of the SiC SBD as a Lissajeous plot of the applied ac frequency. It shows that the I-V

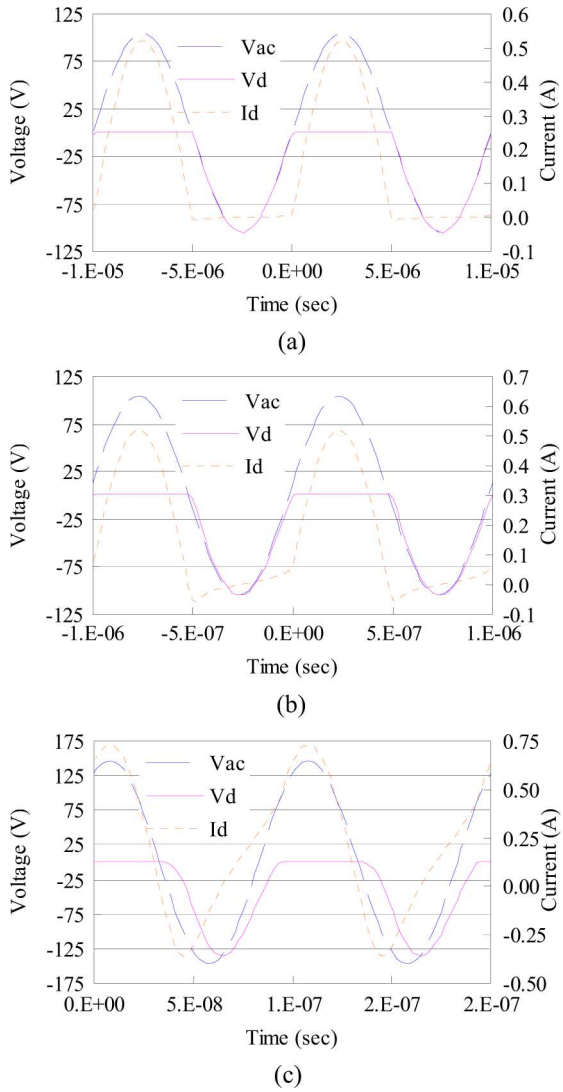

Fig. 11. Simulated result of high frequency ac rectification by SiC SBD model. (a) 100 KHz, (b) 1 MHz, (c) 10 MHz.

characteristics of the SiC SBD are almost ideal for a diode operating at 100 kHz, because the trajectory is close to the voltage and current axis. However, the I-V characteristics produce a round shape at higher frequency operations, due to the phase delay between the device current and terminal voltage induced by the capacitance. The looped area expands for higher frequencies.

These experimented results point to a criterion for using the SiC SBD as a rectifier.

C. Numerical Result of the SiC SBD Model in High Frequency Rectification

Fig. 11 shows the numerical results of the SiC SBD model for half-wave rectification of a high frequency ac voltage. As shown in Fig. 11(a), the diode current results from thermionic emission at the Schottky junction, and is dominant in the relatively low frequency condition of 100 kHz ac voltage, which is the same frequency as the ac signal used for C-V characterization. The SiC SBD model can suitably describe the behavior of the device with a voltage-controlled current source and a series resistance. The charging and discharging displacement currents of the junction capacitance account for a significant portion of rectification

of a high frequency ac voltage, as shown in Figs. 11(b) and (c). The proposed differential capacitance model reproduces the current drawn from the depletion process around the junction in the diode. The accuracy of the device current is evaluated by comparing the simulated results shown in Fig. 11, with the experimental results, shown in Fig. 9. The error in the numerical result increases as the frequency of the ac voltage becomes higher. This can be due to the model errors obtained while extracting the parameters of the C-V characteristic model (10). Another source of error stems from the relaxation-induced defects in a Schottky diode [20]. The differential capacitance of Schottky depletion region has a dependency on the reverse voltage and frequency, due to the combined characteristics of the Schottky depletion region and the carrier-depletion layer caused by the lattice-relaxation induced trap. The results in Figs. 9(c) and 11(c) were obtained at 10 MHz, whereas the parameter extraction took place at 100 kHz. Therefore, the frequency characteristics exert a significant influence on the dynamic performance of the SiC SBD for high frequency region. More accurate modeling of the SiC SBD, which can explain its characteristics at high frequencies, still needs to be worked on.

The voltage wave-form imposed on the diode becomes rectangular or trapezoidal in a switching converter circuit. Such a voltage waveform has a wide frequency spectrum and the high frequency component becomes higher as the $\mathrm{d}v/\mathrm{d}t$ of the imposed voltage increases. Therefore, the proposed model must be evaluated for its applicability to non-sinusoidal voltage waveforms—this will be carried out as a future work.

V. Performance Criterion of SiC SBD

The previous section evaluated the change in rectification behavior of an SiC SBD with the frequency of the applied ac voltage. A comparison between the numerical and experimented results validated the adequacy of the proposed model, which consists of an I-V dc model and a variable capacitance ac model. The results also indicated that the rectification properties of the SiC SBD were affected by the junction capacitance, especially at high frequency operations. This section discusses the performance criteria of the SiC SBD as a rectification device based on the developed model. The depletion of carriers around the junction of the SiC SBD induces capacitive characteristics of the device at the blocking condition. The amount of depleted charge varies with the applied voltage, and the displacement current appears to be the time derivative of the depleted charge. The charge/discharge current becomes significant as the frequency of the applied ac voltage increases, which augments $\mathrm{d}v/\mathrm{d}t$ in proportion to the ac frequency. Then, the SiC SBD rectification performance is expected to be evaluated by means of the relative amount of depleted charge to the diode's forward conduction current. However, the displacement current component originating from the depleted charge is superimposed on the thermionic emission current component to the measured terminal current at turn-on and turn-off. Therefore, it is necessary to discriminate and evaluate the displacement current component flowing through the variable capacitor at the junction. We define the rectification performance criteria as the relation between the total charge in the depletion region and the resultant charge from the thermionic emission current under forward-conduction conditions. In other words, the critical condition for the rectification of the SiC SBD can be defined by the relative amount of the depleted charge to the thermionic emission charge. The relationship of the total depleted charge to the reverse voltage is obtained from the width of the depletion region and the carrier concentrations, as shown in (9).

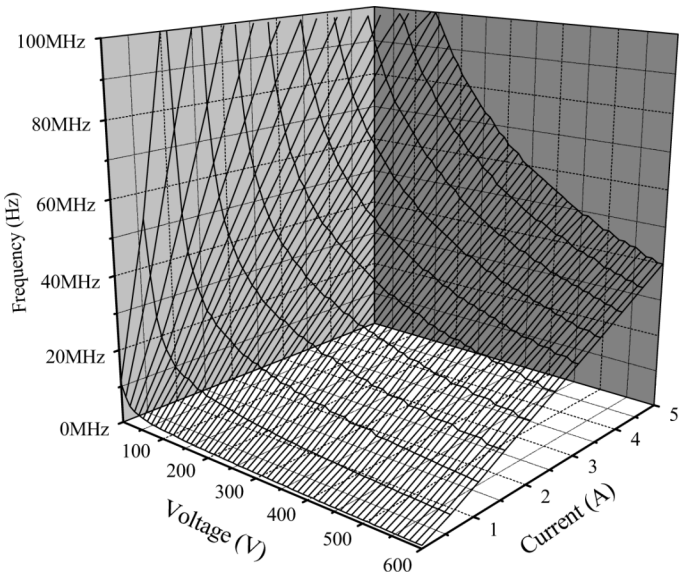

Fig. 12. Operational limit of high frequency rectification of SiC SBD.

The charge resulting from thermionic emission current can be approximated, as shown in (17), for half-wave rectification of sinusoidal ac voltage by considering the I-V characteristics of the SiC SBD to be ideal, and neglecting the internal resistance and the built-in potential.

$$Q_{\mathrm{peak}} = \int_0^{\pi} \frac{V \sin \omega t}{R} \mathrm{d}\omega t = \frac{2I}{\omega} \tag{17}$$

Here, V is the amplitude of the applied sinusoidal voltage, R is the non-inductive resistance load, ω is the angular frequency of the ac voltage, and $I = (V/R)$.

Therefore, the criteria of rectification performance is derived as in (18), when the charge equality condition is used.

The obtained criteria is plotted in Fig. 12 against the amplitude of the forward current I, ac voltage V, and its frequency. This shows that the SiC SBD maintains its rectification performance at high frequencies for a large forward current and low

$$\begin{cases} \frac{2I}{\omega} = \sqrt{2\varepsilon_{\mathrm{s}} e N_{\mathrm{d}} V} & 0 \le V \le V_{\mathrm{pt}} \\ \frac{2I}{\omega} = (N_{\mathrm{d}} - N_{\mathrm{b}}) e W_{\mathrm{d}} + \sqrt{(N_{\mathrm{b}} - N_{\mathrm{d}}) N_{\mathrm{b}} e^2 W_{\mathrm{d}}^2 + 2\varepsilon_{\mathrm{s}} e N_{\mathrm{b}} V} & V_{\mathrm{pt}} < V \le V_{\mathrm{bd}} \end{cases} \tag{18}$$

voltage conditions. However, it deteriorates as the forward current decreases and the voltage increases. This also shows that the punch-through structure does not influence the rectification performance, because the criterion curve change is negligible at the punch-through voltage. This criterion curve is useful in determining the appropriate device design for a given operating condition.

VI. Conclusion

SiC power devices are expected to operate at high switching frequencies by taking advantage of the superior characteristics of the SiC semiconductor material. SiC SBD is a majority carrier device, and is free from the minority carrier effect at the switching transient. The junction capacitance of an SiC SBD dominates the voltage and current dynamics at the switching transient. The junction capacitance of the device is represented by the differential capacitance of the depleted charge, relative to the variation of applied reverse bias voltage. The studied SiC SBD has a punch-through structure to improve the tradeoff between the breakdown voltage and series resistance. The C-V characteristics for a punch-through structure were modeled in this paper. The developed measurement system performed the C-V characterization over the rated voltage range of the SiC SBD, and the model parameters were extracted from the experimental results. The dynamic behavior during switching was tested experimentally, using a half-wave rectification circuit. Time-domain simulation results, obtained from the proposed SiC SBD model, agreed with the experimental results and validated the adequacy of the model. The rectification properties of SiC SBD were assessed for the proposed model. The criterion for operation of SiC SBD in rectification was established as a relationship among the ac voltage, current, and frequency. The proposed criterion is applicable in the design of power circuits with respect to the determined parameters and operating conditions.

Appendix
Derivation of Parameters in the Drift Layer

The relationship among the maximum depletion width, the breakdown voltage, and the impurity concentration in the drift layer are as follows for a non punch-through SBD [20]. The electric field becomes maximum at $x = 0$ in Fig. 1. Breakdown occurs when the maximum electric field reaches the critical value of the semiconductor material $E_{\rm c}$. Therefore, the maximum depletion width $W_{\rm d}$ and the breakdown voltage $V_{\rm bd}$ (maximum $V_{\rm ka}$) are given by (A1) for a non punch-through SBD structure.

$$\begin{cases} W_{\rm d} = \frac{\varepsilon_{\rm s}}{eN_{\rm d}} E_{\rm c} \\ V_{\rm bd} = \frac{eN_{\rm d}}{2\varepsilon_{\rm s}} W_{\rm d}^2 = \frac{\varepsilon_{\rm s}}{2eN_{\rm d}} E_{\rm c}^2 \end{cases} \tag{A1}$$

The impurity concentration $N_{\rm d}$ and the drift layer resistance $R_{\rm d}$ are expressed as a function of $V_{\rm bd}$ by (A2), assuming the drift layer width is equal to $W_{\rm d}$.

$$\begin{cases} N_{\rm d} = \frac{\varepsilon_{\rm s} E_{\rm c}^2}{2eV_{\rm bd}} \\ R_{\rm d} = \frac{W_{\rm d}}{\mu e N_{\rm d} A} = \frac{4V_{\rm bd}^2}{\mu \varepsilon_{\rm s} A E_{\rm c}^3} \end{cases} \tag{A2}$$

Here, μ: the mobility of the carrier.

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References

[1] B. Jayant Baliga, *Silicon Carbide Power Devices*. Singapore: World Scientific, 2006, pp. 15–33.
[2] J. L. Hudgins, G. S. Simin, E. Santi, and M. A. Khan, "An assessment of wide bandgap semiconductors for power devices," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 907–914, 2003.
[3] A. R. Hefner, R. Singh, J. Lai, D. Berning, S. Bouche, and C. Chapuy, "SiC power diodes provide breakthrough performance for a wide range of applications," *IEEE Trans. Power Electron.*, vol. 16, no. 2, pp. 273–280, 2001.
[4] B. Ozpineci and L. M. Tolbert, "Characterization of SiC Schottky diodes at different temperatures," *IEEE Power Electron. Lett.*, vol. 1, no. 2, pp. 54–57, 2003.
[5] Y. Jian, L. Zhenxian, and J. D. vanWyk, "High temperature embedded SiC chip module (ECM) for power electronics applications," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 392–398, 2007.
[6] T. Funaki, J. Balda, J. Junghans, A. Kashyap, A. Mantooth, F. Barlow, T. Kimoto, and T. Hikihara, "Power conversion with SiC devices at extremely high ambient temperatures," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1321–1329, 2007.
[7] T. Funaki *et al.*, "SiC JFET dc characteristics under extremely high ambient temperatures," *IEICE Electron. Express*, vol. 1, no. 17, pp. 523–527, 2004.
[8] T. Funaki *et al.*, "Switching characteristics of SiC JFET and Schottky diode in high-temperature dc-dc power converters," *IEICE Electron. Express*, vol. 2, no. 3, pp. 97–102, 2005.
[9] P. Shah, B. Geil, M. Ervin, T. Griffin, S. Bayne, K. Jones, and T. Oldham, "Advanced operational techniques and pn-pn-pn structures for high-power silicon carbide gate turn-off thyristors," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 1073–1079, 2002.
[10] Y. Gurbuz, W. P. Kang, J. L. Davidson, D. V. Kerns, and Q. Zhou, "PECVD diamond-based high performance power diodes," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 1–10, 2005.
[11] G. Spiazzi, S. Buso, M. Citron, M. Corradin, and R. Pierobeon, "Performance evaluation of a Schottky SiC power diode in a boost PFC application," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1249–1253, 2003.
[12] S. Inoue and H. Akagi, "A bidirectional isolated DC-DC converter as a core circuit of the next-generation medium-voltage power conversion system," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 535–542, 2007.
[13] T. R. McNutt, A. R. Hefner, H. A. Mantooth, J. Duliere, D. W. Berning, and R. Singh, "Silicon carbide PiN and merged PiN Schottky power diode models implemented in the Saber circuit simulator," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 573–581, 2004.
[14] T. McNutt, A. Hefner, A. Mantooth, D. Berning, and R. Sei-Hyung, "Silicon carbide power MOSFET model and parameter extraction sequence," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 353–363, 2007.
[15] A. M. Abou-Alfotouh, A. V. Radun, H. R. Chang, and C. Winterhalter, "A 1-MHz hard-switched silicon carbide DC-DC converter," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 880–889, 2006.
[16] L. Zhenxian, L. Bing Lu, J. D. van Wyk, and F. Lee, "Integrated CoolMOS FET/SiC-diode module for high performance power switching," *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 679–686, 2005.
[17] T. Nomura, M. Masuda, N. Ikeda, and S. Yoshida, "Switching characteristics of GaN HFETs in a half bridge package for high temperature applications," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 692–697, 2008.
[18] T. Funaki *et al.*, "Characterization of punch-through phenomenon in SiC-SBD by capacitance-voltage measurement at high reverse bias voltage," *IEICE Electron. Express*, vol. 3, no. 16, pp. 379–384, 2006.
[19] T. Funaki, T. Kimoto, and T. Hikihara, "Evaluation of capacitance-voltage characteristics for high voltage SiC-JFET," *IEICE Electron. Express*, vol. 4, no. 16, pp. 517–523, 2007.

[20] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981, p. 50, 195.
[21] Impedance Measurement Handbook, pp. 27–28, Jul. 2006, Agilent Technologies, AN-5950-3000.
[22] J. F. Chen, N. C. Chen, J. S. Wang, and Y. F. Chen, "Differential capacitance measurements of relaxation-induced defects in InGaAs/GaAs Schottky diodes," *IEEE Trans. Power Electron.*, vol. 48, no. 2, pp. 204–209, 2001.

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