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N_2O-grown oxides/4*H*-SiC (0001), (03$\bar{3}$8), and (11$\bar{2}$0) interface properties characterized by using *p*-type gate-controlled diodes

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The N_2O-grown $SiO_2/4H$-SiC (0001), (03$\bar{3}$8), and (11$\bar{2}$0) interface properties in *p*-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) have been characterized by using gate-controlled diodes. Although the inversion layer is not formed in simple SiC MOS capacitors at room temperature due to its large bandgap, a standard low frequency capacitance-voltage (*C-V*) curve can be obtained for the gate-controlled diodes, owing to the supply of minority carriers from the source region. From the quasistatic *C-V* curves measured by using gate-controlled diodes, the interface state density has been evaluated by an original method proposed in this study. The interface state density near the valence band edge evaluated by the method is the lowest at the oxides/4*H*-SiC (03$\bar{3}$8) interface. Comparison with the channel mobility is also discussed. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3028016]

The wide bandgap semiconductor silicon carbide (SiC) has superior properties such as high breakdown field, high thermal conductivity, and high saturation electron drift velocity.[1] 4*H*-SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) have been regarded as a candidate for high-power, high-temperature, and high-speed switches,[2] and several high-voltage 4*H*-SiC MOSFETs, which outperform Si power devices, have been already reported.[3–5]

In the last decade, the characteristics of SiC MOS devices have been significantly improved through the development of process technology. For example, the usage of 4*H*-SiC (03$\bar{3}$8)[6] and (11$\bar{2}$0) faces[7] and the utilization of deposited insulators[8–10] are effective to improve the characteristics of SiC *n*-channel MOSFETs. In addition, the nitridation of gate oxides[11–13] is widely adopted to reduce the interface state density near the conduction band edge, leading to high channel mobility in SiC *n*-channel MOS devices.[14] Although the understanding on *n*-channel MOS devices has shown gradual progress, the fundamental study on SiC *p*-channel MOS devices has been lacking. The understanding on SiC MOS interface properties in the lower half of bandgap can contribute to the improvement of SiC power devices and circuits.

Although several groups have reported the *p*-channel MOSFETs on the 4*H*-SiC (0001) face,[15–17] the crystal face dependences of the interface state density and channel mobility have been still missing. The authors characterized the N_2O-grown oxides/4*H*-SiC (0001), (03$\bar{3}$8), and (11$\bar{2}$0) interface properties by using MOSFET structure, called a gate-controlled diode.[18] In the gate-controlled diodes, the capacitance-voltage (*C-V*) characteristics were measured between the gate electrode and other electrodes (source, drain, and substrate electrodes) of the MOSFETs. The measured low-frequency *C-V* curves demonstrate not "accumulation-depletion-deep depletion" characteristics but "accumulation-depletion-inversion" characteristics in contrast to the simple SiC MOS capacitors because the source/drain regions act as an external source of holes. By using gate-controlled diodes, the correlation between channel mobility and shallow interface state density has been demonstrated for *n*-channel SiC (0001) MOSFETs.[19] In this study, the authors propose an original method to estimate the interface state density, and the shallow states in the lower half of the bandgap at the SiO_2/SiC interface are evaluated from the measured *C-V* curves obtained by using the gate-controlled diodes.

The *p*-channel MOSFETs were fabricated on *n*-type 4*H*-SiC 8° off-axis (0001), on-axis (03$\bar{3}$8), and on-axis (11$\bar{2}$0) epilayers. The donor concentration of the *n*-type epilayers was 1×10^{16}, 5×10^{16}, and 5×10^{14} cm^{-3} for (0001), (03$\bar{3}$8), and (11$\bar{2}$0) faces, respectively. The 0.3 μm deep source/drain regions were formed by high-dose Al^+ implantation (energy: 10–160 keV; total dose: 5×10^{15} cm^{-2}) at 300 °C. After ion implantation, thermal annealing was carried out at 1700 °C for 20 min with a carbon cap to suppress surface roughening.[20] Thermal oxidation was performed in dry N_2O ambient (10% diluted in N_2) at 1300 °C.[13,21] The thickness of gate oxides was 49, 44, and 52 nm for (0001), (03$\bar{3}$8), and (11$\bar{2}$0) faces, respectively. The source/drain and substrate electrodes were Ti/Al/Ni and Ni, respectively, and these electrodes were annealed at 950 °C for 5 min. The gate electrode was Al. The typical channel length (*L*) and width (*W*) were 100 and 200 μm, respectively. The design of long-channel MOSFETs was adopted to minimize the influence of source/drain contact resistance and to suppress short-channel effects.[22] The field-effect mobility of the *p*-channel MOSFETs fabricated on (0001), (03$\bar{3}$8), and (11$\bar{2}$0) faces was 7, 11, and 17 cm^2/V s, respectively (not shown). The *p*-channel SiC MOSFETs on the (03$\bar{3}$8) and (11$\bar{2}$0) faces exhibit higher channel mobility than that on the (0001) face as is the case for *n*-channel SiC MOSFETs.[6,7]

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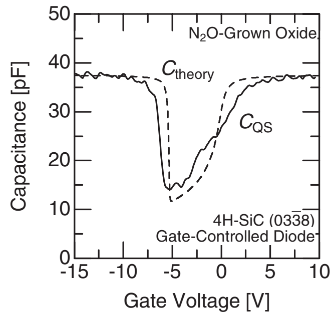

FIG. 1. Quasistatic *C-V* curve obtained in *p*-channel MOSFETs on the 4*H*-SiC $(03\bar{3}8)$ face by using a gate-controlled diode. A theoretical *C-V* curve is also shown by a dashed line.

Quasistatic *C-V* characteristics (C_{QS}) were measured at room temperature under dark condition by using the gate-controlled diodes to evaluate the interface state density. The typical sweep rate for the *C-V* measurements was about 0.15 V/s. The area of gate electrode is about 4.9×10^{-4} cm^2. Figure 1 shows the quasitatic *C-V* curve obtained from the $(03\bar{3}8)$ MOSFETs and theoretical low-frequency *C-V* curve. The measured *C-V* characteristics indicate that the MOS interface under the gate electrode shows strong inversion at sufficiently negative gate voltage, owing to the supply of minority carriers (holes) from the source region. From the measured *C-V* curves, the authors evaluated the interface state density near the valence band edge. At first, the surface potential (Ψ_S)-gate voltage (V_G) characteristics were calculated by using the following equation:[23]

$$\Psi_S(V_{G2}) = \int_{V_{G1}}^{V_{G2}} \left[1 - \frac{C_{QS}(V_G)}{C_{ox}}\right] dV_G + \Psi_S(V_{G1}). \tag{1}$$

In Eq. (1), in order to determine the absolute value of surface potential, the basis of surface potential must be defined. In this study, the authors assumed that the surface potential calculated from the measured *C-V* characteristics coincides with that theoretically obtained at a gate voltage of −15 V. Then, the Ψ_S-V_G characteristics experimentally obtained are compared with the theoretical Ψ_S-V_G relationship.

Figures 2(a)–2(c) show the Ψ_S-V_G curves experimentally and theoretically obtained for the (0001), $(03\bar{3}8)$, and $(11\bar{2}0)$ gate-controlled diodes, respectively. Compared with the theoretical curves, the shift in experimental Ψ_S-V_G curves toward the negative gate voltage direction is caused by the presence of effective fixed charge (positive) located at the SiO_2/SiC interface and the stretch out of Ψ_S-V_G curves by the presence of interface states. In the ideal case (theoretical Ψ_S-V_G curve), the change in gate voltage directly causes that of the surface potential. On the other hand, in the case of the experimental Ψ_S-V_G curves, the additional increment in gate voltage is needed in order to fill the interface states with holes. Thus, the interface state density (D_{it}) can be evaluated from the difference between the slope of Ψ_S-V_G characteristics theoretically and experimentally obtained as described in the following equation:

$$D_{it} = \frac{C_{ox}}{q}\left(\left.\frac{dV_G}{d\Psi_S}\right|_{theory} - \left.\frac{dV_G}{d\Psi_S}\right|_{experiment} \right). \tag{2}$$

From this equation, the interface state density near the valence band edge in the *p*-channel SiC MOSFETs was calculated. This method can be also used to estimate the interface state density near the conduction band edge in the *n*-channel MOSFETs.

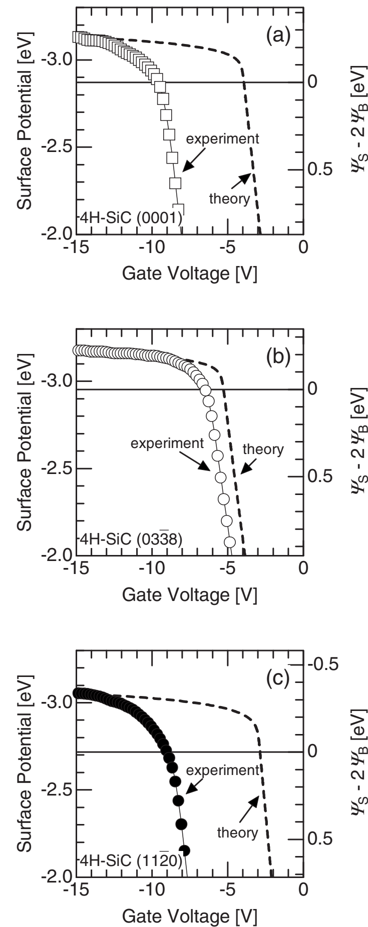

FIG. 2. Ψ_S-V_G characteristics of the fabricated MOSFETs on (a) (0001), (b) $(03\bar{3}8)$, and (c) $(11\bar{2}0)$ faces. Open squares in (a), open circles in (b), and closed circles in (c) mean the Ψ_S-V_G characteristics experimentally obtained. Dashed line means the theoretical Ψ_S-V_G curve. The right vertical axis denotes the $\Psi_S-2\Psi_B$ and the solid line represents the $\Psi_S=2\Psi_B$ (onset of strong inversion).

Figure 3 shows the distributions of the interface state density near the valence band edge in the (0001), $(03\bar{3}8)$, and $(11\bar{2}0)$ MOSFETs. From Fig. 3, the interface state density is exponentially increased toward the valence band edge and reaches 2×10^{12} cm^{-2} eV^{-1} at E_V+0.2 eV for the (0001) interface. On the other hand, the $(03\bar{3}8)$ face shows a lower interface state density of 1×10^{12} cm^{-2} eV^{-1} at 0.2 eV above

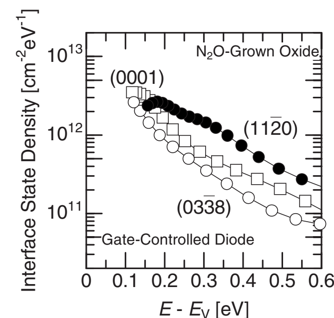

FIG. 3. Distribution of interface state density on the 4*H*-SiC (0001) face (open squares), $(03\bar{3}8)$ face (open circles), and $(11\bar{2}0)$ face (closed circles). The interface state density was estimated by *C-V* curves measured by using the gate-controlled diode structure.

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the valence band edge. Contrary to expectations, the $(11\bar{2}0)$ face exhibits higher interface state density than the $(03\bar{3}8)$ face, and the interface state density is 2×10^{12} $cm^{-2}\,eV^{-1}$ at E_V+0.2 eV. Compared with the $SiO_2/4H$-SiC (0001) interface, the interface state density at the $SiO_2/4H$-SiC $(11\bar{2}0)$ interface is high in the deep energy region and relatively low in the shallow energy region from the valence band edge.

The gate voltage at which the MOS interface becomes strong inversion can be obtained from the intersection of Ψ_S-V_G curve and $\Psi_S=2\Psi_B$ line (horizontal solid line in Fig. 2). The effective fixed charge at the MOS interface was calculated from the difference between the theoretical and experimental gate voltage at which the MOS interface becomes strong inversion. A highest effective fixed charge (positive) of 3.0×10^{12} cm^{-2} was obtained for the $(11\bar{2}0)$ face, and the effective fixed charge was lowest at the $(03\bar{3}8)$ interface (4.6×10^{11} cm^{-2}). The effective fixed charge at the (0001) interface was 2.5×10^{12} cm^{-2}. The magnitude of the effective fixed charge is consistent with that of the interface state density in the deep energy region from the valence band edge as shown in Fig. 3. The high effective fixed charge at the $(11\bar{2}0)$ interface may be mainly due to the high density of interface state in the deep energy region.

The N_2O-grown oxide/4*H*-SiC $(03\bar{3}8)$ interface exhibits the lowest interface state density, leading to the high channel mobility in the $(03\bar{3}8)$ MOSFETs. Although the N_2O-grown oxides/4*H*-SiC $(11\bar{2}0)$ interface shows high interface state density in the deep energy region, the *p*-channel MOSFETs on 4*H*-SiC $(11\bar{2}0)$ face exhibit high channel mobility as described above. The main reason for the high channel mobility in the $(11\bar{2}0)$ MOSFETs may be the low donor concentration ($N_D=5\times10^{14}$ cm^{-3}) of the employed epilayers. The channel mobility of MOSFETs generally depends on the doping concentration of epilayers.[21,24] The decrease in donor concentration results in an increase in channel mobility because the influence of surface roughness scattering and Coulomb scattering from the charges located near the interface is weakened due to its low vertical electric field in the inversion layer. Although the high effective fixed charge density was observed in the $(11\bar{2}0)$ MOSFETs as mentioned above, the charges hardly affected the channel mobility of the MOSFETs due to small effect of Coulomb scattering. The low donor concentration contributes to the high channel mobility in the $(11\bar{2}0)$ MOSFETs. In addition, the $SiO_2/4H$-SiC $(11\bar{2}0)$ interface shows the relatively low interface state density near the valence band edge. In the case of 4*H*-SiC *n*-channel MOSFETs, the interface state density near the conduction band edge adversely affects the channel mobility due to severe electron trapping.[14] In a similar way, the channel mobility of *p*-channel MOSFETs fabricated on the (0001) face may be severely influenced by the shallow interface states, which cause hole trapping. This relatively low density of interface states also contributes to the increase in channel mobility in $(11\bar{2}0)$ face.

In conclusion, the authors have investigated the correlation between the characteristics of *p*-channel 4*H*-SiC MOSFETs with N_2O-grown oxides and their interface properties. The fabricated *p*-channel MOSFETs exhibited a channel mobility of 7 $cm^2/V\,s$ for the (0001) face, 11 $cm^2/V\,s$ for the $(03\bar{3}8)$ face, and 17 $cm^2/V\,s$ for the $(11\bar{2}0)$ face. The shallow interface state density was estimated from the Ψ_S-V_G characteristics calculated by using the quasistatic and theoretical low-frequency *C*-*V* curves of the gate-controlled diodes. The $SiO_2/4H$-SiC $(03\bar{3}8)$ interface exhibited the lowest interface state density ($D_{it}=1\times10^{12}$ $cm^{-2}\,eV^{-1}$ at E_V +0.2 eV). The high channel mobility in the $(11\bar{2}0)$ MOSFETs may be attributed to the low doping concentration in *n*-type epilayer and relatively low interface state density near the valence band edge. The usage of the nonbasal faces and the nitridation of gate oxides are attractive methods to enhance the characteristics of both 4*H*-SiC *p*-channel and *n*-channel MOS-based devices.

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[1]H. Matsunami and T. Kimoto, Mater. Sci. Eng., R. **20**, 125 (1997).
[2]J. A. Cooper, Jr., M. R. Melloch, R. Singh, A. Agarwal, and J. W. Palmour, IEEE Trans. Electron Devices **49**, 658 (2002).
[3]D. Peters, R. Schörner, P. Friedrichs, and D. Stephani, Mater. Sci. Forum **433–436**, 769 (2003).
[4]M. Matin, A. Saha, and J. A. Cooper, IEEE Trans. Electron Devices **51**, 1721 (2004).
[5]M. Noborio, J. Suda, and T. Kimoto, IEEE Trans. Electron Devices **54**, 1216 (2007).
[6]T. Hirao, H. Yano, T. Kimoto, H. Matsunami, and H. Shiomi, Mater. Sci. Forum **389–393**, 1065 (2002).
[7]H. Yano, T. Hirao, T. Kimoto, H. Matsunami, K. Asano, and Y. Sugawara, IEEE Electron Device Lett. **20**, 611 (1999).
[8]T. Kimoto, H. Kawano, M. Noborio, J. Suda, and H. Matsunami, Mater. Sci. Forum **527–529**, 987 (2006).
[9]S. Hino, T. Hatayama, J. Kato, E. Tokumitsu, N. Miura, and T. Oomori, Appl. Phys. Lett. **92**, 183503 (2008).
[10]M. Noborio, J. Suda, and T. Kimoto, IEEE Trans. Electron Devices **55**, 2054 (2008).
[11]P. Jamet, S. Dimitrijev, and P. Tanner, J. Appl. Phys. **90**, 5058 (2001).
[12]G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, R. A. Weller, S. T. Pantelides, L. C. Feldman, O. W. Holland, M. K. Das, and J. W. Palmour, IEEE Electron Device Lett. **22**, 176 (2001).
[13]L. A. Lipkin, M. K. Das, and J. W. Palmour, Mater. Sci. Forum **389–393**, 985 (2002).
[14]N. S. Saks, *Silicon Carbide – Recent Major Advances*, edited by W. J. Choyke, H. Matsunami, and G. Pensl (Springer, Berlin, 2003) 387.
[15]J. S. Han, K. Y. Cheong, S. Dimitrijev, M. Laube, and G. Pensl, Mater. Sci. Forum **457–460**, 1401 (2004).
[16]M. Okamoto, M. Tanaka, T. Yatsuo, and K. Fukuda, Appl. Phys. Lett. **89**, 023502 (2006).
[17]M. K. Das, S. K. Haney, C. Jonas, and Q. Zhang, Mater. Sci. Forum **556–557**, 667 (2007).
[18]A. S. Grove and D. J. Fitzgerald, Solid-State Electron. **9**, 783 (1966).
[19]S. Suzuki, S. Harada, R. Kosugi, J. Senzaki, W. Cho, and K. Fukuda, J. Appl. Phys. **92**, 6230 (2002).
[20]Y. Negoro, K. Katsumoto, T. Kimoto, and H. Matsunami, J. Appl. Phys. **96**, 224 (2004).
[21]T. Kimoto, Y. Kanzaki, M. Noborio, H. Kawano, and H. Matsunami, Jpn. J. Appl. Phys., Part 1 **44**, 1213 (2005).
[22]M. Noborio, Y. Kanzaki, J. Suda, and T. Kimoto, IEEE Trans. Electron Devices **52**, 1954 (2005).
[23]C. N. Berglund, IEEE Trans. Electron Devices **13**, 701 (1966).
[24]S. Takagi, A. Toriumi, M. Iwase, and H. Tango, IEEE Trans. Electron Devices **41**, 2357 (1994).

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