Conductance of Si nanowires formed by breaking Si-Si junctions

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We have fabricated Si nanowires (NWs) by breaking Si-Si tip-sample junctions and studied their conductance for both *p-n* and *p-p*-type junctions at room temperature. Upon breaking the junction by retracting the Si tip from the Si clean surface, the conductance decreases by orders of magnitude from $\sim 1G_0$ to $\sim 10^{-6}G_0$, where G_0 is the quantum unit of conductance. The conductance histogram plotted against $\log(G/G_0)$ reveals peaklike structures for $G > 10^{-3}G_0$, but becomes featureless for $10^{-6}G_0 < G < 10^{-3}G_0$. In this low-conductance region, the histogram shows strong dependence on bias polarity and doping; the *p*-type-tip-*n*-type-sample junctions under positive sample biases yield large intensity in the histogram, while the same junctions under the opposite bias polarity and the *p-p* junctions under both bias polarities show small intensity below $10^{-4}G_0$. This observation suggests that longer and thinner Si NWs can be preferably formed in the reversely biased *p-n* Si junctions. We also investigated how the conductance of Si NWs varies with the tip displacement ΔL and found a quadratic dependence of $\log(G/G_0)$ on ΔL, suggesting the localization of carriers in disordered Si NWs. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2812563]

I. INTRODUCTION

Si nanowires (NWs) are potential material for applications in nanoscale electronics, and their formation and characterization have been a subject of intensive and experimental investigations in the past decade. Single-crystalline Si NWs of 20–50 nm in diameter have been well studied and already incorporated as building blocks into various types of homo- and hetero-Si nanodevices.[1] These Si NWs show resistance (0.1–1) MΩ after annealing.[2] Smaller-diameter Si NWs with diameters less than 10 nm have also been synthesized by various methods, e.g., oxide assisted growth,[3,4] oxidation thinning,[5,6] in addition to the catalytic growth from Au nanoparticles.[7] These methods yield different Si NWs showing a variety of transport properties, from ballistic conduction[5] to Coulomb blockade.[6] Theoretical calculations usually predict high conductance for Si NWs of various atomic arrangements, though their electronic transport sensitively depends on surface conditions, e.g., reconstruction,[8] passivation,[9] disorder,[10,11] and roughness.[12] The single-atom chain of Si, the smallest of Si NWs, is predicted to be metallic, and its conductance becomes $(2-3)G_0$ depending on the chain length.[13] However, the conductance of real Si NWs rarely achieves predicted high values, except in the case of nearly perfect Si NWs, which behave as a coherent single quantum dot.[14] More accumulation of experimental results is clearly needed for understanding the electron transport through thin Si NWs.

For metals and alloys, the break junction method has been successfully employed for producing atom-sized NWs and characterizing their transport properties.[15] In this method, two macroscopic electrodes are first brought into contact and then separated. The contact point makes a necking deformation, becomes thinner, and eventually evolves into a NW in the final stage of the junction break. Since the break junction method critically depends on the junction deformation, it had been rarely applied to brittle materials like Si, except for a couple of experiments using scanning tunneling microscopy (STM).[16] Recently, however, Arai and Tomitori,[17] and Kizuka *et al.*[18] have successfully produced Si NWs by breaking atomic force microscopy (AFM) tip-sample junctions. They employed a conductive Si AFM tip and brought it to contact with a Si surface kept at high or room temperatures. By slowly retracting the tip from the surface, a Si NW of a few nanometers wide can be formed between the tip and the sample. Kizuka *et al.* carried out detailed *in situ* transmission electron microscopy (TEM) observations of Si NWs, and simultaneously measured the force and the contact current during the NW evolution. They found that the conductance becomes $\sim 0.01G_0$ for ~3 nm diameter Si NWs.

The experiments by Kizuka *et al.* clearly demonstrate that the Si-Si break junction method can yield Si NWs even at room temperature. Encouraged by these previous experi-

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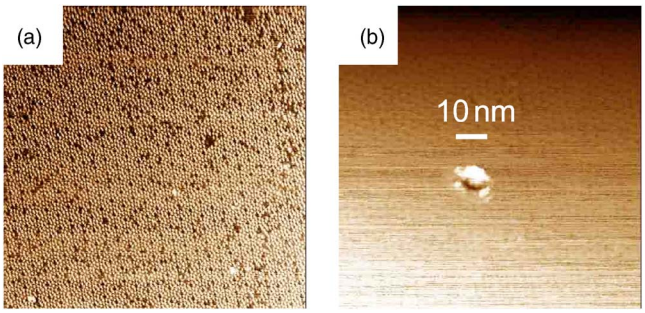

FIG. 1. (Color online) (a) STM image of the Si(111) surface acquired with a Si tip. (b) A contact footprint formed on a *p*-type Si(111) by a Si tip. The contact was made at 2 V and ~10 nA, i.e., at $\sim 6.5\times 10^{-5}G_0$ in conductance. Before making this footprint, the tip was used for the conductance measurements and subject to touching the surface several times. Therefore, the crater roughly indicates the average initial size of the NWs formed between the Si tip and the Si(111) surface.

ments, we have employed in this work a STM-type tip-sample break junction for producing Si NWs at room temperature in ultrahigh vacuum (UHV). We have extended the conductance measurements down to the $10^{-6}G_0$ region and investigated how the conductance of Si NWs changes with the bias, the tip and sample doping, and the junction stretching.

II. EXPERIMENT

Si tips were prepared from Si rods [0.28 mm $\times$(0.2–0.4) mm$\times$(10–15) mm], cut from a highly doped *p*-type Si wafer ($\leq$0.02 Ω cm). One end of the rod was chemically polished to form a sharply pointed tip. The etching solution is a 3:4 mixture of 40% HF and concentrated HNO_3, with and without additional CH_3COOH which controls the etching speed. The tip axis is along the [100] direction. The tip apex has a radius of ~100 nm but becomes strongly faceted with four (100) planes to form a quadrangular pyramid. The polished Si tip was inserted into a thin-wall Pt tube, which was then placed into a STM tip holder. The tip was clamp-fixed by gently crashing the Pt tube from the side with two set screws of the holder. The Pt-Si contact thus formed revealed ohmic behavior and showed negligible resistance compared to that of Si NWs.

The STM used in this work is a commercial UHV STM (UNISOKU USM-1200). Each tip was first cleaned in UHV by electron-beam heating, which occasionally resulted in slight blunting of the tip apex. Nevertheless, we could still routinely observe Si surface steps, and sometimes surface atoms, with the cleaned Si tips as shown in Fig. 1(a). Samples used in this experiment are highly doped *n*- and *p*-type Si(111) substrates, with resistivity of $\leq$0.02 and $\leq$0.02 Ω cm, respectively. Their surfaces were cleaned by high-temperature annealing and flushing in UHV.

The tip was first manually brought into contact with the surface until the conductance becomes higher than $\sim 3G_0$, to make sure that no substantial resistance appears at the tip-sample junction. After retracting the tip, the make-break cycle of the tip-sample junction was repeated by applying a triangular driving voltage to the *z*-piezo of the tip. The approaching and retracting speeds of the tip were the same and varied between 78, 36.7, and 7.3 nm/s. We typically carried out the NW formation at a couple of surface points and, at each point, repeated the make-break cycle of the tip-sample junction a few times. We obtained ~(10–20) data in total on the junction conductance per one experiment. All measurements were made at room temperature in UHV.

We monitored changes in the junction conductance during the tip retraction and, in some cases, also recorded the conductance during the tip approaching. The bias was applied to the sample and varied from −5 to +5 V. We found that the conductance varies over a wide range from a couple of G_0 to $\sim 10^{-6}G_0$ during the junction break. Since our current amplifier with a fixed gain could not cover the entire conductance range, we had to perform separate experiments with the different amplifier gain for high and low-conductance regions, $G \geq 10^{-3}G_0$ and $10^{-2}G_0 \geq G \geq 10^{-6}G_0$, respectively. The experimental results obtained in these conductance regions are thus separately presented and discussed in Secs. III B and III C, respectively.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Contact footprints

For obtaining rough estimation of the tip-sample junction size, we carried out a single tip-sample contact with a fresh tip and imaged a contact footprint left on the surface. The observed STM images showed that the size of the footprint always remains ~10 nm, even when the conductance increases from $0.65G_0$ to $2.3G_0$. Since the first tip-sample contact was made at $\gtrsim 6.5G_0$, the initial junction size before the tip retraction is likely around 10 nm in diameter. Note that a similar junction size (~5 nm) has been reported for the W-tip-Si-sample junction at $\sim 0.01G_0$.[19]

Since the same tip was repeatedly used for making ~(10–20) junction breaks, the initial size of each junction would vary and not stay the same as that of the first tip-sample contact mentioned above. Unfortunately, the "used" Si tips usually yielded no stable STM images, so we could not directly estimate the junction size. On rare occasions, however, we could image the contact footprints with the used Si tip and obtain the size-conductance relationship. Figure 1(b) shows a footprint which was formed by pressing the used tip onto the surface until the conductance reaches $\sim 6.5\times 10^{-5}G_0$. As can be seen in the image, a crater of ~5 nm in diameter is formed by the tip touching. For this tip, the crater size increases to ~20 nm at $2\times 10^{-4}G_0$. This result suggests that the Si NWs showing the conductance $(10^{-3}-10^{-5})G_0$, which will be discussed in Sec. III C, would be a few to a few tens of nanometers in diameter, depending on their conductance. The observations with the used tip also indicate that, at the same contact size, the used tip yields significantly lower conductance than the fresh tip. This reduction in the conductance would be the result of the junction disordering, which will be discussed in Sec. III D.

B. High-conductance region

Figures 2(a)–2(c) show typical conductance traces observed when we made and broke the Si-Si tip-sample junctions. The sample is an *n*-type Si(111) surface biased at

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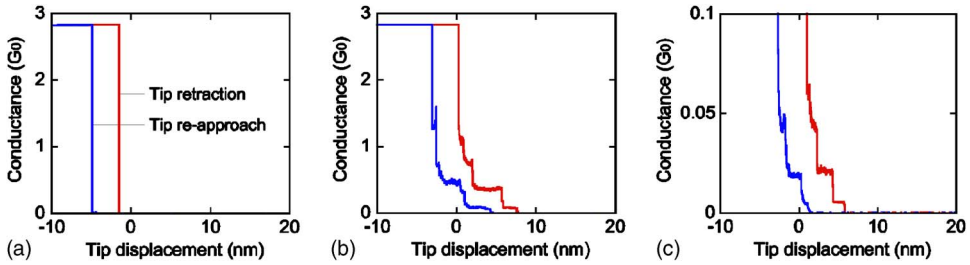

FIG. 2. (Color online) Examples of transient conductance trace observed in the high-conductance region $G > 10^{-3}G_0$. Two traces in each panel represent the conductance recorded during the tip retraction and the reapproach, respectively. In many cases, the conductance simply jumps down and up, as shown in (a), but occasionally exhibits a couple of plateaus, mostly in the subquantum range as shown in (b) and (c). The plateaus are nearly reproducible in the retraction and the reapproach traces.

+1.6 V, and the tip speed is 78 nm/s. In each panel, two traces represent the conductance recorded for the tip retraction and the reapproach, respectively. Note that a different conductance scale is used in Fig. 2(c), where the conductance traces are displayed for $G \geq 0.1G_0$. The zero of the tip displacement in each panel is arbitrary chosen and of little physical significance. In Figs. 2(a) and 2(b), the flat part of the traces is due to the saturation of the current amplifier. In most cases, the conductance traces are like those shown in Fig. 2(a) and simply jump down and up between upper and lower limits of the measurement, without revealing any distinct features. Occasionally, however, the trace shows a couple of short plateaus as seen in Fig. 2(b). In Fig. 2(c), the plateaus appear even below $0.1G_0$. An interesting observation on these plateaus is that they are nearly reproducible. In Figs. 2(b) and 2(c), each plateau in the retraction trace reappears at nearly the same position in the reapproach trace, though with the different plateau length. This observation implies reversibility in the deformation of the Si NWs even after their failure. Such reversible conductance traces are often observed on atom-sized contacts of metals at cryogenic temperatures,[20] where the conductance varies with the reversible displacement of one or two contact atoms. It is, however, unexpected for Si NWs at room temperature, where the conductance depends on the irreversible necking deformations of Si NWs. Direct TEM observations by Kizuka *et al.*[18] revealed a couple of twin boundaries within Si NWs. The reversible twinning of nano-sized grains might thus be a possibility, but we cannot conclude at this time on the deformation mechanism(s) responsible for the reproducible plateaus shown in Figs. 2(b) and 2(c).

In metal NWs, the conductance plateaus tend to appear at specific conductance values and produce well-defined peaks in the conductance histogram. For most metals, the first peak locates at $\sim(1-1.5)G_0$. It is generally considered that these peaks in the conductance histogram correspond to certain preferred geometries of metal NWs.[15] On the other hand, the majority of the conductance plateaus of Si NWs appears below $1G_0$, and their positions are widely distributed from $\sim 0.01G_0$ to $\sim 1G_0$. As a result, the plateaus of Si NWs produce no clear peaklike features in the conductance histogram. To properly represent the wide conductance distribution, we replotted the histogram against $\log(G/G_0)$ instead of G/G_0. The result is shown in Fig. 3. Two histograms are for the *n*-type and *p*-type samples, or the *p-n* and *p-p* junctions, respectively, since our Si tips are *p*-type. The sample bias is +2 V. We used 174 and 80 traces (both the retraction and reapproach traces are included) for the *p-n* and *p-p* histograms, respectively. To compensate this difference in the data size, the bin height for each histogram is normalized by the number of total traces. In the logarithmic conductance scale, both histograms now reveal a few peak features, though the peaks in the *p-p* histogram are less clear due to the small data size. Except for a peak around $\log(G/G_0) \sim -1.2$, other peaks appear at nearly the same positions in two histograms. It is thus likely that these peaks are genuine peaks and, like the conductance peaks of metal NWs, correspond to certain preferred geometries of Si NWs. At this time, however, we have no other information on these preferred Si NWs, and their structures are yet unclear. As mentioned in Sec. I, theoretical models do not predict subquantum conductance and give no clues to the peaks in Fig. 3. The emergence of the peak structures in the logarithmic conductance scale implies that not G/G_0 but $\log(G/G_0)$ is relevant to the Si NW geometry. This point will be discussed in Sec. III D.

C. Low-conductance region

To explore the lower conductance region below $10^{-3}G_0$, we carried out another set of measurements with increasing the current amplifier sensitivity to 10^7 V/A. A conductance trace shown in Fig. 4 displays a typical result observed in the

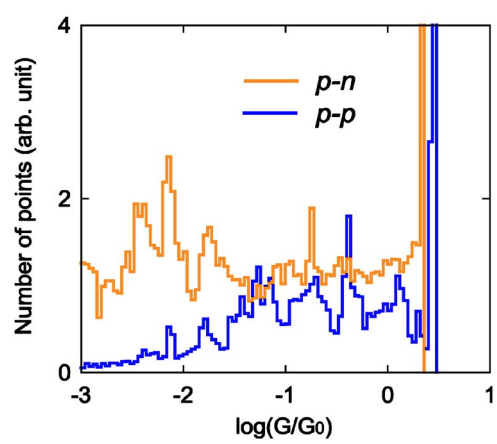

FIG. 3. (Color online) The *p-n* and the *p-p* conductance histograms at +2 V in the high-conductance region $G > 10^{-3}G_0$. The histograms are plotted against $\log(G/G_0)$ to cover the wide distribution of the junction conductance. A few peaklike features are commonly observed in two histograms.

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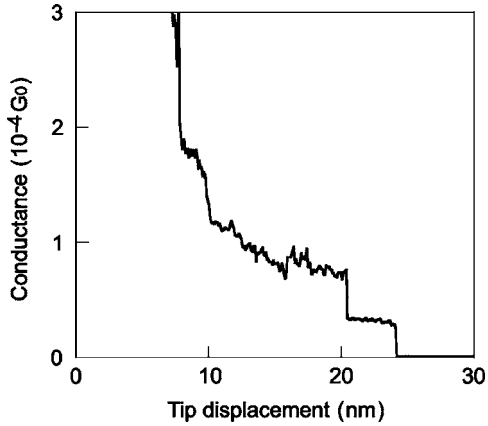

FIG. 4. An example of transient conductance trace observed on the *p-p* junction and in the low-conductance region $G < 10^{-3}G_0$. This trace shows a well-defined plateau in the $10^{-5}G_0$ range.

$10^{-4}G_0$ region. In this example, a well-defined plateau can be seen at $\sim 4 \times 10^{-5}G_0$, and similar plateaus were occasionally observed in other traces. As in the case of the high-conductance plateaus, these plateaus are also likely to correspond to certain preferred geometries of Si NWs, but of smaller size. Different from the high-conductance plateaus, however, the plateaus below $10^{-3}G_0$ produce no peaklike features in the histogram, even plotted in the logarithmic conductance scale. In Fig. 5, we summarize low-conductance histograms obtained on the *p-n* and *p-p* junctions under sample biases from −5 to +5 V. As in Fig. 3, the histograms are plotted against $\log(G/G_0)$. Only the retraction traces were recorded, and the number of traces used for each histogram is 40 for Figs. 5(a) and 5(b), and 10 for Figs. 5(c) and 5(d), respectively. To compensate this difference in data size, the vertical scales of the *p-n* and *p-p* histograms are adjusted

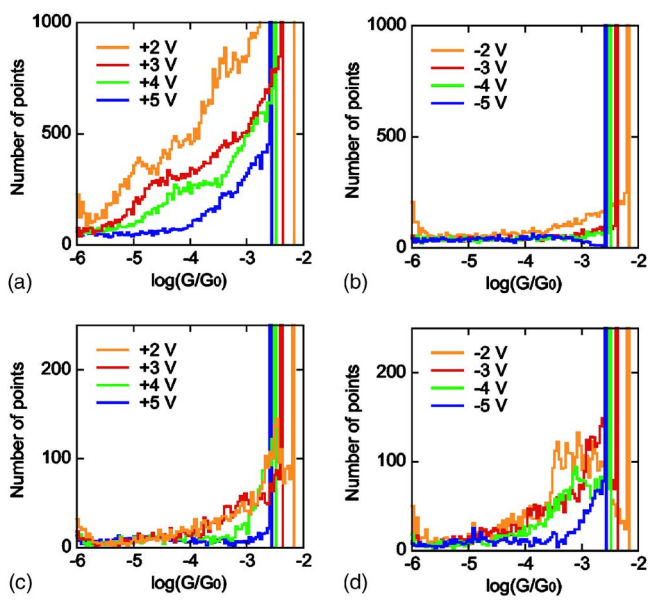

FIG. 5. (Color online) Conductance histograms in the low-conductance region $G < 10^{-3}G_0$ obtained under different sample biases. Histograms (a), (b) and (c), (d) are for the *p-n* and the *p-p* junctions, respectively. The vertical axis in each panel is appropriately scaled so that we can directly compare the intensity of each plot. The *p-n* histogram in (a) under positive biases shows appreciable intensity at low biases.

so that the intensity of each histogram can be directly compared. It is first noted that neither *p-n* nor *p-p* histograms show clear peaklike features below $10^{-3}G_0$, though some obscure ups and downs can be observed in the histograms at ±2 V. This result suggests that the low-conductance plateaus such as the one shown in Fig. 4 is not narrowly distributed in their position, even in a logarithmic conductance scale, and would thus not be specific to some preferred Si NWs.

Another interesting observation in Fig. 5 is the strong bias polarity dependence of the *p-n* histogram. Under positive sample biases, the *p-n* histogram in Fig. 5(a) shows appreciable intensity down to $10^{-6}G_0$, whereas the histograms in Fig. 5(b), obtained under negative sample biases, nearly vanish below $10^{-3}G_0$. On the other hand, the *p-p* histograms in Figs. 5(c) and 5(d) show moderate intensity at $G > 10^{-4}G_0$ but decrease at lower conductances. Different from the *p-n* histogram, the *p-p* histogram depends little on the bias polarity and exhibits the same behavior for both positive and negative sample biases. These results show that Si NWs of $G \lesssim 10^{-4}G_0$ are predominantly produced only when the *p-n* tip-sample junctions are stretched under positive sample biases. At the opposite bias polarity, or in the *p-p* combination, the junctions tend to fail at $G \gtrsim 10^{-4}G_0$, without further shrinking to form NWs of lower conductances. A possible source of this polarity-dependent junction stretching would be a current effect because the *p-n* tip-sample junctions at $\sim 0.2G_0$ revealed a rectifying $I-V$ characteristic, and the positive and negative sample biases correspond to the reverse and the forward biases, respectively. Perhaps, under the forward bias condition, the junction current would become too high to promote the necking evolution but would rather make the junction unstable. In the histogram shown in Fig. 5(a), the intensity becomes reduced with increasing the sample bias up to +5 V. As in the case of metal NWs,[21] this suppression of the histogram intensity is probably due to the junction instability caused by high biases/currents, which would rupture most *p-n* junctions at +5 V, before they shrink into smaller junctions. According to the $I-V$ curve measured at $0.2G_0$, the current flowing through the *p-n* junctions at −2 V would be orders of magnitude higher than the current at +5 V. It would thus be reasonable to consider that the current effect under the forward-bias conditions is strong enough to disrupt the junction at their early stage of necking deformation and yield negligible intensity in the histogram in Fig. 5(b). The moderate intensity in the *p-p* histograms cannot, however, be understood solely in terms of the current effect, and some additional factors should be taken into consideration for obtaining the full understanding of the doping-dependent deformation of Si NWs.

We consider that the high-bias/current instability mentioned above occurs when the junctions are thick and in high-conductance states. Once they shrink into the low-conductance states, the junction current decreases and probably makes little Joule heating. According to the theoretical analyses made by Cheng *et al.*,[22] the local heating of NWs depends on the conductance and the phonon thermal coupling with the electrode. They showed that the local temperature of a molecular benzenedithiol junction is much lower than that of a gold single-atom contact because the former

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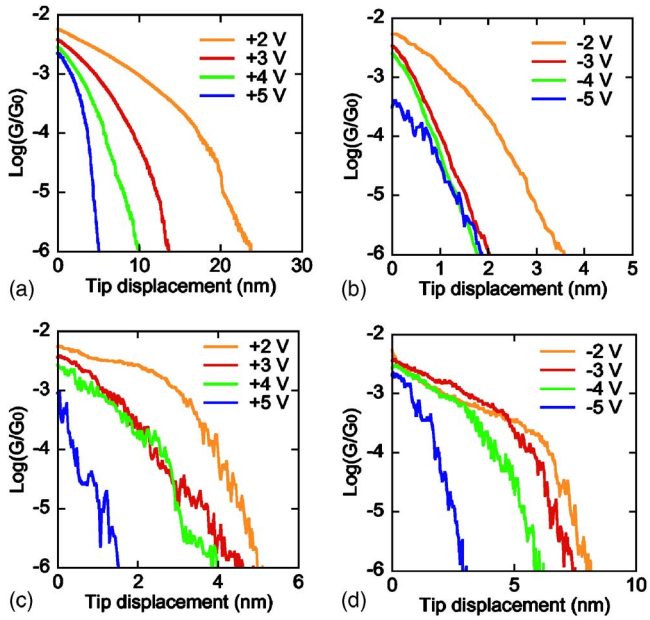

FIG. 6. (Color online) The $\log(G/G_0)-\Delta L$ curves in the low-conductance region $G<10^{-3}G_0$ obtained under different sample biases. As in Fig. 6, the plots (a), (b) and (c), (d) are for the *p-n* and the *p-p* junctions, respectively. Note that each plot has a different scale for ΔL, for clearly displaying the behavior of $\log(G/G_0)$. Below $\sim 10^{-5}G_0$, all curves show a nearly linear decrease with increasing ΔL, whereas they exhibit more moderate and nonlinear dependence at higher conductances. The latter behavior is particularly evident for the curves in (a).

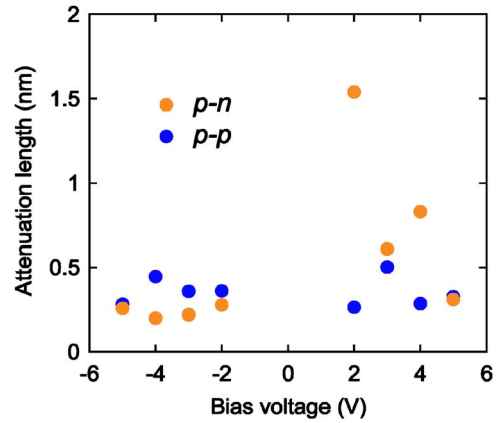

FIG. 7. (Color online) The attenuation length of the conductance deduced from the linear part of the $\log(G/G_0)-\Delta L$ curves in Fig. 6 is plotted as a function of the sample bias. The filled circles and squares represent the data for the *p-n* and the *p-p* junctions, respectively. Despite some scatter, the magnitude of the attenuation length is around 0.5 nm and shows no systematic dependence on the bias and the junction type.

has lower conductance ($\sim 0.01G_0$) and higher stiffness. In the case of our Si NWs in the low-conductance region, their conductance is typically $(10^{-4}-10^{-5})G_0$, and the stiffness (as measured by Debye temperature) of Si is approximately four times higher than that of Au. We can thus expect no significant overheating in the low-conductance Si NWs. The bias-induced suppression of the histogram intensity in Fig. 5 does not represent the intrinsic instability of the low-conductance Si NWs but reflects the reduced chance of their formation at high biases.

D. Dependence of the conductance on junction stretching

Our experimental results show that the conductance of Si NWs decreases orders of magnitude, from $\sim 1G_0$ to $\sim 10^{-6}G_0$, with the tip retraction. To investigate how the conductance changes with the tip displacement, we averaged the conductance traces at each bias and obtained an average $G-\Delta L$ curve, where ΔL represents the tip displacement. The number of $G-\Delta L$ curves used for averaging is 40 and 10 for the *p-n* and *p-p* junctions, respectively. The results are shown in Fig. 6, where $\log(G/G_0)$ is plotted against ΔL. Note that each panel has a different scale for ΔL because the junction stretching strongly depends on the junction type and the bias condition as we showed in the previous section. In the low-conductance region, $\log(G/G_0)<-4$, all curves in Figs. 6(b)–6(d) show nearly linear decrement with ΔL, i.e., G decays exponentially with ΔL as $\exp(-\Delta L/\xi)$. By fitting the data in the range $\log(G/G_0)<-4$, we determined the attenuation length ξ and plotted it in Fig. 7 as a function of the sample bias. For the curves in Fig. 6(a), the linear region starts around $\log(G/G_0)\sim -5$ so that the fitting was made for $-6<\log(G/G_0)<-5$. The magnitude of ξ shows some scatter and becomes exceptionally large for the *p-n* junctions at +2 V. For other junctions, however, ξ lies around 0.5 nm and exhibits no systematic dependence on the bias and the junction type. Similar exponential decay of the conductance in the subquantum region has been observed by Rodrigo *et al.*[23] on semimetallic Bi NWs. They found that the decay length is a few nanometers at room temperature but decreases to a few angstroms at low temperatures. For the short decay length, they consider the tunneling conduction of carriers, where the barrier changes with the temperature. Since our ξ is in the same range as their low-temperature decay length, the tunneling with certain effective barriers might be a possible conduction mechanism for $-6<\log(G/G_0)<-4$. We, however, propose a different conduction mechanism, the carrier localization, for the exponential decay of the conductance. We first note that the observed ξ is comparable to the localization length of amorphous Si, which is typically ~ 1 nm.[24] As mentioned in Sec. II, our Si NWs are formed by the necking deformation of the tip-sample break junctions and would naturally contain considerable amounts of structural disorders. The formation of elongated and disordered Si NWs has been recently demonstrated by Justo *et al.*[25] in their molecular dynamics simulations of Si NWs under external tensile strain. Amorphization of NW has also been reported in the necking deformation of metal junctions at 300 K.[26–28] It is thus likely that our Si NWs, after being deformed into small-sized junctions, have sufficient disorders to give rise to the carrier localization.

When the conductance is still higher than $10^{-4}G_0$, the $\log(G/G_0)-\Delta L$ curves in Fig. 6 are convex upward and do not exhibit a simple exponential decay. This nonlinear behavior is particularly evident in curves in Fig. 6(a), where the NWs show larger stretching. For such elongated NWs, Pascual *et al.*[29] have pointed out that the localization length changes with the NW stretching, resulting in a quadratic dependence of $\log(G/G_0)$ on ΔL. They experimentally demonstrated that the resistance of the elongated Au NWs increases

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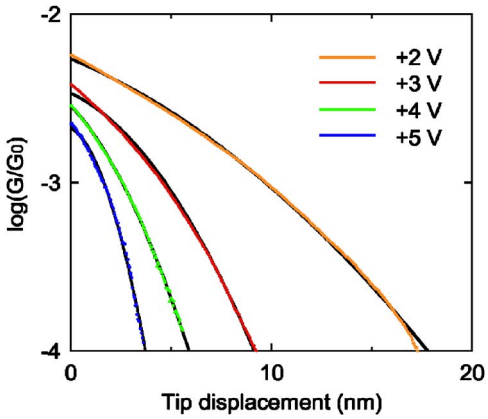

FIG. 8. (Color online) The quadratic fit (solid lines) to the nonlinear part of the $\log(G/G_0)-\Delta L$ curves in Fig. 6(a).

as a quadratic function of ΔL. If the carrier localization occurs in our Si NWs, a similar relationship could be expected for the nonlinear part of $\log(G/G_0)$ where the NWs are more or less elongated. We therefore fitted four $\log(G/G_0)-\Delta L$ curves in Fig. 6(a) by the quadratic form $A(\Delta L-L_0)^2+B$, where A, B, and L_0 are parameters. The fitting was carried out for $\log(G/G_0)>-4$, and the agreement with the data is quite satisfactory as shown in Fig. 8. Similar quadratic fitting can also be made for other $\log(G/G_0)-\Delta L$ curves in Fig. 6, but with moderate agreement with the data, probably because of the small junction stretching. These results provide another support for the localization-mediated conduction through our Si NWs. The whole behavior of the $\log(G/G_0)-\Delta L$ curves could be understood as representing the crossover from the elongated NW regime, where the varying localization length leads to the quadratic decrement of $\log(G/G_0)$ with increasing ΔL, to the atom-sized NW regime, where the localization length remains nearly constant and yields the conductance decaying exponentially with ΔL.

Through the above discussion, we have implicitly assumed that the junction conductance is determined primarily by the narrowest NW part of the junction, and other portions of the junction can be treated as leads to the NW. This is, however, indeed an oversimplification, and the real Si-Si tip-sample junctions should have complicated electronic structures along their length. At both ends of the junction, very far from the contact, the junction would remain a doped single-crystalline Si as initially prepared. But, coming close to the constriction, both the crystallinity and dopant concentration change along the junction, and the band gap may also vary with the junction diameter. On the sample side, the coupling of the junction states with the Si(111)7×7 surface states should also be taken into consideration. Accordingly, the electronic structure is not uniform along the junction axis, and some transitional zones in the band structure or band offsets might form local barriers for the carrier transport. In such a case, the observed $\log(G/G_0)-\Delta L$ curves can be interpreted as representing the transmission characteristics of such barriers, without appealing to the structural disorder and the carrier localization. For example, the observed exponential decay of G shown in Fig. 6 might be explained by direct tunneling through a depleted NW as we suggested before. Though we cannot rule out these conduction mechanisms, we still consider the localization conduction the likeliest because it provides us a plausible explanation of the observed $\log(G/G_0)-\Delta L$ characteristics not only for $\log(G/G_0)<-4$ but also for $\log(G/G_0)>-4$.

It should be pointed out that Kizuka *et al.*[18] found no evidence of amorphization in their direct TEM observations of Si NWs, even though their NWs were also formed by the junction breaking. They instead observed recrystallization and growth of Si NWs. Presumably, the higher bias voltage (10 V), and the resulting higher current density, employed in their experiments might have promoted the migration of junction atoms, healed structural disorders, and prevented the NWs from amorphization. Our disordered Si NWs could have been annealed out if we could apply higher biases around 10 V. In our experiment, however, the NWs rapidly fail at ±5 V, and the current-induced annealing could not be realized in our Si NWs.

IV. CONCLUSION

Recent experiments have demonstrated that the Si-Si tip-sample break junction can produce Si NWs at room temperature. In this work, we have exploited this method for studying the conductance of Si NWs, formed between *p*-type Si tips and *p*- and *n*-type Si clean surfaces at room temperature in UHV. Upon breaking the tip-sample junction, we found that the conductance varies by orders of magnitude in the subquantum range, from $1G_0$ to $10^{-6}G_0$. Conductance plateaus occasionally appear in conductance traces but produce no peaks in the usual conductance histogram. The histograms for $G>10^{-3}G_0$ show some peaklike features only when they are plotted in the logarithmic conductance scale. On the other hand, the histograms for $G<10^{-3}G_0$ are featureless, even in the logarithmic scale, but show strong dependence of their intensity on the doping and the bias polarity. The reverse-biased *p*-tip-*n*-sample junctions yield appreciable intensity in the low-conductance histogram, whereas the forward-biased junctions make negligible contributions, perhaps due to the higher junction current which tends to disrupt the junction necking during its early stage.

Analyses of the conductance as a function of the tip displacement revealed two regimes showing different $\log(G/G_0)-\Delta L$ characteristics. In the range $-6<\log(G/G_0)<-4$, $\log(G/G_0)$ decreases linearly with ΔL while it shows a quadratic dependence on ΔL for higher conductances. We find that the carrier localization can account for both these characteristics. This result suggests that the Si NWs formed in the Si-Si tip-sample break junctions would contain a significant degree of disorder.

Note added in proof: TEM observations of the plastic formation of long necks and the amorphization of SI NWs have been recently reported by X. Han *et al.*[30]

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