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Kyoto University
Plasma-Induced Defect-Site Generation in Si Substrate and Its Impact on Performance Degradation in Scaled MOSFETs

Koji Eriguchi, Yoshinori Nakakubo, Asahiko Matsuda, Yoshinori Takao, and Kouichi Ono

Abstract—Plasma-induced ion-bombardment damage was studied in terms of defect sites created underneath the exposed Si surface. From the shift of capacitance–voltage \((C–V)\) curves, the defect sites were found to capture carriers (being negatively charged in the case of an Ar plasma exposure). This results in a change of the effective impurity-doping density and the profile. We also report that the defect density depends on the energy of ions from plasma. A simplified and quantitative model is proposed for the drain–current degradation induced by the series-resistance increase by the damage. The relationship derived between the defect density and the drain–current degradation is verified by device simulations. The proposed model is useful to predict the device performance change from plasma process parameters.

Index Terms—Capacitance, defect site, device simulation, drain current, plasma-induced damage (PID).

I. INTRODUCTION

WITH regard to the present-day process technology, plasma processing is widely used for fabricating finer patterns with anisotropic features in advanced MOSFETs. In general, plasma-induced damage (PID) is classified based on the mechanism into charging damage, physical damage, and radiation damage [1]. Physical damage is commonly associated with the damage induced by high-energy ion bombardment on material surfaces. Damage to the Si surface occurs during gate-, offset-, and sidewall-spacer etch processes, resulting in Si material surfaces. Damage to the Si surface occurs during gate-, offset-, and sidewall-spacer etch processes, resulting in Si material surfaces. From the shift of capacitance–voltage \((C–V)\) curves, the defect sites were found to capture carriers (being negatively charged in the case of an Ar plasma exposure). This results in a change of the effective impurity-doping density and the profile. We also report that the defect density depends on the energy of ions from plasma. A simplified and quantitative model is proposed for the drain–current degradation induced by the series-resistance increase by the damage. The relationship derived between the defect density and the drain–current degradation is verified by device simulations. The proposed model is useful to predict the device performance change from plasma process parameters.

II. IMPACTS OF PLASMA-INDUCED PHYSICAL DAMAGE

A. Defect-Site Generation During Plasma Processing

Fig. 1 shows mechanisms of plasma-induced physical damage. This figure shows an offset-spacer etch process. As shown, the damaged layer with defect sites is formed by an impact of energetic ions accelerated in the plasma sheath. As analyzed by ellipsometry and molecular dynamic simulations [3], [11], the damaged layer consists of two regions, i.e., the surface and interfacial layers (in this letter, we will abbreviate them as SL and IL, respectively). The SL is composed of SiO\(_2\) and SiO\(_2\) phases [3], [11]. As expected, during the subsequent wet-etch step, the SL and a portion of the IL are stripped off. However, as deduced from the results by Kokura et al. [6], some defects are still present and expected to induce the variation...
of impurity-doping profile as a carrier trapping site, because they are not fully recovered by the subsequent annealing. Thus, this mechanism is believed to exacerbate the variation of device performance.

B. Analysis of Defect-Site Density

In this section, we experimentally clarify the electrical characteristics and density range of defect sites created by the plasma. N-type (100) Si (\(\sim 0.02 \ \Omega \cdot \text{cm}\)) was exposed to an inductively coupled plasma (ICP) with Ar gas mixture for 30 s. A sample without the exposure served as a reference. The source ICP power was 300 W, and the pressure was \(2.0 \times 10^{-2}\) torr. RF bias at 13.56 MHz (\(P_{RF}\)) was applied with various powers ranging from 0 to 100 W. Plasma diagnostics determined the plasma potential (\(V_p \sim 11.0\) V) and the average self dc bias (\(V_{dc} < 0\)). The present plasma configuration results in a constant ion flux \((\Gamma_i)\) to Si substrate [12] for all conditions \((\Gamma_i \sim 5.0 \times 10^{10} \text{ cm}^{-2} \cdot \text{s}^{-1})\). Since the bias frequency is high enough, the ion energy distribution function has a narrow energy spectrum [13]. Thus, we define the average impacting ion energy \(E_i\) as \(q(V_p - V_{dc})\), where \(q\) is electronic charge. Therefore, the incident ion energy was varied throughout the experiments with \(\Gamma_i\) being constant.

We conducted capacitance–voltage (C–V) measurement to clarify the electrical feature of defects by using a mercury probe without inducing any additional damage by forming an electrode. As shown in Fig. 2, we evaluated the bias-voltage shift (\(\Delta V_b\)) in C–V curves at \(0.4 \times 10^{-8} \ \text{F}\) for various plasma-exposed samples. As shown, \(\Delta V_b\) increases with an increase in \(P_{RF}\). In addition, in the present case, \(V_b\) shifts toward the positive direction. This implies that the defects are able to capture negative charges (electrons). Thus, the defects are considered to trap or detraps electrons in accordance with applied bias, i.e., in this case, electron trapping sites [4], [13]. Further study is required to ascertain the energy level of these defects in detail. By assuming that the defect sites are located within the IL, one can estimate an areal defect density \(N_d\) from the thickness of SL and IL [14]. The results are listed in the table shown in Fig. 2. As shown, the estimated \(N_d\) increases with an increase in \(E_i\). From the IL thickness obtained by SE \((\sim 2 \ \text{nm})\) [3], the estimated areal density range of \(N_d\) corresponds to an average volume density on the order of \(\sim 10^{19} \ \text{cm}^{-3}\), which is consistent with the results by other methods [4]. Thus, we focus on the peak volume density of defect which ranges from 0 to \(10^{19} \ \text{cm}^{-3}\).

C. Model for Drain–Current Degradation By Defect Site

In order to clarify the plasma-induced device performance degradation, we consider the case shown in Fig. 1 without the recess \((d_R = 0)\). As discussed earlier, the defects are carrier trapping sites, thus change the doping density and its profile in the S/D extension (SDE) regions, resulting in increase in the series resistance \((R_{dam})\), as shown in Fig. 1. By taking into account the voltage drop by the series resistance [15], one can write the drain current for damaged devices with \(R_{dam}\) as

\[
I_d = \frac{\mu C_{ox} W (V_g - V_{th} - V_d/2) (V_d - 2V_d R_{dam})}{1 + \theta (V_g - V_{th} - V_d R_{dam})}
\]

where \(L_{eff}\) is the effective channel length, \(\mu\) is the effective surface mobility, \(C_{ox}\) is the dielectric capacitance, \(W\) is the channel width, \(\theta\) is a mobility-degradation coefficient, \(V_g\) is the gate voltage, and \(V_{th}\) is the threshold voltage. Since the PID under consideration does not affect the mobility in channel region, one can let \(\theta = 0\). In the case of a low-drain bias case \((V_d \ll (V_g - V_{th}))\), the drain current is described as

\[
I_d^\text{dam} = \frac{\beta' V_d}{1 + 2 \beta' R_{dam}}
\]

where \(\beta' = \mu C_{ox} W / L_{eff} \cdot (V_g - V_{th} - V_d/2)\). For simplicity, in (2), we define \(R_{dam} = A \times (n_0 - n_{dam})^{-1}\) [14], where \(n_0\) and \(n_{dam}\) are the effective dopant density in the SDE without PID and the effective defect-site density, respectively. Note that \(n_0\) depends on the peak concentration and the junction depth \((X_j)\), and \(n_{dam}\) on the peak defect-site density (or \(N_d\)) and the distribution depth \((X_{dam})\). \(A\) is the SDE structure-dependent constant. From the experimental result [3], as aforementioned, \(X_{dam}\) is a few nanometers; thus, \(X_j \gg X_{dam}\). This means that \(n_0 \gg n_{dam}\), i.e., \((2A\beta' + n_0) \gg n_{dam}\). Therefore, one can make an approximation for the drain–current degradation in (2) as

\[
I_d^\text{dam} \approx \frac{\beta' V_d}{2A\beta' + n_0} \left( n_0 - 2A\beta' + n_{dam} \right).
\]

This equation indicates that \(I_d^\text{dam}\) depends linearly on \(n_{dam}\).

D. Device Simulations

In order to investigate the device performance degradation and to verify the relationship in (3), we performed 2-D technology computer-aided design (TCAD) simulations for n-channel MOSFETs. Gate dielectric thickness was 2 nm. The substrate doping was \(5 \times 10^{17} \ \text{cm}^{-3}\). The peak concentration of SD region was \(1 \times 10^{20} \ \text{cm}^{-3}\). The junction depth of SD was 120 nm. The peak concentration of SDE region \((n_{0\text{max}})\) was

Fig. 2. Capacitance–voltage curves of metal/SL/IL/Si structure obtained by a mercury probe for various bias powers \(P_{RF}\). The table lists the average ion energy \(E_i = q(V_p - V_{dc})\) and the calculated areal density of defect site \(N_d\).
and $\mu$ estimated by (3). In this calculation, gate length $L_g$ is employed. The defect site by PID was introduced as the counter doping [6] with its peak value $n_{\text{dam}}$ at the Si surface. $X_{\text{dam}}$ was 2.0 nm. At $X_{\text{dam}}$, the density is $0.1 \times n_{\text{dam}}$. We adopted a Gaussian profile for the distribution tail. This assumption is based on the imponging ion profile obtained by an etching profile simulation [1], [4], [16]. This is also consistent with the damage distribution model by ion implantation [5], [17]. Based on a Gaussian profile, $n_0$ and $n_{\text{dam}}$ are in proportion to $n_{0_{\text{max}}}$ and $n_{\text{dam_{max}}}$, respectively. Details of other parameters used in this letter are described elsewhere [3]. Fig. 3 shows the simulated results. As shown, the drain current decreases with the increase in $n_{\text{dam_{max}}}$, and the slope becomes steeper as the gate length ($L_g$) becomes shorter. Fig. 3 also shows the results estimated by (3). In this calculation, $L_{\text{eff}} = L_g - \Delta L$ (5 nm) and $\mu = 210 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ were used. The $n_0$ and $n_{\text{dam}}$ in (3) are derived from $n_{0_{\text{max}}}$, $n_{\text{dam_{max}}}$, and the profiles ($X_j$ and $X_{\text{dam}}$). Other parameters were determined from TCAD data for the references with various $L_g$. The good agreement between TCAD data and (3) is shown. Since the defect-site density can be determined from the PID analyses as performed in this letter, one can predict the drain–current degradation from the PID data by using (3).

III. CONCLUSION

A linear relationship between defect-site density and drain current has been proposed. The model was verified by the device simulations. The proposed quantitative model is useful to estimate the device performance degradation from plasma parameters ($T_1$ and $E_i$) via $N_d$ and IL thickness. Moreover, one can quantify the damage by the device parameter change.

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