

Digital Active Gate Drive of SiC MOSFETs for Controlling Switching Behavior — Preparation toward Universal Digitization of Power Switching

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Summary

In this paper, a digital active gate driver for SiC power MOSFETs is proposed. High-frequency switching with SiC power MOSFETs can realize an integrated power circuit with higher power density. However, the large surge voltage and ringing caused by the fast switching will lose the reliability of the device and increase electromagnetic interference (EMI) problems. To achieve high-frequency switching without these drawbacks, an active gate driver based on the architecture of a digital-to-analog converter has been designed. The gate-source voltage waveform of the MOSFET is generated directly and flexibly by a multibit gate signal sequence, considering the device characteristics and a variety of circuit conditions. Effective gate signal sequences are investigated by focusing on the switching trajectory on the state space of the device, which is discretely controlled through successive transitions between operating points. Experimental and simulated results confirm that the proposed gate driver effectively suppresses and regulates the surge voltage and ringing during turn-off.

Keywords: digital active gate drive, EMI, fast switching, SiC MOSFET, surge voltage, switching trajectory

1 Introduction

The development of wide-bandgap (WBG) semiconductor power devices, such as SiC power MOSFETs, has opened up a promising future for power electronics [1, 2, 3]. To make full use of its superior physical potential, improvements are needed in associated technologies such as gate drive circuits and packaging [2]. Higher power density and more degree of integration can be realized by the high-frequency switching of WBG devices, which is especially important for applications in the limited space, such as electric vehicles or airplanes [3]. Nowadays, SiC power MOSFETs can be switched at more than 10 MHz with an improved gate driver [4]. In another study [5], GaN HEMT is applied in a boost converter, achieving switching frequency as high as 25 MHz. On the other hand, such fast and high-frequency switching faces to large surge voltage and ringing during its switching transient, attributed to the presence of parasitic components in the circuit [6]. They lose the reliability of the power device, increase electromagnetic interference (EMI) problems, and can even cause self turn-on phenomenon [7]. Conventionally, these drawbacks have been handled by applying external circuits, such as a snubber. However, the overall circuit size and switching losses can be increased by such approaches [8, 9]. Moreover, flexible meeting variable operating conditions is challenging, which restricts the versatility of power switching utilizing WBG power devices. In relatively low-power converters, EMI reduction can be achieved by spread-spectrum clocking [10]. Even so, for WBG devices exhibiting high switching speeds and output powers, each switching operation must be optimized to achieve the widespread application of these devices.

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Active gate drive has been intensively studied to achieve a better trade-off among the surge voltage, EMI, and switching losses by controlling the switching speed of the power devices during the switching transient. It was first applied to IGBTs to control the gate current during the Miller period [11] or to apply additional gate resistances during reverse recovery in the bridge configuration [8]. In another study [12], active gate drive based on gate-input-voltage control has been investigated. In recent years, active gate drivers for WBG power devices have also been studied [9, 13, 14, 15, 16]. As the switching speed increases, constructing real-time analog feedback control becomes challenging. In fact, this observation was reported earlier [11], and phase-locked-loop-based feedforward control was adopted. Digitalized active gate drivers have been studied for their potential in achieving flexible open-loop control, such as a programmable one for GaN FETs [14] and for IGBTs using sequential optimization [17], while the study on real-time feedback control was reported [18]. FPGA-controlled stage-wise switched resistor [15] or multi-voltage-level [16] active gate drivers for SiC MOSFETs are investigated for their applications in multiple conditions. An active snubber is also a promising alternative [19]. However, its design principle depends on the operating conditions, thus limiting its flexibility.

In this paper, a digitalized, open-loop controlled active gate driver for SiC MOSFETs is investigated [20]. Inspired by the architecture of a digital-to-analog converter, the gate-source voltage is discretely treated using a multibit gate signal sequence. This allows the direct adjustment of the gate-source voltage waveform in response to the device characteristics and operating conditions. In particular, SiC MOSFETs are known to exhibit variations in device parameters, such as threshold voltage, whose mismatch leads a problem when they are connected in parallel [21]. Such voltage-related characteristics can easily be treated using the proposed driver by setting individual gate-source voltage waveform for each device. Here, the act of selecting the voltage level is strongly related to the device characteristics exposed on the state space of the MOSFET. The switching trajectory can be adjusted discretely by the successive alteration of gate-source voltage. We focus on this aspect by analyzing the switching behavior of the MOSFET on the state space. This is the concept that should be realized by the digitization of power switching, where such adjustments are totally managed in the gate-driver's side, using software. This will ease the restriction of the use of power devices with different characteristics, and enhance the potential of new functions and operations of power converters. The possibility of the concept is verified by developing a prototype of the proposed driver using a simple switching test circuit. Its operation is adjusted to investigate its effectiveness in suppressing the surge voltage and ringing.

2 Concept and configuration of digital active gate driver

Here, we propose a digital active gate driver for SiC power MOSFETs. As previously described, active gate drivers dynamically shape the gate-source voltage (V_{GS}) waveform of MOSFETs. The digital-to-analog converter architecture is introduced into the gate drive circuit; the V_{GS} waveform is directly shaped through the successive alteration of V_{GS} by a multibit gate signal sequence. This is possible because the gate drive circuit can switch faster than the main circuit. Since the gate signal sequence is adjustable flexibly, the proposed driver can designate a unique V_{GS} waveform for each MOSFET based on the device characteristics or circuit conditions.

2.1 Circuit design

The configuration of n -bit digital active gate driver is shown in Figure 1. It is designed according to the architecture of the binary-weighted resistor digital-to-analog converter. The n single gate drive circuits are connected in parallel with gate resistances of $2^k R \Omega$ ($k = 0, 1, \dots, n-1$). Note that each resistance value is a sum of the gate driver's output resistance and the gate resistance. When all the input signals $b_0, b_1, \dots, b_{n-1}$ are 1/0, the MOSFET is on/off. During the transient state of switching, the input signals are successively changed at the clock rate of the controller. They divide the gate input voltage (V_{drv}) by the switched gate resistors to set the value of V_{GS} as given by (1).

$$V_{GS} = \frac{R_{off}}{R_{on} + R_{off}} V_{drv} = \frac{\sum_{j=0}^{n-1} b_j 2^j}{\sum_{j=0}^{n-1} 2^j} V_{drv} \quad (1)$$

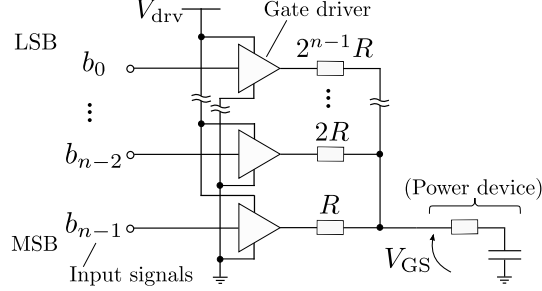


Figure 1: Configuration of n -bit digital active gate driver.

Here, R_{on} and R_{off} refer to the combined resistances of the gate resistors whose input signals are 1 and 0, respectively. The flexibility of the shaping depends on the number of bits and the clock rate of the gate signal. In this paper, 4 bit is examined because of its less complexity in circuit implementation without loss of generality. This driver is intended to be used for open-loop control, and the gate signal sequences are adjusted with taking the device characteristics into consideration. The idea of paralleling the gate drive circuits is somewhat similar to the reported AGDs using variable gate resistances [9, 13] or using multiple driver cells [14, 18]. These operations are completely different. The proposed driver directly designate a V_{GS} value rather than changing the gate resistance to control the time constant. Some of the reported variable-gate-voltage AGDs [12, 16] adopt three voltage levels typically for the simplicity in configuration and control. The proposed driver can set V_{GS} at multiple voltage levels successively during each turn-on/off operation without any limitation. This gains the flexibility of the gate-driving strategy and generality, which are apart from the hardware configuration.

2.2 Strategies for shaping gate-source voltage waveforms

To investigate effective V_{GS} waveforms to suppress the surge voltage, an understanding of the detailed switching operation is required [22]. An example of the switching waveforms of the MOSFET during turn-off is shown in Figure 2(a) with solid lines, in which V_{DS} denotes the drain-source voltage and I_{D} the drain current. Here, an ideal resistive load is assumed. The switching trajectory is shown in Figure 2(b), along with the $I_{\text{D}}-V_{\text{DS}}$ characteristics for several values of V_{GS} . The turn-off operation begins at t_1 when 0 V is applied to the gate terminal. Then, V_{GS} starts to decrease until it becomes flat at the Miller plateau voltage (V_{plateau}). During this period, the MOSFET operates in its quasi-linear region. V_{GS} stays flat until t_2 owing to the Miller effect, where almost only the gate-drain internal capacitor is discharged. At t_2 , the MOSFET enters its saturation region, and both I_{D} and V_{DS} start to change rapidly. At t_3 , V_{GS} crosses the threshold voltage (V_{th}), and the MOSFET turns off.

In a real circuit, because of the presence of stray inductances, the fast turn-off of the device leads to large surge voltage and ringing, as shown in Figure 2(a) with dashed lines. They can be suppressed using active gate drive, as it regulates the large di/dt of the drain current. If we set V_{GS} between V_{plateau} and V_{th} during t_2 and t_3 , the switching becomes slow only during the period and the surge voltage is hopefully reduced. This is equivalent to setting operating points on the state space and thereby controlling the switching trajectory discretely, as illustrated in Figure 3. Note that the V_{GS} -shaping strategy depends on the load conditions, because the load line is not the simply linear relationship.

2.3 Evaluation method for switching time

The switching time of the MOSFET used to be calculated from the V_{DS} waveform, and indicates how quickly the device can be turned on or off. However, when high-amplitude ringing appears, the output power of the MOSFET does not reach a stable state, making it difficult to specify the end of the switching operation clearly. Instead, the following index is introduced to estimate how long the device is in the transient state during the switching operation. The ON and OFF regions on the $I_{\text{D}}-V_{\text{DS}}$

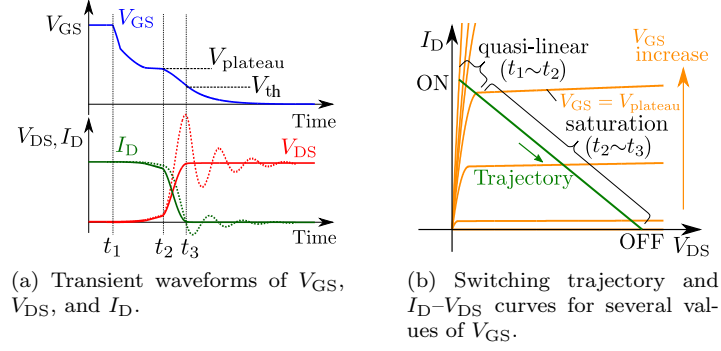


Figure 2: Examples of switching waveforms of MOSFET during turn-off, assuming load is an ideal resistor.

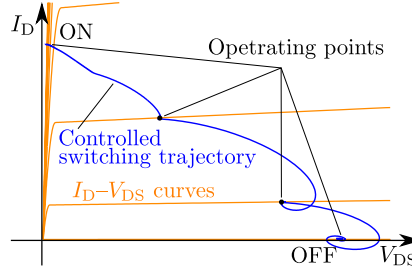


Figure 3: Conceptual diagram of switching trajectory control using discrete operating points.

plane are used for this definition, which are given by (2).

$$\begin{cases} \text{OFF region : } \left(\frac{I_D}{I_{D,\text{on}}} \right)^2 + \left(\frac{V_{DS}}{V_{DS,\text{off}}} - 1 \right)^2 \leq 0.2^2 \\ \text{ON region : } \left(\frac{I_D}{I_{D,\text{on}}} - 1 \right)^2 + \left(\frac{V_{DS}}{V_{DS,\text{off}}} \right)^2 \leq 0.2^2 \end{cases} \quad (2)$$

Here, $I_{D,\text{on}}$ denotes the value of I_D when the MOSFET is on, and $V_{DS,\text{off}}$ that of V_{DS} when the MOSFET is off. We define $t_{\text{tran,off}}$ for turn-off and $t_{\text{tran,on}}$ for turn-on as the time between the transition from one region to another, until the trajectory converges in the region. With these definitions, as long as the ringing remains, the switching is regarded to be in a transient state and does not converge. This index is particularly relevant to high-frequency switching because the transient state accounts for a large proportion of a switching period.

3 Experimental verification

In this section, the operation of the proposed gate driver is verified in the experiment. Various V_{GS} waveforms are tested for their effectiveness in suppressing the surge voltage during turn-off without sacrificing the switching time.

3.1 Fabricated circuit

Figure 4 shows the photograph of the digital active gate driver fabricated on a PCB. The schematic diagram of the circuit is shown in Figure 5. A commercial isolated gate driver (Si Labs, Si8235) is used as the switch for each bit. Gate resistors are selected considering the output resistances of this driver, which are 2.7Ω for source operation and 1.0Ω for sink operation [23]. The gate signals are generated by an FPGA (National Instruments, sbRIO-9607) and are changeable at the clock of 40 MHz. SiC MOSFET (ROHM, SCT2450KE) is switched at 50 kHz and 33 V is supplied. The load is composed

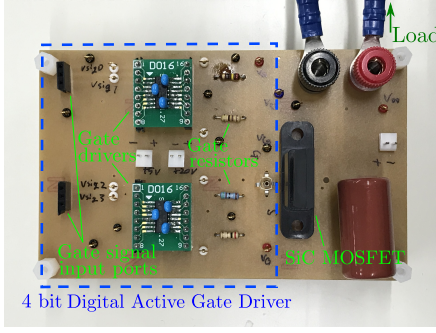


Figure 4: Photograph of fabricated circuit.

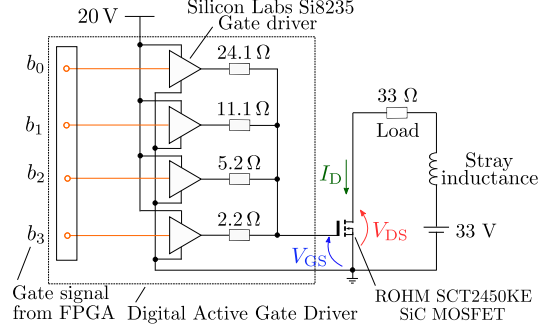


Figure 5: Schematic diagram of experimental circuit.

of a resistor of 33Ω and wires, which has a large stray inductance and contributes to a large surge voltage during turn-off.

3.2 Switching improvements with active gate drive

Firstly, the MOSFET is switched without active gate drive (without AGD); the gate signal is changed from 1111 to 0000 during turn-off. The switching waveforms of V_{GS} , V_{DS} , I_D , and instantaneous power dissipation ($P_D = V_{DS} \times I_D$) are plotted in Figure 6 with red lines. A large surge voltage and ringing are apparent, and the peak of V_{DS} is 90.8 V. Secondly, to investigate the relationship between the

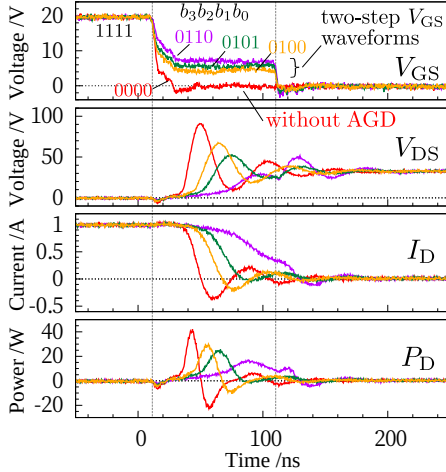


Figure 6: Switching waveforms without AGD and with simple two-step V_{GS} waveforms.

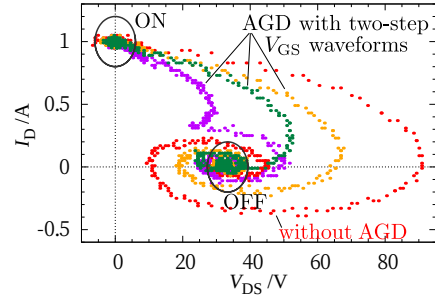


Figure 7: Switching trajectories without AGD and with simple two-step V_{GS} waveforms.

value of V_{GS} and the switching waveform, the simple two-step V_{GS} waveforms as shown in Figure 6 with purple/green/yellow lines are tested. Here, the three signals are selected out of the possible 15 levels because they showed the most remarkable change. The switching trajectories are also plotted on the phase plane in Figure 7 using the same colors. The ON and OFF regions given by (2) are also shown with ellipses.

When the gate signal is 0100, the gate charge extraction is slowed down and the surge voltage is suppressed. The switching trajectory moves toward the OFF operating point from the start. In the next case, the switching trajectory moves toward the outside of the OFF region during 0101 is input. This means that the designated V_{GS} is between $V_{plateau}$ and V_{th} . The switching is therefore not completed during the period, but it is when the gate signal turns 0000. It is more clear in the last case, where, while 0110 is given, the switching trajectory stays between the ON and OFF regions, and

then the rest of the switching continues when the gate signal turns 0000.

From these results, it is confirmed that the surge voltage can be suppressed by setting V_{GS} between $V_{plateau}$ and V_{th} .

3.3 Switching results with adjusted gate signal sequences

In the cases above, the gate charge extraction is slowed down, which results in the delay of V_{DS} and I_D to start switching. To discharge it quickly before switching begins, 0000 should be sent briefly as the first step of turn-off, until V_{GS} reaches $V_{plateau}$. Also, after V_{DS} and I_D finish switching, the gate signal should quickly be changed to 0000 to complete the turn-off operation.

Considering these, the gate signal sequence is adjusted as listed in Table 1 through trial and error. The resulting waveforms are plotted in Figure 8 and Figure 9. Table 2 shows the peak of the surge voltage ($V_{DS,peak}$), calculated $t_{tran,off}$, and switching loss (P_{mos}) in each case, compared with those without active gate drive. Between AGD 1 and 2, the surge voltage is better suppressed in AGD 2, by about 50 V compared with that without AGD. The switching time is shorter in AGD 1, because in AGD 2 the trajectory stays longer outside the OFF region. The reason for these differences is that the designated value of V_{GS} in AGD 2 is slightly above V_{th} , as confirmed in Section 3.2, which leads to the slower switching speed during the active period. It is expected that by combining these two waveforms, as can be observed in AGD 3, a good balance between the V_{DS} peak and $t_{tran,off}$ can be achieved. In AGD 3, the switching trajectory first follows that of AGD 2, and then switches to that of AGD 1. However, although the surge voltage is well suppressed, the switching time is the longest among these three. This is probably because of the additional fluctuation in V_{GS} , followed by the additional oscillation in V_{DS} and I_D .

The turn-off loss in the MOSFET (P_{mos}) is calculated by integrating P_D . Since the slopes of V_{DS} and I_D become gentle by active gate drive, the loss inevitably increases. The loss in the gate drive circuit also increases due to the configuration of the digital-to-analog converter. The efficiency of this driver for practical application needs to be investigated.

In short, the proposed gate driver and the strategy of shaping the V_{GS} waveform proved effective

Table 1: Adjusted gate signal sequences during turn-off.

case	gate signal sequence (changed every 25 ns)
AGD 1	1111 → 0000 → 0100 → 0100 → 0000
AGD 2	1111 → 0000 → 0101 → 0101 → 0000
AGD 3	1111 → 0000 → 0101 → 0100 → 0000

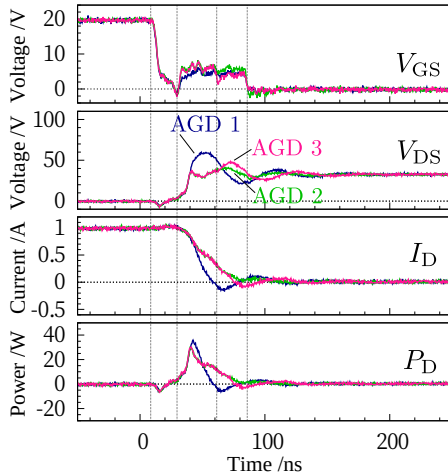


Figure 8: Switching waveforms in AGD 1, 2, and 3.

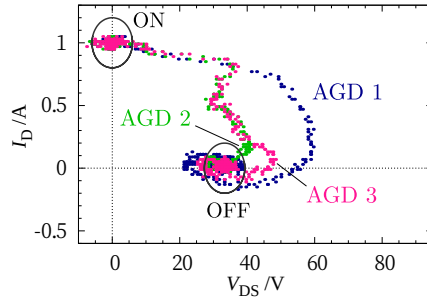


Figure 9: Switching trajectories in AGD 1, 2, and 3.

Table 2: Peak of surge voltage, switching time, and switching loss.

case	$V_{DS,peak}$ (V)	$t_{tran,off}$ (ns)	P_{mos} (μ J)
without AGD	90.8	115	0.21
AGD 1	59.6	61	0.43
AGD 2	41.2	73	0.64
AGD 3	48.4	88	0.60

in suppressing the surge voltage and mitigating the turn-off transient. It is also confirmed that the adjustment of the gate signal sequence allows the application of various V_{GS} waveforms. This result characterizes the proposed driver, because the operating principle of many reported active gate drivers, such as switched resistor ones, limits the outline of the V_{GS} waveform. The increase in the number of bits and the clock rate will facilitate the development of sophisticated strategies.

3.4 In-rated switching operation test of SiC MOSFET

As described above, the main issue of this paper focused on confirming the operation of the proposed gate driver. However, because SiC MOSFETs are aimed at high-power applications, the proposed gate driver also needs to be tested in a higher power region. Accordingly, the operating condition is set at 200 V and 4 A using the same circuit board. The transient switching waveforms and switching trajectories without and with AGD are shown in Figures 10 and 11, respectively. As can be seen in

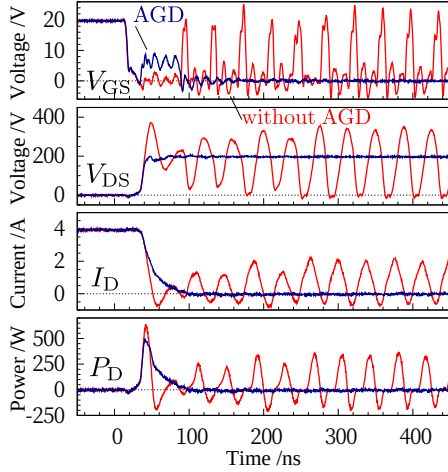


Figure 10: Switching waveforms without/with AGD under a higher-voltage condition.

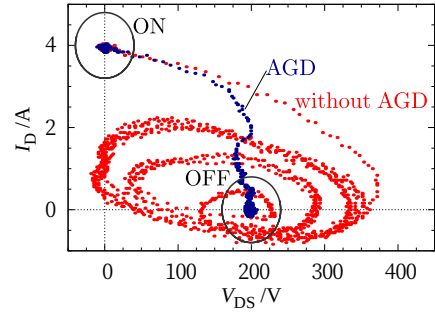


Figure 11: Switching trajectories without/with AGD under a higher-voltage condition.

Figure 10, the switching waveforms without AGD exhibit sustained oscillation at around 25 MHz. This frequency approximately corresponds to the resonant frequency of stray inductance and the output capacitance of the MOSFET, which are hundreds of nH and hundreds of pF, respectively. Meanwhile, with AGD, where the gate signal sequence is adjusted to 1111 $\rightarrow$ 0000 $\rightarrow$ 0101 $\rightarrow$ 0101 $\rightarrow$ 0000 every 25 ns, oscillation does not occur and the surge voltage is suppressed. In Figure 11, the trajectory without AGD first approaches the OFF operating point, until the oscillation begins and the trajectory converges into a limit cycle outside the OFF region. With AGD, the trajectory smoothly moves toward the OFF operating point.

The circuit used here has large stray inductances on purpose, which caused oscillation at a relatively low voltage. However, such a failure in circuit operation can happen with less stray inductances under much higher voltage conditions. These results indicate that the influence of stray inductances can be set aside by active gate drive. In other words, active gate drive allows larger stray inductances, which

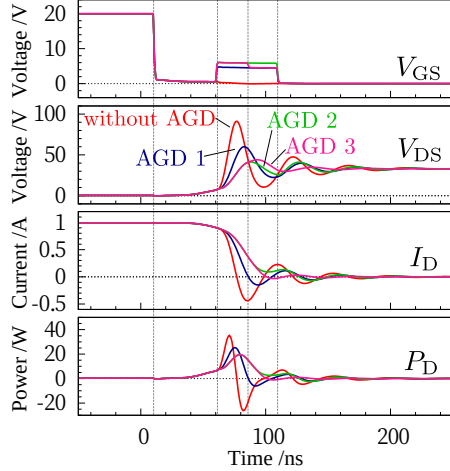


Figure 12: Simulated switching waveforms without/with AGD.

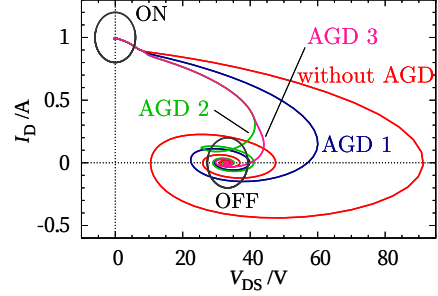


Figure 13: Simulated switching trajectories without/with AGD.

Table 3: Peak of surge voltage, switching time, and switching loss (simulation).

case	$V_{DS,peak}$ (V)	$t_{tran,off}$ (ns)	P_{mos} (μ J)
without AGD	91.3	88	0.23
AGD 1	60.0	55	0.46
AGD 2	41.5	71	0.63
AGD 3	44.1	41	0.57

will ease the restrictions in circuit design and operation, especially in highly-integrated power circuits.

4 Simulation results

The verification of the experimental results is given by SPICE simulation using the SIMetrix software. The simulation settings are basically the same as those shown in Figure 5, except for some differences as follows: the gate drivers are configured using ideal switches with the same output resistances as the Si8235; the characteristics of the SiC MOSFET is given by a model available on the manufacturer's website; the stray inductance in the main circuit is assumed to be 600 nH.

Switching waveforms without and with AGD are shown in Figure 12. The gate signal sequences in AGD 1, 2, and 3 are the same as in the experiment, except that 0000 is designated for the first 50 ns. This is because the time at which V_{DS} and I_D start switching is delayed compared to that in the experiment. It is confirmed that the driving results of without AGD, AGD 1, and AGD 2 approximately reproduce the experimental results. However, as opposed to the experimental results, AGD 3 shows the shortest switching time and a well-suppressed surge voltage, as shown in Table 3, which is the result we expected to see in the experiment. This difference is explained by the switching trajectory, which transits from that of AGD 2 to that of AGD 1 smoothly, thereby converging into the OFF region without additional oscillation.

The simulations indicate the possibility of predicting the appropriate gate signal sequences by utilizing the information obtained from device models. The analysis on the state space requires the accuracy of the model, especially the I_D - V_{DS} characteristics. The use of originally-developed surface-potential-based model of SiC MOSFET [24] helps us to develop the control strategy on the state space, which we have already started the investigation [25]. Then, starting from the predicted gate signal sequence, general optimization methods may be applied to further adjust the sequence according to the load condition and device parameter variation. The results in this paper provide important clues that will be a basis for developing control strategies and algorithms for generating gate signal sequences to obtain the physically appropriate power switching.

5 Conclusion

In this paper, the concept of the digital active gate driver for SiC MOSFETs is investigated via experiment and simulation. The proposed driver directly shapes the V_{GS} waveform using a multibit gate signal sequence, which provides a flexible gate-driving strategy. Discrete V_{GS} values give discrete operating points on the state space of the device. This point of view gives the advantage of controlling the switching trajectory of the MOSFET by means of digital signals. The experimental results indicate that the switching behavior of the device drastically changes by the selection of gate signal sequence during the switching transient. It is confirmed that the surge voltage during turn-off is suppressed and the switching transient is shortened by adjusting the V_{GS} waveform based on the measured device characteristics. These results are also verified in SPICE simulation. Meanwhile, it is suggested that the four-bit system is not enough to further improve the switching characteristics.

With more number of bits and faster clock rate, more controllability on the V_{GS} waveform will be achieved. This versatility paves the way for digital control schemes to function in a wide range of operating conditions and under different device characteristics. Also, the device model itself or the data obtained from it can be utilized in the algorithm and help predict the appropriate gate signal sequence. In particular, obtaining the accurate I_D - V_{DS} characteristics will be a key for developing the strategy on the state space. Based on these considerations, the desired switching behavior for a given condition will be reproduced digitally[†]. Further research is to consider the practical application of the driver, such as a series or parallel operation of SiC MOSFETs and power converters. We hope that these works contribute to the extensive applications of SiC MOSFETs.

Appendix

A Tests on another SiC MOSFET

The experimental results of driving another SiC MOSFET (Wolfspeed, C3M0280090D) are presented to demonstrate the flexibility of the proposed driver on different device characteristics. The same setup as described in Figure 5 is used. Figure A1 shows the driving results. It is confirmed that the surge

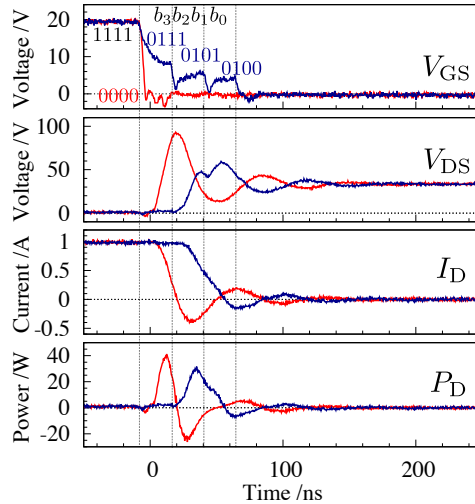


Figure A1: Switching waveforms of another SiC MOSFET. The gate signal sequence is individually adjusted.

[†]With the digital active gate driver, the variation of load condition is expected to be handled. A control strategy is developed [25] to work in a wide operating range based on the I_D - V_{DS} characteristics of the MOSFET. The effective gate signal sequence for improving the switching characteristics are predicted previously from the relationship between the load lines and I_D - V_{DS} curves on the state space.

voltage and ringing are suppressed by the individually adjusted gate signal sequence.

B Performance comparison with gate-resistance-incremented gate drivers

This section describes a comparison of gate drivers' performance between the proposed method and the conventional gate driver (CGD) with different values of gate resistances in simulation. We used the same setup as described in Section 4. The five cases as follows are compared; the first two cases, "without AGD" and "AGD 3", are picked up from Figure 12 and Table 3, and the other three cases are obtained using CGD, where one gate driver is used and the gate resistance (R_G) is set at 10/50/100 Ω . Figure B2 shows the simulated switching waveforms, and Table B1 shows the peak of surge voltage, switching time, and switching loss in each case. From Table B1, when $R_G = 100 \Omega$, the surge voltage is suppressed as low as in AGD 3. However, the switching loss and the switching time are almost doubled, and the switching is delayed compared to AGD 3. These results indicate that the proposed gate driver can achieve a better trade-off than the conventional gate drivers.

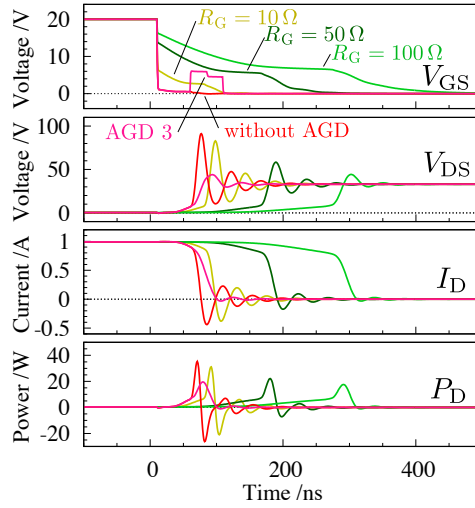


Figure B2: Simulated switching waveforms without AGD, with AGD 3, and with CGD ($R_G = 10/50/100 \Omega$).

Table B1: Peak of surge voltage, switching time, and switching loss: comparison between the proposed gate driver and the conventional gate driver (CGD) with incremented gate resistances (simulation).

case	$V_{DS,peak}$ (V)	$t_{tran,off}$ (ns)	P_{mos} (μJ)
without AGD	91.3	88	0.23
AGD 3	44.1	41	0.57
CGD ($R_G = 10 \Omega$)	83.0	76	0.32
CGD ($R_G = 50 \Omega$)	58.4	77	0.64
CGD ($R_G = 100 \Omega$)	44.3	83	0.98

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Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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