

**Interface Charge Engineering in
AlGaN/GaN Heterostructures
for GaN Power Devices**

2019

Satoshi NAKAZAWA

Interface Charge Engineering in AlGa_N/Ga_N Heterostructures for Ga_N Power Devices

August 2019

Satoshi NAKAZAWA

Department of Electronic Science and Engineering
Kyoto University

Abstract

In this thesis, effects of interface charges on the electrical characteristics of aluminum gallium nitride on gallium nitride (AlGa_N/Ga_N) heterojunction field-effect transistors (HFETs) have been studied to improve their performance. Owing to the superior properties of III-nitride semiconductor materials, Ga_N-based HFETs have attracted much attention as high frequency and high power devices which surpass the performance of conventional silicon (Si) power devices. One of the distinct features in III-nitride semiconductors from other conventional materials is their strong polarization effect, which yields the high density of the two dimensional electron gas (2DEG) without the intentional impurity doping at the heterojunctions, providing the large current density and the low sheet resistance. In addition, introduction of the metal-insulator-semiconductor (MIS) gate structures, which mitigate the gate leakage current degrading the performance of the devices with the conventional Schottky gate structures, offer the tolerance for the large gate-voltage swing and thereby enable the large current density even in the devices with the normally-off operations.

Meanwhile, control of the sheet carrier density and the threshold voltage requires the precise polarization engineering. The inadequate control of the polarization charges at the heterointerfaces leads to the undesired increase of the parasitic resistance, and thus limits the performance of the devices. As for the MIS gate structures, the instability in the transfer characteristics such as the threshold voltage shift or the hysteresis is often observed, which would be attributed to the charges at the MIS interfaces and/or in the insulators. The interface charges have profound effects on the performance of the Ga_N-based HFETs, and thus the control of such interface charges through designing and fabricating the devices is critical to improve the performance of the AlGa_N/Ga_N HFETs. In this thesis, the effects of the interface charges on the performance of the AlGa_N/Ga_N HFETs were investigated, from which the technical directions to control the interface charges were derived for the improvement in the device performance.

In Chapter 2, the effects of the polarization charges at the heterojunction on the electrical characteristics, particularly the parasitic resistance in the AlGa_N/Ga_N HFETs, are described. An InAlGa_N capping layer, the polarization of which was balanced with that of the underlying AlGa_N barrier layer, prevented the generation of the depletion layer at the InAlGa_N/AlGa_N heterojunction, which resulted in the reduction of the contact resistance. The value of the extracted parasitic resistance at the InAlGa_N/AlGa_N heterojunction was $7.8 \times 10^{-6} \Omega\text{cm}^2$, which was one-fifth as low as that of the resistance at the Ga_N/AlGa_N heterojunction.

In Chapter 3, AlGaIn/GaN HFETs on Si substrates exhibiting high power together with a high gain for high frequency applications are demonstrated. Effects of the field plates on the device performance were characterized through extraction of device parameters. Too long field plates cause the large variation in the output impedance at the high input power, which leads to the output mismatch limiting the output power. Suppression of the variation by the improved design of the field plate was confirmed by device simulation. The fabricated AlGaIn/GaN HFET on Si with the optimized field plates exhibits an output power of 203 W together with a linear gain of 16.9 dB at the operation frequency of 2.5 GHz, which is comparable with the performance of HFETs on SiC substrates.

In Chapter 4, effects of the device fabrication processes (dry etching, annealing and nitrogen incorporation) on the MIS interfaces were investigated to find the direction to achieve the stable MIS structures by characterizing the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MIS heterojunction diodes. Increase of the interface state density especially around 0.4 eV below the conduction band edge of AlGaIn was observed in the MIS diode fabricated on the dry etched AlGaIn surface, indicating generation of nitrogen vacancy by the dry-etching process. The post-deposition annealing in O_2 atmosphere at 750 °C caused the threshold voltage shift of +4 V with the reduction of the positive charges in the Al_2O_3 insulators by $6 \times 10^{12} \text{ cm}^{-2}$, which would be attributed to reduction of the oxygen vacancy in the insulators. Nitrogen incorporation into Al_2O_3 enhanced the tolerance to the electron injection, preventing the threshold voltage shift caused by applying the high positive bias to the gate electrodes. The threshold voltage shift was reduced from 0.6 to 0.2 V at the electric field in the insulators of 2 MV/cm.

In Chapter 5, normally-off AlGaIn/GaN MIS-HFETs on Si substrates with the stable gate characteristics were demonstrated. The MIS-HFETs fabricated by the device-process flow based on the results described in Chapter 4 exhibited the suppressed threshold voltage shift and hysteresis in the transfer characteristics at gate voltage up to 10 V. The stable gate characteristics enabled application of the high positive bias to the gate, which results in the fast switching operation of the fabricated MIS-HFETs with the gate width of 100 nm measured at the off-state drain voltage of 400 V, on-state drain current of 10 A, and in the inductive load condition. The switching time of 4 ns and 8 ns for turn-on and turn-off, respectively, was confirmed, which is fast enough to use practical MHz-class switching applications.

Chapter 6 concludes this thesis, summarizing the achievements in this study. Remaining issues and future work for further improvements are also described.

Acknowledgment

The author would like to express his deep gratitude to Professor Tsunenobu Kimoto for his providing the opportunity to accomplish this work and for his continuous guidance, supervision, and encouragement throughout this study. He would like to thank Professor Yoichi Kawakami and Associated Professor Kazuhiko Sugiyama for their valuable advice and comments on this study.

He wishes to express sincere gratitude to Emeritus Professor Hiroyuki Matsunami for his guidance, which has been genuinely valuable since the author started the research on semiconductors in 1999.

He also would like to express his special gratitude to Dr. Tetsuzo Ueda, Director of Industrial Business Development Center, Panasonic Corporation, for his providing the opportunity to accomplish this work and for his continuous guidance, supervision, and encouragement since the author started the research on GaN at Panasonic.

He is also very obliged to Dr. Daisuke Ueda (currently Specially Appointed Professor at Nagoya University) and Dr. Tsuyoshi Tanaka (currently Director of Sensing Solution Development Center, Panasonic Corporation), former Directors of Semiconductor Device Research Center, Matsushita Electric Industrial Co. Ltd for their providing the opportunity to accomplish this work.

Special thanks to Mr. Tsuguyasu Hatsuda, Director of Energy Solution Development Center for his supervision and support for this study. The author is grateful to Mr. Masahiro Ishida, Mr. Hiroyuki Handa, and Dr. Toru Yamada, for their support for this study as managers of Energy Solution Development Center, Panasonic Corporation, and other laboratory members. The author is especially grateful to Dr. Yoshiharu Anda and Mr. Naohiro Tsurumi for their support on the device development throughout this work. He also thanks to Mr. Satoshi Tamura for his kind encouragement for this study.

He is very obliged to Professor Takashi Egawa and Lecturer Hiroyasu Ishikawa (currently Professor at Shibaura Institute of Technology) at Nagoya Institute of Technology for their support and valuable advice on InAlGa_N growth.

He is also very much obliged to Professor Tamotsu Hashizume at Hokkaido University for his instructive advice on characterization on the MIS interfaces.

He is also obliged Professor Heiji Watanabe and Assistant Professor Takuji Hosoi at Osaka University for having valuable discussion on the characteristics of the MIS devices.

The author wishes to express thanks to Professor Jun Suda at Nagoya University and Associated Professor Hiroshi Yano at Tsukuba University for their continuous encouragement since the author

was a member of Matsunami laboratory at Kyoto University.

He wishes also express thanks to all members of Kimoto laboratory at Kyoto University for their kind support and cheerful encouragement.

Finally, the author indeed thanks to his wife, Mayumi, his children, Asuka and Takumi, his parents, and his parents-in-law for their understanding, support, and heartfelt encouragement.

Contents

Abstract	i
Acknowledgment	iii
Contents	v
Chapter 1. Introduction	1
1.1 Background	1
1.2 III-Nitride Semiconductors	3
1.2.1 Properties of III-Nitride Semiconductors	3
1.2.2 Polarization Effects	6
1.3 III-Nitride Heterojunction Field-Effect Transistors (HFETs)	9
1.4 Outline of Thesis	12
References	17
Chapter 2. Polarization Engineering in III-Nitride Heterostructures	21
2.1 Introduction	21
2.2 Polarization in III-Nitride Heterostructures	22
2.3 Effects of Polarization Charges on Electrical Characteristics	24
2.3.1 Polarization Engineering by InAlGa _N Quaternary Alloy	26
2.3.2 Crystal Growth and Device Fabrication	26
2.3.3 Analysis of Parasitic Resistance	28
2.4 Summary	35
References	38
Chapter 3. AlGa_N/Ga_N HFETs for High Frequency Applications	41
3.1 Introduction	41
3.2 High Power, High Gain AlGa _N /Ga _N HFETs	42
3.2.1 Structure of AlGa _N /Ga _N HFETs with Field Plates	42
3.2.2 Design of Field Plates	42
3.3 Performance of Fabricated AlGa _N /Ga _N HFETs	52
3.4 Discussion	52

3.5	Summary	55
	References	56
Chapter 4. Interface Properties in Al₂O₃/AlGa_N/Ga_N Metal-Insulator-Semiconductor		
	Diodes	59
4.1	Introduction	59
4.2	Characterization Method of AlGa _N /Ga _N MIS Heterostructures	60
4.3	Charge Engineering at MIS Interfaces during Device Fabrication Processes	60
4.3.1	Effects of Dry Etching Process	60
4.3.2	Effects of Annealing Process	67
4.3.3	Effects of Nitrogen Incorporation into Al ₂ O ₃	73
4.4	Discussion	77
4.5	Summary	77
	References	79
Chapter 5. AlGa_N/Ga_N MIS-HFETs for Power Switching Applications		
5.1	Introduction	83
5.2	Normally-off AlGa _N /Ga _N MIS-HFETs	83
5.2.1	Device Structure	83
5.2.2	Device Fabrication Process	85
5.3	Performance of Fabricated MIS-HFETs	85
5.4	Discussion	89
5.5	Summary	95
	References	96
Chapter 6. Conclusions		
6.1	Conclusions	97
6.2	For Future Work	99
List of Publications		
		101

Chapter 1

Introduction

1.1 Background

Recent progress in the information and communication technologies, such as the wide spread of smart devices and the development of the Internet of Things (IoT), have caused explosive increase in mobile data traffic [1]. Everything is connected to the network, and the information derived from those things yields the convenience and creates new values in our lives. In such a situation, demands for the efficiency and immediacy in the information collection have tremendously been growing. Since the larger capacity and wider bandwidth of the data transmission are required to meet the demands, high-frequency devices supporting the data transmission need to be enhanced in the power capability and the operation frequency. Meanwhile, transmitting, processing, and storing such enormous data are accompanied by the huge consumption of the electrical power. From the viewpoint of the global environmental sustainability, the international community has been required urgent actions for reduction of the greenhouse-gas emission including the energy saving [2]. It is hence crucially important to improve the efficiency in the high-frequency devices for data transmission and power devices for power conversion.

To date, silicon (Si)-based devices have dominantly been used for both high frequency and power conversion applications. Their performance has been improved steadily over the last several decades owing to the highly sophisticated processing technologies. However, the performance is approaching to the theoretical limit originating from the material properties and thus faces a difficulty in satisfying the continuous requirement for the further improvement. Then the wide bandgap semiconductors such as gallium nitride (GaN) and silicon carbide (SiC) have emerged as the next generation materials for the high-frequency and high-power devices because of their superior material properties. Figure 1.1 shows the potential applications of the wide bandgap semiconductors categorized by the operating frequency and the handling power capacity [3]. In particular, GaN has much attention as high-frequency and high-speed devices owing to the high mobility and the high saturated drift velocity.

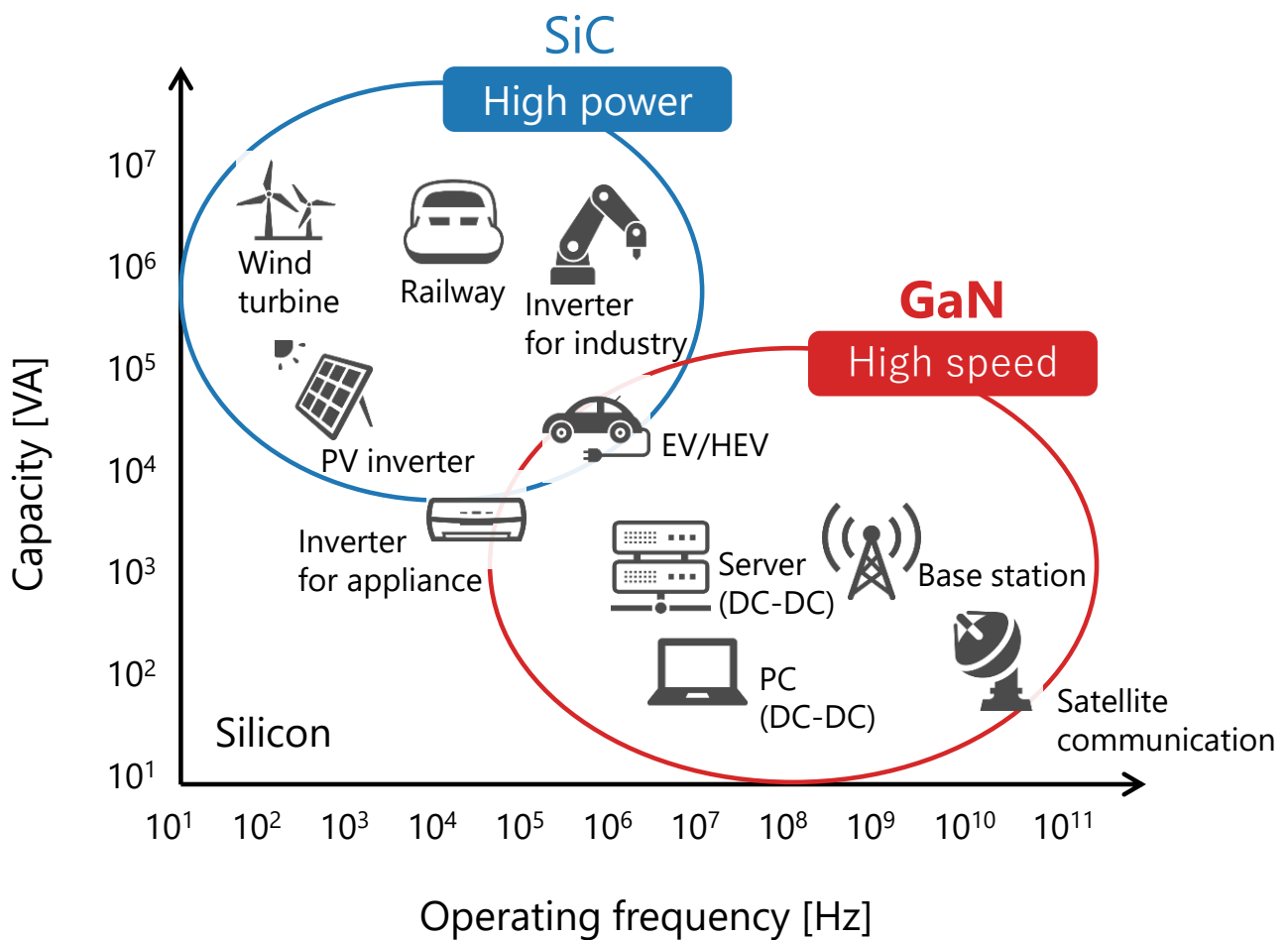


Figure 1.1: Potential applications of the wide gap semiconductors [3].

1.2 III-Nitride Semiconductors

1.2.1 Properties of III-Nitride Semiconductors

The III-nitride semiconductors dealt with in this thesis are GaN, aluminum nitride (AlN), indium nitride (InN), and their ternary or quaternary alloys. These compound semiconductors and alloys, composed of the group III elements of gallium (Ga), aluminum (Al) or indium (In), and the group V element of nitrogen (N), can crystallize in three different structures, that is wurtzite, zinc-blende, and rock-salt. Among these structures, the thermodynamically stable structure under ambient conditions is wurtzite [4]. The III-nitride semiconductors with the wurtzite structure have direct bandgaps, ranging from 0.7 to 6.2 eV [5–9]. Figure 1.2 shows the bandgap energy plotted as a function of the basal-plane lattice constant for the III-nitride semiconductors. The material properties including the bandgap energy and lattice constants can be designed and controlled by changing the composition of the ternary or quaternary alloys, which is one of the most important features of the III-nitride semiconductors. Because of such wide controllability in the bandgap energy and accordingly in the emission wavelength, III-nitride semiconductors have first been developed for optical applications. Since the GaN-based blue-violet laser diodes as well as blue and green light-emitting diodes (LEDs) were commercialized in the mid-1990s [10–12], the GaN-based optical devices have been widely used around the world and they are indispensable in our lives at present.

Besides the optical applications, III-nitride semiconductors have attracted much attention as the emerging electronic devices for high-frequency and high-power applications owing to their superior physical properties. The major physical properties of GaN are shown in Table 1.1, together with those of Si, GaAs, and 4H-SiC for comparison [13–19]. Since the III-nitride semiconductors are composed of Ga, Al, or/and In with N the atomic radius of which is small, the atomic bonds between the anion and the cation are strong and the lattice constants are thereby smaller than the conventional semiconductors. This strength of the atomic bonds results in the robustness in the thermal, chemical, and mechanical points of view. For example, the bandgap energy of GaN is as large as 3.39 eV at room temperature and the breakdown field is over 3×10^6 V/cm, about ten times larger than Si and GaAs [20]. Although the electron mobility of GaN is smaller than that of GaAs, the saturated drift velocity is 2.7×10^7 cm/s which is 30 % larger than that of GaAs [21].

To predict and compare the ultimate performance of devices fabricated with different materials, several figures of merit have been proposed. Table 1.2 summarizes such figures of merit for GaN, Si, GaAs, and 4H-SiC, where each value is normalized by that of Si. Johnson's figure of merit (JFOM) related to the high-frequency and high-power capability of devices is defined by the following equation [22]:

$$\text{JFOM} = \frac{E_B^2 v_{\text{sat}}^2}{4\pi^2}, \quad (1.1)$$

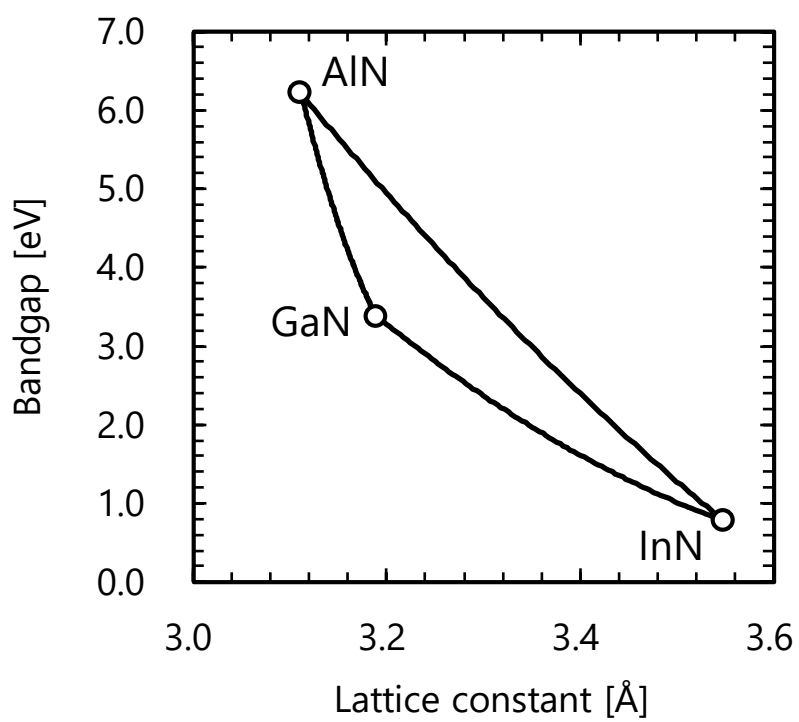


Figure 1.2: Bandgap energy of III-nitride semiconductors as a function of the basal-plane lattice constant.

Table 1.1: Physical properties of GaN, Si, GaAs, and 4H-SiC [13–19].

			GaN	Si	GaAs	4H-SiC
Bandgap	E_g	[eV]	3.42	1.12	1.42	3.26
Electron mobility	μ	[cm ² /(V·s)]	1400	1500	8500	1200
Breakdown field	E_B	[V/cm]	3.3×10^6	3.0×10^5	4.0×10^5	3.0×10^6
Saturation drift velocity	v_{sat}	[cm/s]	2.7×10^7	1.0×10^7	2.0×10^7	2.2×10^7
Relative dielectric constant	ϵ_s		8.9	11.9	12.8	9.7
Thermal conductivity	κ	[W/(cm·K)]	1.3	1.5	0.5	4.9

Table 1.2: Figures of merit for GaN, Si, GaAs, and 4H-SiC. Each value is normalized by that of Si.

	GaN	Si	GaAs	4H-SiC
JFOM	68	1	6	41
KFOM	2	1	0.5	5
BFOM	929	1	14	652
BHFOM	113	1	10	80

where E_B and v_{sat} are the breakdown field and the saturated drift velocity. Keyes's figure of merit (KFOM) was proposed from the viewpoint of the thermal limitation in the high-speed switching operations and defined by [23]

$$\text{KFOM} = \kappa \sqrt{\frac{c v_{\text{sat}}}{4\pi \varepsilon_s}}, \quad (1.2)$$

where κ , ε_s , and c are the thermal conductivity, the permittivity, and the speed of light in vacuum, respectively. Baliga's figures of merit for power devices in low-frequency (BFOM) and high-frequency (BHFFOM) applications are related to the conductive loss and the switching loss in the switching operations, and given by [24, 25]

$$\text{BFOM} = \varepsilon_s \mu E_B^3, \quad (1.3)$$

$$\text{BHFFOM} = \mu E_B^2, \quad (1.4)$$

where μ is the mobility. The thermal conductivity of III-nitride semiconductors are in the same order as that of Si, while the saturated drift velocity is higher than Si and thus the KFOM is still higher than Si. Moreover, the III-nitride semiconductors exhibit other figures of merit higher than Si and GaAs by orders of magnitude, indicating their great potential for high-frequency and high-power applications.

1.2.2 Polarization Effects

In addition to the superior physical properties of III-nitride semiconductors, the polarization effect is their distinct feature compared with other conventional semiconductors. Under the atmospheric pressure, the stable structure of III-nitride semiconductors is wurtzite, a hexagonal crystal structure defined by the edge length a of the basal hexagon, the height c of the hexagonal prism, and internal parameter u defined as the anion-cation bond length along the [0001] axis in units of c , as shown in Fig. 1.3. Due to the large difference in the electronegativity between the group III atom and the nitrogen atom, the atomic bond in the III-nitride semiconductor has large ionicity, causing the polarization from the negatively-charged nitrogen atom to the positively-charged group III atom. If the tetrahedron composing the wurtzite structure is ideal, all components of the polarization caused by pairs of atoms cancel one another out. However, when the atom is displaced with an external stress, the resultant polarization emerges externally, which is called the piezoelectric polarization.

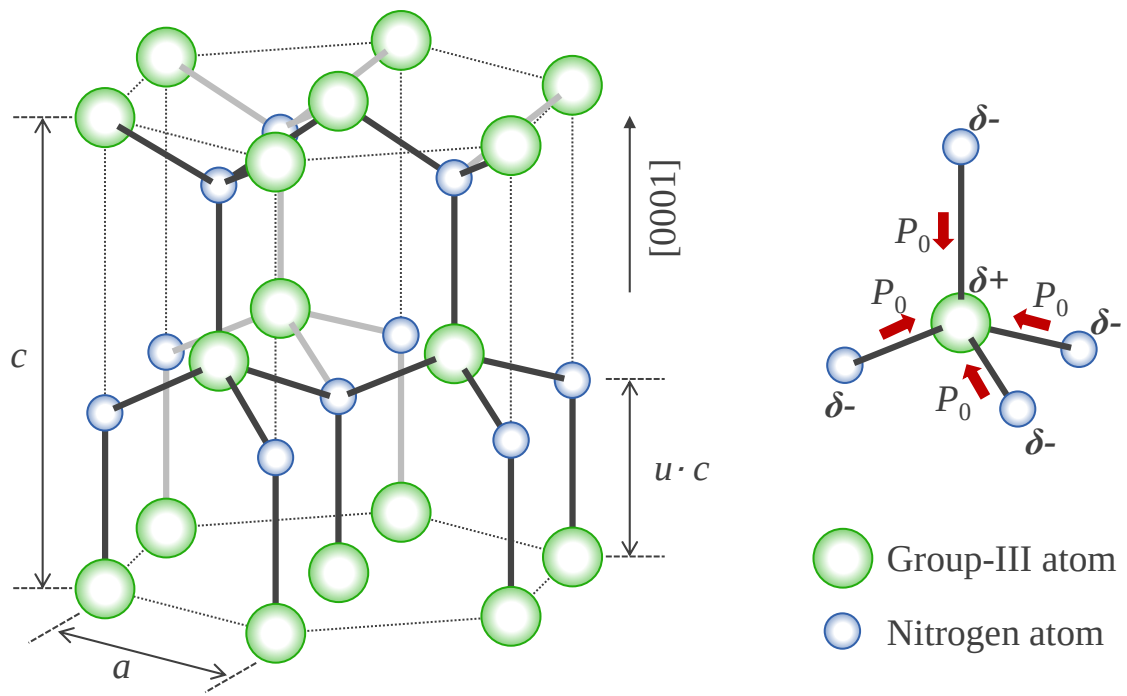


Figure 1.3: Schematic drawing of the crystal structure of III-nitride semiconductors with wurtzite structures and polarization vectors.

The piezoelectric polarization in the wurtzite structure is given by [26]

$$\begin{pmatrix} P_x \\ P_y \\ P_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{yz} \\ \varepsilon_{zx} \\ \varepsilon_{xy} \end{pmatrix}, \quad (1.5)$$

where P_i , e_{ij} and ε_{ij} represent the polarization, the piezoelectric coefficient and strain, respectively. In general, the heteroepitaxial layers grown along the [0001] direction undergo the biaxial in-plane stress due to the differences of lattice constants and thermal expansion coefficients. In this case, $\varepsilon_{yz} = \varepsilon_{zx} = \varepsilon_{xy} = 0$ can be assumed and Eq. (1.5) is thus reduced to

$$P_z = e_{31}(\varepsilon_{xx} + \varepsilon_{yy}) + e_{33}\varepsilon_{zz}. \quad (1.6)$$

The in-plane (ε_{xx} , ε_{yy}) and out-of-plane (ε_{zz}) strains are given by

$$\varepsilon_{xx} = \varepsilon_{yy} = \frac{a - a_0}{a_0}, \quad (1.7)$$

$$\varepsilon_{zz} = \frac{c - c_0}{c_0}. \quad (1.8)$$

Here, a_0 and c_0 represent the relaxed (equilibrium) in-plane and out-of-plane lattice constants, while a and c represent the strained ones. The relationship between stress and strain is expressed as

$$\begin{pmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{xy} \\ \sigma_{yz} \\ \sigma_{zx} \end{pmatrix} = \begin{pmatrix} C_{11} & C_{12} & C_{13} & 0 & 0 & 0 \\ C_{12} & C_{11} & C_{13} & 0 & 0 & 0 \\ C_{13} & C_{13} & C_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{C_{11}-C_{12}}{2} \end{pmatrix} \begin{pmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{xy} \\ \varepsilon_{yz} \\ \varepsilon_{zx} \end{pmatrix}, \quad (1.9)$$

where σ_{ij} , C_{ij} and ε_{ij} represent stress, the elastic coefficients and strain, respectively. In case that only a biaxial stress is present, the stress related to the [0001] direction (z -direction) is negligible and $\sigma_{zz} = \sigma_{yz} = \sigma_{zx} = 0$. Then, from Eq. (1.9), the following equation is obtained:

$$\varepsilon_{zz} = -\frac{C_{13}}{C_{33}}(\varepsilon_{xx} + \varepsilon_{yy}). \quad (1.10)$$

Substituting Eq. (1.10) into Eq. (1.6) result in

$$P_z = 2(e_{31} - \frac{C_{13}}{C_{33}}e_{33})\epsilon_{xx}. \quad (1.11)$$

The piezoelectric polarization thus emerges depending on the strain along the [0001] axis induced by the in-plane stress.

While the lattice constant ratio c_0/a_0 and the internal parameter u for the ideal wurzite are $\sqrt{8/3} \approx 1.633$ and 0.375, the actual III-nitride crystals exhibit the smaller c_0/a_0 and the larger u in equilibrium as summarized in Table. 1.3 [27–30]. These discrepancies indicate that the actual III-nitride crystals are compressed along the [0001] axis and/or stretched along the in-plane directions even in equilibrium, causing the resultant polarization along the [000 $\bar{1}$] direction. Induced without the external stress, this polarization is called the spontaneous polarization. The values of the spontaneous polarization of AlN, GaN, and InN are reported as -0.081 , -0.029 , and -0.032 C/m², respectively [27], approximately ten times larger than those of other III-V semiconductors [31, 32]. The sum of the spontaneous and piezoelectric polarization charges emerge at the heterojunctions in III-nitride semiconductors.

1.3 III-Nitride Heterojunction Field-Effect Transistors (HFETs)

Owing to the strong polarization effect at the heterojunctions in III-nitride semiconductors, a high density of the sheet carriers what is called a two-dimensional electron gas (2DEG) is induced at the heterointerface even without the intentional impurity doping. The device utilizing the sheet carriers as the channel is the heterojunction field-effect transistor (HFET), the schematic cross section of which is shown in Fig. 1.4. Owing to large conduction band discontinuity and large polarization charges, the density of the induced 2DEG exceeds 10^{13} cm⁻² [33]. In addition, since the mobile carriers and the polarization charges are spatially separated, the ionized impurity scattering is almost eliminated, which results in the higher mobility at the heterointerface than that in the bulk. As a result of these high carrier density and high mobility, AlGaN/GaN HFETs with the Al contents of around 0.2 are expected to exhibit the high drain current density and the low parasitic resistance at the high operation frequency.

After the first observation of the 2DEG with a carrier density of 1×10^{11} cm⁻² and a mobility of 800 cm²/(V·s) at room temperature in the AlGaN/GaN heterojunction was reported in 1991 [34], the first AlGaN/GaN HFET was demonstrated in 1993 [35]. Since then, the AlGaN/GaN HFETs have extensively been investigated for high-frequency applications owing to their material properties suitable for the high speed operation such as the high mobility and high saturated drift velocity [36–41]. By downscaling of the gate length to 20 nm, GaN based HFETs with a maximum current gain cutoff frequency (f_T) of 454 GHz and that with a maximum power gain cutoff frequency (f_{max}) of

Table 1.3: Structural parameters for AlN, GaN and InN [27–30].

	AlN	GaN	InN
a_0 [Å]	3.111	3.189	3.548
c_0 [Å]	4.981	5.185	5.760
c_0/a_0	1.601	1.626	1.623
u_0	0.380	0.376	0.377

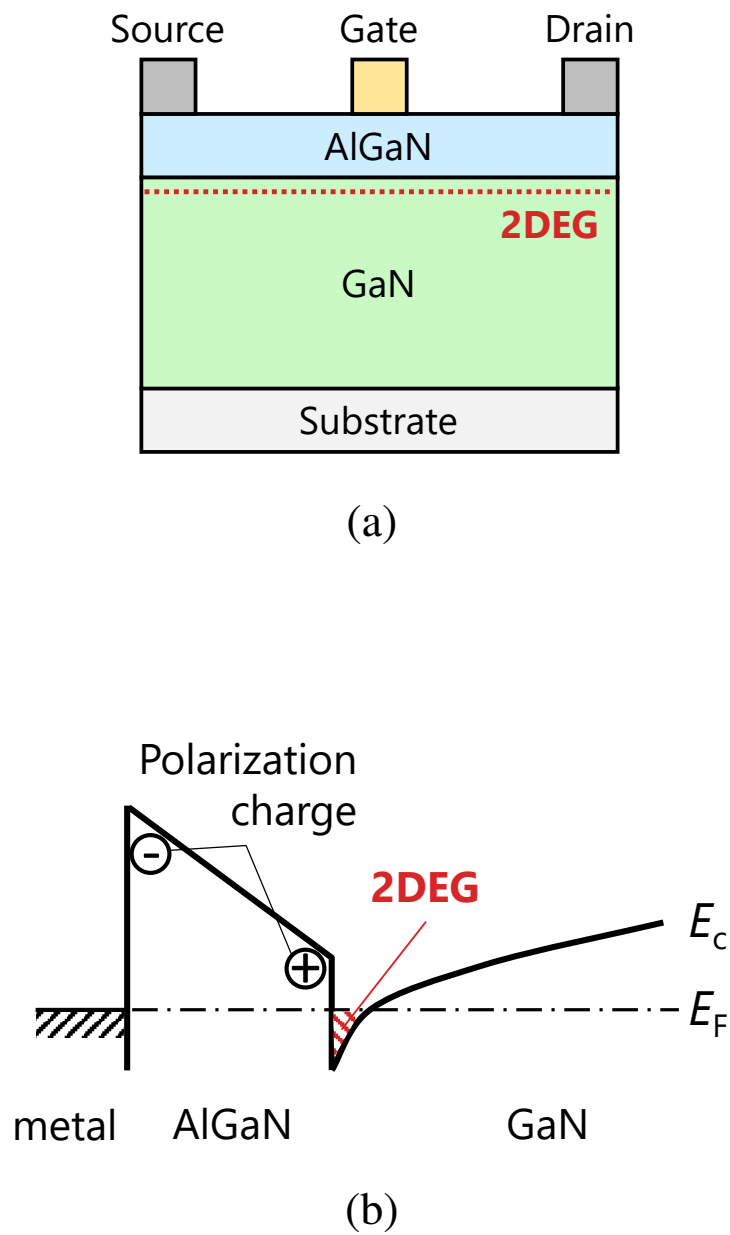


Figure 1.4: (a) Schematic cross section of an AlGaN/GaN HFET and (b) Schematic band diagram of an AlGaN/GaN HFET under the gate region.

582 GHz were demonstrated [42, 43]. As for the large signal performance, introduction of Si_xN passivation and adoption of a field plate had significant impacts on increasing the output power density [44–46]. Combining these technologies, the power density as high as 40 W/mm at 4 GHz was reported [47].

At present, AlGaIn/GaN HFETs mainly fabricated on SiC substrates, taking advantage of better crystal quality of GaN on SiC and high thermal conductivity of SiC, have been put into practical use for the power amplifiers used in the cellular base stations and satellite communication systems. As for the high-frequency applications, further improvement in the operation frequency is required for the future communication systems. Shortening the gate length is effective to achieve the higher frequency operation, which requires simultaneous thinning of the barrier layers to avoid the short channel effect. However, thinning the barrier layers results in the decrease of sheet carrier density leading to the increased parasitic resistance, and thus thin barrier layers with more polarization charges are required. Thus control of the polarization charge at the heterostructure is important to improve the device performance.

Meanwhile, AlGaIn/GaN HFETs for high-power switching applications have also extensively been investigated [48–51]. Since the cost-effectiveness is especially required for these applications, the progress in the crystal-growth technology of GaN on Si substrates has greatly promoted the research in this field [52–54]. The normally-off operations of the devices for high-power switching applications are strongly required from the viewpoint of the safe system operation. Among the various structures designed to achieve the normally-off operations, metal-insulator-semiconductor (MIS) gate structures have attracted much attention, since they reduce the gate leakage current and enable the wider gate-voltage-swing, which is indispensable for fast switching operation [55]. The MIS gate structure is required also for the HFETs for high-frequency applications which suffer from severe gate leakage current, leading to the reduction of the gain and the efficiency [56]. However, the instability of the gate characteristics, such as the threshold voltage shift and hysteresis in the transfer characteristics, is often observed in the MIS gate structures [57], which would be attributed to the interface charges at the MIS interface. To achieve practical AlGaIn/GaN MIS-HFETs, this instability is the technical issues to be solved.

1.4 Outline of Thesis

Since the performance of the AlGaIn/GaN HFETs is profoundly affected by the interface charges such as the polarization charges at the heterointerface and the charges at the MIS interface, it is critically important to control those interface charges through designing and fabricating the devices for improvement in the performance of the AlGaIn/GaN HFETs. Inadequate control of those interface charges causes the undesired characteristics such as the increase of the parasitic resistance at the heterointerface and the unstable operation in the devices with the MIS gate structures, as summarized

in the Fig. 1.5.

Intensive investigation on controlling the polarization charges in AlGaIn/GaN heterostructures was carried out around 2000, enabling control of sheet carrier density of AlGaIn/GaN HFETs by changing Al mole fractions and thickness of AlGaIn barrier layers [33,58,59]. These studies however has focused on control of sheet carrier density and there still remain technical issues caused by the polarization charges such as generation of depletion layer at the heterointerface which increases parasitic resistance [60].

As for the AlGaIn/GaN MIS-HFETs, one of the most critical issues in AlGaIn/GaN MIS-HFETs is the instability of the gate characteristics caused by the interface charges at the MIS interfaces as described in Section 1.3. Since the first AlGaIn/GaN MIS-HFET using a SiO₂ gate insulator was demonstrated [61], various kinds of insulators such as SiN_x [62,63], Al₂O₃ [64,65] and HfO [66] have been investigated as a gate insulator, leading to successful reduction of gate leakage current. In addition, it has been reported that radical treatment with nitrogen plasma prior to insulator deposition effectively removes surface contaminations and native oxides on AlGaIn and GaN surfaces, leading to reduction of interface state density at MIS interfaces [67,68]. Despite these intensive studies on GaN-based MIS interfaces, AlGaIn/GaN MIS-HFETs with sufficiently stable gate characteristics to be applied to practical use have not been achieved at present. Since the methodology to control interface charges has not established, it is necessary to clarify their origins and effects induced by the fabrication processes.

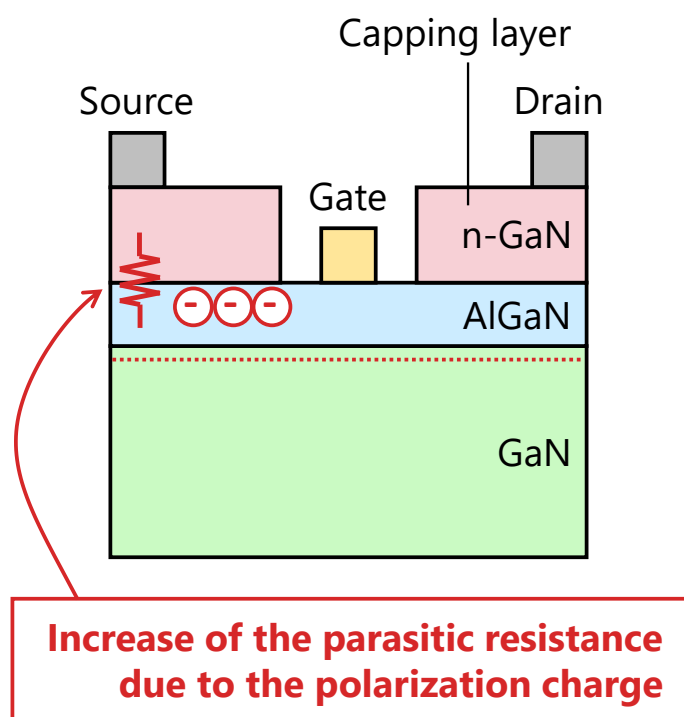
In this thesis, effects of the interface charges on the electrical characteristics of AlGaIn/GaN HFETs were investigated to obtain the technical direction to control the interface charges and thereby improve the performance in the AlGaIn/GaN HFETs. The outline of this thesis is summarized in Fig. 1.6.

Chapter 2 describes effects of the polarization charges at the heterojunctions on the parasitic resistance in the AlGaIn/GaN HFETs. Importance of the polarization engineering is discussed and thereby reduction of the source resistance is demonstrated.

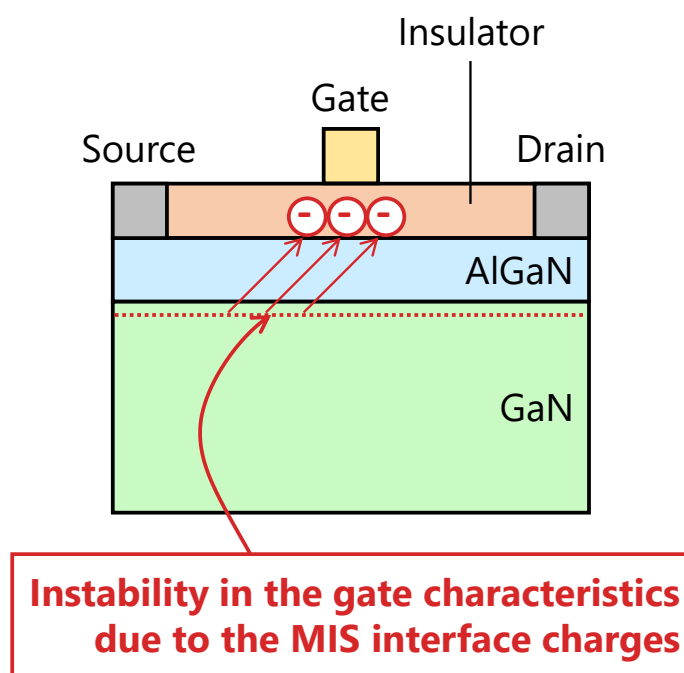
Chapter 3 presents improvement of the device performance in AlGaIn/GaN HFETs in terms of the output power and linear gain based on the analysis of the effects of the field plates. The optimized design of the field plate successfully suppresses the undesired variation in the parasitic capacitance and thus the output impedance, resulting in the high output power with high gain.

Chapter 4 describes effects of the device fabrication processes on the Al₂O₃/AlGaIn MIS interface properties by characterizing the *C-V* characteristics of the Al₂O₃/AlGaIn/GaN MIS heterojunction diodes, from which the technical direction is derived to achieve the MIS structures exhibiting the stable characteristics mandatory for application of the MIS devices to the practical use.

Chapter 5 presents normally-off AlGaIn/GaN MIS-HFETs with stable gate characteristics exhibiting the fast switching performance. Owing to the improved fabrication process based on the results described in Chapter 4, the stability of the gate characteristics was maintained up to the gate voltage of 10 V, high enough to use the devices for practical applications.



(a)



(b)

Figure 1.5: Technical issues on control of the interface charges treated in this thesis, that is (a) polarization charges at the heterointerface and (b) charges at the MIS interface.

The present work is summarized in Chapter 6, including remaining issues and the future work for improving the performance of the AlGaN/GaN HFETs.

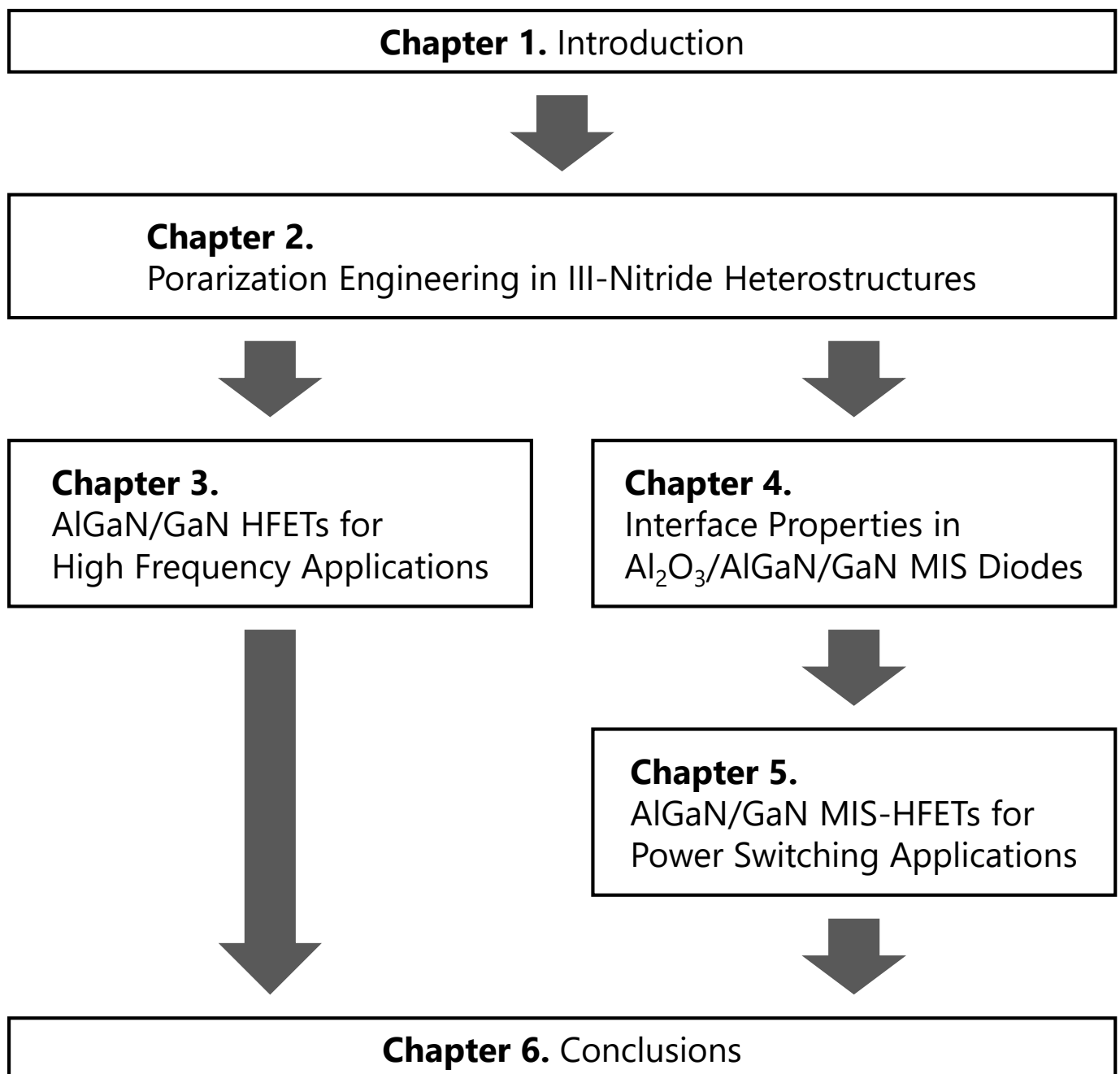


Figure 1.6: Outline of thesis.

References

- [1] Cisco Visual Networking Index: Forecast and Trends, 2017-2022 White Paper, <https://www.cisco.com/>.
- [2] IPCC (Intergovernmental Panel on Climate Change), 2014: *Climate Change 2014: Synthesis Report. Contribution of Working Groups I, II and III to the Fifth Assessment Report of the Intergovernmental Panel on Climate Change* [Core Writing Team, R. K. Pachauri and L. A. Meyer (eds.)]. IPCC, Geneva, Switzerland.
- [3] T. Ueda, S. Takahashi, H. Umimoto, Y. Kanzawa, K. Sawada, and A. Yamasaki, *Panasonic Technical Journal* **61**, 67 (2015).
- [4] H. Morkoç, *Handbook of Nitride Semiconductors and Devices: Materials Properties, Physics and Growth, Volume 1*, (Wiley-VCH Verlag GmbH & Co. KGaA, Germany, 2008).
- [5] H. P. Maruska and J. J. Tietjen, *Appl. Phys. Lett.* **15**, 327 (1969).
- [6] W. M. Yim, E. J. Stofko, P. J. Zanzucchi, J. I. Pankove, M. Ettenberg, and S. L. Gilbert, *J. Appl. Phys.* **44**, 292 (1973).
- [7] O. Ambacher, J. Majewski, C. Miskys, A. Link, M. Hermann, M. Eickhoff, M. Stutzmann, F. Bernardini, V. Fiorentini, V. Tilak, B. Schaff, and L. F. Eastman, *J. Phys.: Condens. Matter.* **14**, 3399 (2002).
- [8] J. Wu, W. Walukiewicz, K. M. Yu, J. W. Ager III, E. E. Haller, H. Lu, W. J. Schaff, Y. Saito, and Y. Nanishi, *Appl. Phys. Lett.* **80**, 3967 (2002).
- [9] J. Wu, W. Walukiewicz, W. Shan, K. M. Yu, J. W. Ager III, S. X. Li, E. E. Haller, H. Lu, and W. J. Schaff, *J. Appl. Phys.* **94**, 4457 (2003).
- [10] S. Nakamura, M. Senoh, and T. Mukai, *Jpn. J. Appl. Phys.* **32**, L8 (1993).
- [11] S. Nakamura, T. Mukai, and M. Senoh, *Appl. Phys. Lett.* **64**, 1687 (1994).
- [12] S. Nakamura and G. Fasol, *The Blue Laser Diode*, (Springer-Verlag, 1997).
- [13] S. Strite and H. Morkoç, *J. Vac. Sci. Technol. B* **10**, 1237 (1992).
- [14] M. N. Yorder, *IEEE Trans. Electron Devices* **43**, 1633 (1996).
- [15] J. B. Casady and R. W. Johnson, *Solid-State Electronics* **39**, 1409 (1996).
- [16] D. C. Look and J. R. Sizelove, *Appl. Phys. Lett.* **79**, 1133 (2001).

- [17] D. Huang, F. Yun, P. Visconti, M. A. Reshchikov, D. Wang, H. Morkoç, D. L. Rode, L. A. Farina, Ç. Kurdak, K. T. Tsen, S. S. Park, and K. Y. Lee, *Solid-State Electron.* **45**, 711 (2001).
- [18] R. Trew, *Proc. IEEE* **90**, 1032 (2002).
- [19] B. E. Foutz, S. K. O’Leary, M. S. Shur, and L. F. Eastman, *J. Appl. Phys.* **85**, 7727 (1999).
- [20] T. P. Chow and M. J. Ghezzo, *MRS Proc.* **423**, 69 (1996).
- [21] U. V. Bhapkar and M. S. Shur, *J. Appl. Phys.* **82**, 1649 (1997).
- [22] E. O. Johnson, *RCA Rev.* **26**, 163 (1965).
- [23] R. W. Keyes, *Proc. IEEE* **60**, 225 (1972).
- [24] B. J. Baliga, *J. Appl. Phys.* **53**, 1759 (1982).
- [25] B. J. Baliga, *IEEE Electron Device Lett.* **10**, 455 (1989).
- [26] J. D. Zook, *Phys. Rev.* **136**, A869 (1964).
- [27] F. Bernardini and V. Fiorenini, *Phys. Rev. B* **56**, R10 024 (1997).
- [28] T. Detchprohm, K. Hiramatsu, K. Itoh, and I. Akasaki, *Jpn. J. Appl. Phys.* **31**, L1454 (1992).
- [29] T. L. Tansley and C. P. Foley, *J. Appl. Phys.* **59**, 3241 (1986).
- [30] D. Nilsson, E. Janzén, and A. Kakanakova-Georgieva, *J. Phys. D: Appl. Phys.* **49**, 175108 (2016).
- [31] A. Belabbes, J. Furthmuller, and F. Bechstedt, *Phys. Rev. B* **87**, 035305 (2013).
- [32] B. Bauer, J. Hubmann, M. Lohr, E. Reiger, D. Bougesrd, and J. Zweck, *Appl. Phys. Lett.* **104**, 211902 (2014).
- [33] I. P. Smorchkova, C. R. Elsass, J. P. Ibbetson, R. Vetury, B. Heying, P. Fini, E. Haus, S. P. DenBaars, J. S. Speck, and U. K. Mishra, *J. Appl. Phys.* **86**, 4520 (1999).
- [34] M. Asif Khan, J. M. Van Hove, J. N. Kuznia, and D. T. Olson, *Appl. Phys. Lett.* **58**, 2408 (1991).
- [35] M. Asif Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, *Appl. Phys. Lett.* **63**, 1214 (1993).
- [36] M. Asif Khan, J. N. Kuznia, D. T. Olson, W. J. Schaff, J. W. Burm, and M. S. Shur, *Appl. Phys. Lett.* **65**, 1121 (1994).
- [37] M. A. Khan, Q. Chen, M. S. Shur, B. T. Dermott, J. A. Higgins, J. Burm, W. Schaff, and L. F. Eastman, *Electronics Lett.* **32**, 357 (1996).

- [38] Y.-F. Wu, B. P. Keller, S. Keller, D. Kapolnek, S. P. DenBaars, and U. K. Mishra, *IEEE Electron Device Lett.* **17**, 455 (1996).
- [39] M. Asif Khan, Q. Chen, Michael S. Shur, B. T. Dermott, J. A. Higgins, J. Burm, W. J. Schaff, and L. F. Eastman, *IEEE Electron Device Lett.* **17**, 584 (1996).
- [40] G. J. Sullivan, M. Y. Chen, J. A. Higgins, J. W. Yang, Q. Chen, R. L. Pierson, and B. T. McDermott, *IEEE Electron Device Lett.* **19**, 198 (1998).
- [41] S. T. Sheppard, K. Doverspike, W. L. Pribble, S. T. Allen, J. W. Palmour, L. T. Kehias, and T. J. Jenkins, *IEEE Electron Device Lett.* **20**, 161 (1999).
- [42] K. Shinohara, D. C. Regan, Y. Tang, A. L. Corrion, D. F. Brown, J. C. Wong, J. F. Robinson, H. H. Fung, A. Schmitz, T. C. Oh, S. J. Kim, P. S. Chen, R. G. Nagele, A. D. Margomenos, and M. Micovic, *IEEE Trans. Electron Devices* **60**, 2982 (2013).
- [43] Y. Tang, K. Shinohara, D. Regan, A. Corrion, D. Brown, J. Wong, A. Schmitz, H. Fung, S. Kim, and M. Micovic, *IEEE Electron Device Lett.* **36**, 549 (2015).
- [44] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, *IEEE Electron Device Lett.* **21**, 268 (2000).
- [45] Y. Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue, and M. Kuzuhara, *IEEE Electron Device Lett.* **24**, 289 (2003).
- [46] A. Chini, D. Buttari, R. Coffie, S. Heikman, S. Keller, and U. K. Mishra, *Electronics Lett.* **40**, 73 (2004).
- [47] Y.-F. Wu, M. Moore, A. Saxler, T. Wisleder, and P. Parikh, *Proc. Device Research Conf.*, 2006, p. 151.
- [48] N.-Q. Zhang, B. Moran, S. P. DenBaars, U. K. Mishra, X. W. Wang, and T. P. Ma, *Phys. Stat. Sol. (a)* **188**, 213 (2001).
- [49] W. Saito, Y. Tanaka, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura, and H. Ohashi, *IEEE Trans. Electron Devices* **50**, 2528 (2003).
- [50] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. P. DenBaars, and M. K. Mishra, *IEEE Electron Device Lett.* **27**, 713 (2006).
- [51] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, and D. Ueda, *IEEE Trans. Electron Devices* **54**, 3393 (2007).

- [52] H. Ishikawa, G.-Y. Zhao, N. Nakada, T. Egawa, T. Jimbo, and M. Umeno, *Jpn. J. Appl. Phys.* **38**, L492 (1999).
- [53] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda, *IEEE Trans. Electron Devices* **60**, 3053 (2013).
- [54] K. J. Chen, O. Häberlen, A. Lidow, C. L. Tsai, T. Ueda, Y. Uemoto, and Y. Wu, *IEEE Trans. Electron Devices* **64**, 779 (2017).
- [55] T. Hashizume, K. Nishiguchi, S. Kaneki, J. Kuzmìk, and Z. Yatabe, *Mat. Sci. Semicond. Process.* **78**, 85 (2018).
- [56] M. Kanamura, T. Kikkawa, T. Iwai, K. Imanishi, T. Kubo, and K. Joshin, *IEDM Tech. Dig.*, 2005, 572.
- [57] S. Huang, S. Yang, J. Roberts, and K. J. Chen, *Jpn. J. Appl. Phys.* **50**, 110202 (2001).
- [58] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, *J. Appl. Phys.* **85**, 3222 (1999).
- [59] L. Hsu and W. Walukiewicz, *J. Appl. Phys.* **89**, 1783 (2001).
- [60] M. Kanamura, T. Kikkawa, N. Adachi, T. Kimura, S. Yokogawa, M. Nagahara, N. Hara, and K. Joshin, *Ext. Abstr. Solid State Devices and Materials*, 2003, p. 916.
- [61] M. A. Khan, X. Hu, G. Sumin, A. Lunev, J. Yang, R. Gaska, and M. S. Shur, *IEEE Electron Device Lett.* **21**, 63 (2000).
- [62] E. M. Chumbes, J. A. Smart, T. Prunty, and J. R. Shealy, *IEDM Tech. Dig.*, 2000, p. 385.
- [63] X. Hu, A. Koudymov, G. Simin, J. Yang, M. A. Khan, A. Tarakji, M. S. Shur, and R. Gaska, *Appl. Phys. Lett.* **79**, 2832 (2001).
- [64] S. Ootomo, T. Hashizume, and H. Hasegawa, *Phys. Stat. Sol. (c)* **0**, 90 (2002).
- [65] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Hwang, *Appl. Phys. Lett.* **86**, 063501 (2005).
- [66] A. Kawano, S. Kishimoto, Y. Ohno, K. Maezawa, T. Mizutani, H. Ueno, T. Ueda, and T. Tanaka, *Phys. Stat. Sol. (c)* **4**, 2700 (2007).
- [67] J. Son, V. Chobpattana, B. M. McSkimming, and S. Stemmer, *J. Vac. Sci. Technol. A* **33**, 020602 (2015).
- [68] S. Liu, S. Yang, Z. Tang, Q. Jiang, C. Liu, M. Wang, B. Shen, and K. J. Chen, *Appl. Phys. Lett.* **106**, 051605 (2015).

Chapter 2

Polarization Engineering in III-Nitride Heterostructures

2.1 Introduction

One of the most notable features in the III-nitride semiconductors is the polarization effects. The wurtzite III-nitride crystals lack the center of inversion symmetry, exhibiting piezoelectric effects along the [0001] axis [1]. Piezoelectric coefficients in III-nitride semiconductors are almost an order of magnitude larger than in other conventional III-V semiconductors [1, 2]. The spontaneous and strain-induced piezoelectric polarization charges strongly affect the device operations. In the devices with the heterojunctions such as heterojunction field-effect transistors (HFETs) where the heterointerface and strain are present, the two-dimensional electron gas (2DEG) with the sheet carrier density of 10^{13} cm^{-2} or higher is achieved at the heterojunctions without intentional impurity doping. The mobile carrier in the 2DEG is spatially separated from the polarization charges, leading to high mobility. This sheet carriers with a high density together with high mobility makes these materials attractive for high power RF amplifiers [3, 4], low noise amplifiers [5, 6] and high power switches [7].

On the other hand, such strong effects of the polarization charges on the device performance must be taken into consideration in the designing of the heterostructures. For instance, to control the threshold voltage of HFETs, precise control of the polarization at the heterojunction between the barrier and channel layers are required. In addition, since the polarization is dependent on the polarity of the crystal, undesired effects on the device performance, such as increase of parasitic resistance at the heterojunctions due to the depletion induced by the polarization charges, occurs depending on a layer sequence in the heterostructures [8]. Although there are several reports on the control of the sheet carrier density by designing the barrier layers [9–11], the drawbacks due to the polarization charges have rarely been reported. In this chapter, the effects of the polarization charges at the heterojunctions on the electric characteristics, particularly the parasitic resistance, are examined and its improvement by the polarization engineering is described.

2.2 Polarization in III-Nitride Heterostructures

As described in Chapter 1, in the absence of external fields, the total macroscopic polarization P of a III-nitride semiconductor is the sum of the spontaneous polarization P_{SP} and the piezoelectric polarization P_{PE} given by

$$P = P_{\text{SP}} + P_{\text{PE}}. \quad (2.1)$$

While the microscopic polarization within an identical crystal is shielded from the outside, at an abrupt heterointerface of the III-nitride semiconductors the polarization varies within a bilayer, causing a polarization sheet charge. The sheet charge density σ induced at the heterointerface in a single heterostructure is defined by

$$\sigma = P^{\text{upper}} - P^{\text{lower}} \quad (2.2)$$

$$= (P_{\text{SP}}^{\text{upper}} + P_{\text{PE}}^{\text{upper}}) - (P_{\text{SP}}^{\text{lower}} + P_{\text{PE}}^{\text{lower}}), \quad (2.3)$$

where the superscripts upper and lower refer to the upper and lower layer, respectively [9]. If the polarization induced sheet charge density is positive, free electron will compensate the polarization induced charge, resulting in the formation of 2DEG. Conversely, if the polarization induced charge is negative, free electron will recede from the heterointerface and thus depletion will occur at the interface.

Here, a polarization induced sheet charge density at InAlGaN/GaN heterointerface is calculated. In this case, the bottom layer (GaN) is assumed to be relaxed and thus piezoelectric polarization of bottom layer in Eq. (2.3) is neglected. The spontaneous polarization of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ is given by

$$P_{\text{SP}}^{\text{InAlGa}}(x, y) = xP_{\text{SP}}^{\text{InN}} + yP_{\text{SP}}^{\text{AlN}} + (1 - x - y)P_{\text{SP}}^{\text{GaN}}, \quad (2.4)$$

where $P_{\text{SP}}^{\text{InN}}$, $P_{\text{SP}}^{\text{AlN}}$, and $P_{\text{SP}}^{\text{GaN}}$ are spontaneous polarization of InN, AlN, and GaN, respectively. The piezoelectric polarization is given by

$$P_{\text{PE}}^{\text{InAlGa}}(x, y) = 2(e_{31}(x, y) - \frac{C_{13}(x, y)}{C_{33}(x, y)}e_{33}(x, y))\varepsilon_{xx}, \quad (2.5)$$

$$\varepsilon_{xx} = \frac{a(x, y) - a_0^{\text{GaN}}}{a_0^{\text{GaN}}}, \quad (2.6)$$

where $e_{ij}(x, y)$ and $C_{ij}(x, y)$ is the piezoelectric coefficient and the elastic coefficient, a_0^{GaN} and $a(x, y)$ represent the in-plane lattice constant of GaN and $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$. Derivation of this equation is described in Sec. 1.2.2. Each coefficient in Eqs. (2.5) and (2.6) is derived from the linear interpolation of the values of each material summarized in Tab. 2.1 [12–16]. As a result, the sheet charge density

Table 2.1: Lattice constant, spontaneous polarization, the piezoelectric coefficient, and the elastic coefficient for AlN, GaN and InN [12–17].

			AlN	GaN	InN
Lattice constant	a_0	[Å]	3.111	3.189	3.548
Spontaneous polarization	P_{SP}	[C/m ²]	-0.081	-0.029	-0.032
Piezoelectric coefficient	e_{31}	[C/m ²]	-0.60	-0.49	-0.57
	e_{33}	[C/m ²]	1.46	0.73	0.97
Elastic coefficient	C_{13}	[GPa]	99	106	121
	C_{33}	[GPa]	389	398	182

induced at an $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}/\text{GaN}$ heterojunction is given by

$$\sigma(x, y) = P_{\text{SP}}^{\text{InAlGa}} + P_{\text{PE}}^{\text{InAlGa}} - P_{\text{SP}}^{\text{GaN}}. \quad (2.7)$$

In case that $\sigma(x, y)$ is positive, free electrons compensate this sheet charge at the heterojunction, generating the 2DEG. The maximum 2DEG density induced by the sheet charge is expected to be

$$n_s(x, y) = \frac{\sigma(x, y)}{q} - \left(\frac{\varepsilon_s \varepsilon_0}{d q^2}\right)(q\varphi_b + E_F - \Delta E_C), \quad (2.8)$$

where d is thickness of an $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ layer, ε_s and ε_0 are relative dielectric constant of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}$ and permittivity, $q\varphi_b$ is Schottky barrier height of a gate contact, E_F is the Fermi level with respect to the GaN conduction band edge, and ΔE_C is the conduction discontinuity at the $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}/\text{GaN}$ heterojunction [18]. Calculated sheet carrier densities for AlGaIn/GaN heterojunctions with various AlGaIn thickness as a function of Al mole fraction in AlGaIn layers are shown in Fig. 2.1, indicating that the sheet carrier density can be controlled by both Al mole fraction and thickness of AlGaIn layers.

2.3 Effects of Polarization Charges on Electrical Characteristics

One of the technical obstacles for the improvement of the AlGaIn/GaN HFETs is the high parasitic resistance including high ohmic contact resistance, which should decrease the saturation current and seriously limit the performance of the AlGaIn/GaN HFETs [19–21]. The recessed-gate structure commonly used in the GaAs-based FETs, where highly conductive capping layers are placed between the channel layer and the ohmic contacts to form a recess around the gate, is expected to reduce such parasitic resistance, mainly dominated by the resistance referred to as the source resistance [22, 23]. Applying this technique to the AlGaIn/GaN HFETs, however, raises difficult problems to reduce the source resistance. Because of the cracks in relatively thick and highly Si-doped AlGaIn films, the reduction of the source resistance using the AlGaIn capping layer has been limited. On the other hand, highly doped n-type GaN capping layers suffer from the electron depletion caused by the internal electric field due to the difference of the polarization between the n-type GaN and AlGaIn, which results in the increase of the source resistance [8]. Thus, the polarization engineering by using InAlGaIn alloy capping layers was investigated to reduce the source resistance in the recessed-gate AlGaIn/GaN HFETs. The design of the polarization in InAlGaIn and the analysis of the parasitic resistance in the InAlGaIn/AlGaIn/GaN heterostructures are described.

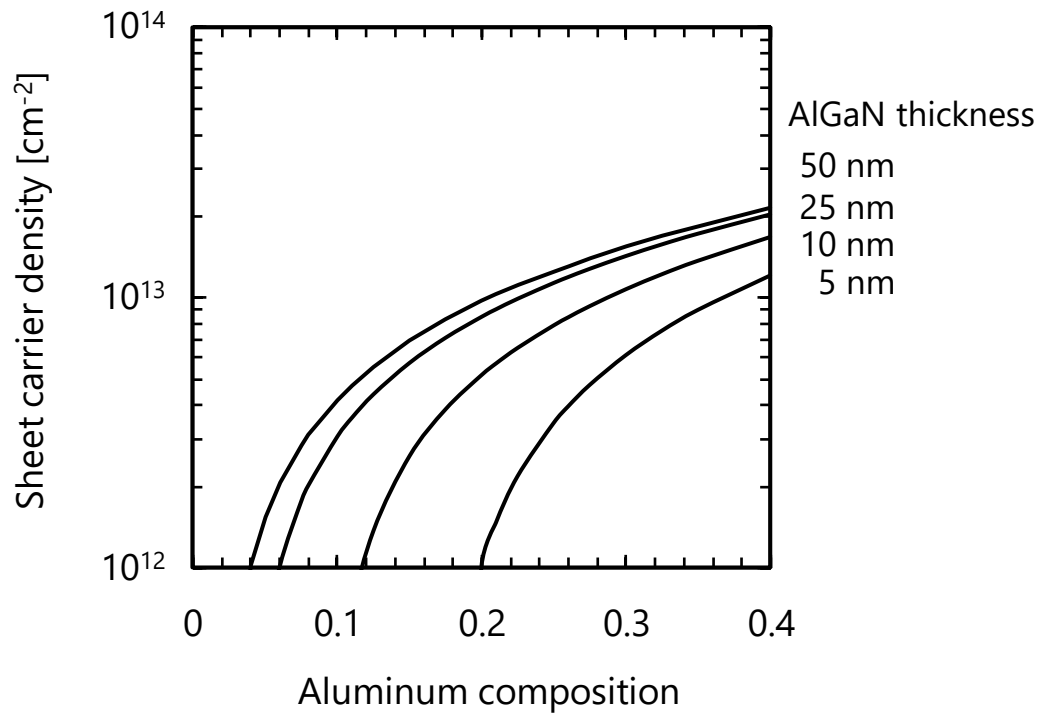


Figure 2.1: Calculated sheet carrier density in AlGaN/GaN heterostructures with various AlGaN thickness as a function of the aluminum composition.

2.3.1 Polarization Engineering by InAlGaN Quaternary Alloy

The requirements for the InAlGaN capping layers to solve the above-mentioned issues are (1) to be lattice matched with GaN serving enough thickness, (2) to have equal or larger polarization than that of the underlying AlGaN barrier layer to eliminate the interfacial depletion and (3) to have larger bandgap than the underlying AlGaN barrier layer to reduce the potential barrier. The lattice constant of the $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ is given by

$$a_{\text{InAlGaN}} = xa_{\text{InN}} + ya_{\text{AlN}} + (1 - x - y)a_{\text{GaN}}, \quad (2.9)$$

where a_{InN} , a_{AlN} , and a_{GaN} are lattice constants of InN, AlN and GaN, respectively [24–30]. The lattice-matching condition is given in case $y = 4.7x$ assuming that a_{InAlGaN} is equal to a_{GaN} .

The polarization of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ is given by the sum of the spontaneous polarization and the piezoelectric polarization expressed by Eqs. (2.4) and (2.5). Fig. 2.2 shows the calculated total polarization of lattice matched InAlGaN layer as a function of the indium composition and that of the $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ layer. As seen in the figure, InAlGaN layer with more than 8 % In composition (37 % Al composition) gives larger polarization than the $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ barrier layer.

The bandgap of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ is given by

$$E_g^{\text{InAlGaN}} = xE_g^{\text{InN}} + yE_g^{\text{AlN}} + (1 - x - y)E_g^{\text{GaN}} - b_{\text{In}}x(1 - x) - b_{\text{Al}}y(1 - y), \quad (2.10)$$

where E_g^{InN} , E_g^{AlN} and E_g^{GaN} represent the bandgap of InN, AlN and GaN, respectively [31–33], b_{In} and b_{Al} represent the bowing parameters for InGaN and AlGaN, respectively. Fig. 2.3 shows the calculated bandgap as a function of the indium composition for the lattice-matching condition. In the calculation, the bowing parameter of 1.0 eV was used for AlGaN [34], while several values were used for InGaN since the reported values ranged from 1.0 to 4.5 eV [35–37]. In case the bowing parameter is 1.0 eV, more than 8 % In composition is required to obtain larger bandgap than that of the $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ barrier layer. The required minimum indium composition increases if the actual bowing parameter is larger than 1.0 eV. Considering the above three conditions, targeted compositions of the lattice-matched InAlGaN layers as the capping layers were set as the indium composition of 8 % and the aluminum composition of 37 %.

2.3.2 Crystal Growth and Device Fabrication

A 2.5 μm -thick undoped GaN channel layer, a 25nm-thick n-type $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ barrier layer ($N_d = 4 \times 10^{18} \text{ cm}^{-3}$) and a 50 nm-thick n-type $\text{In}_{0.09}\text{Al}_{0.32}\text{Ga}_{0.59}\text{N}$ capping layer ($N_d = 9 \times 10^{18} \text{ cm}^{-3}$) were grown in order on the sapphire (0001) substrates by the metalorganic chemical vapor deposition (MOCVD). Trimethylgallium (TMG), trimethylaluminium (TMA) and trimethylindium (TMI) were used as the precursors of group-III material and ammonia was used as the nitrogen source. The

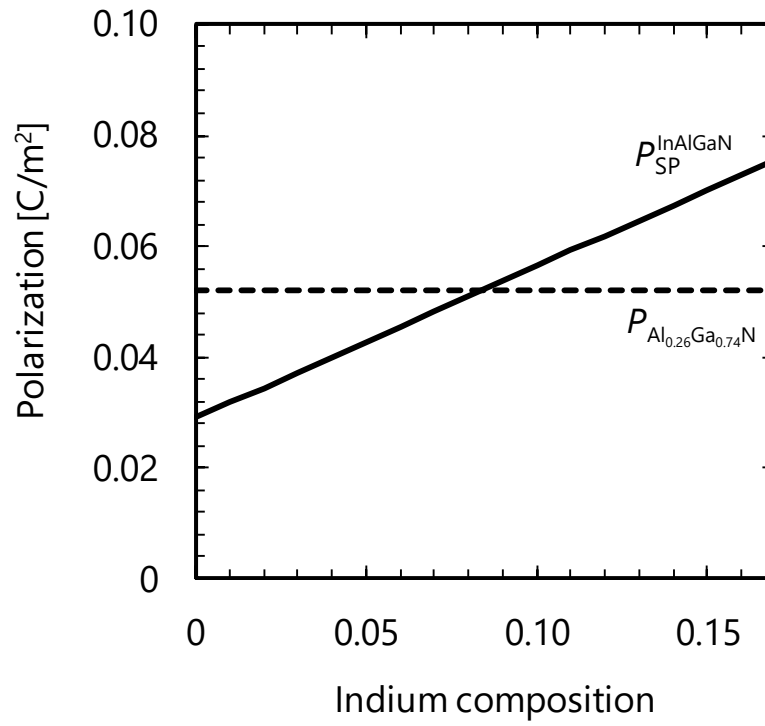


Figure 2.2: Calculated total polarization in lattice-matched InAlGaN as a function of the indium composition.

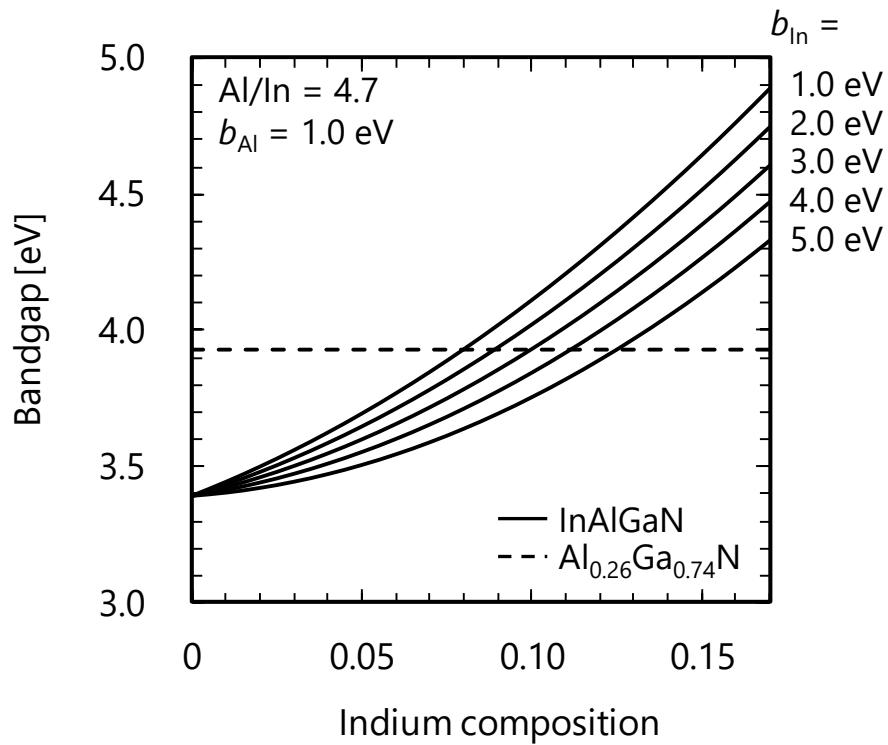


Figure 2.3: Calculated bandgap energies of lattice-matched InAlGaN for various bowing parameters as a function of the indium composition.

compositions of the grown InAlGa_N layers were estimated by both the electron-probe microanalysis and Rutherford backscattering.

Figures 2.4 and 2.5 show the ω - 2θ X-ray diffraction spectra of InAlGa_N/Ga_N heterostructures with various composition and the reciprocal space map of the In_{0.09}Al_{0.32}Ga_{0.59}N/Ga_N heterostructure, respectively. The thickness of InAlGa_N layer of each sample was approximately 150 nm. The In_{0.09}Al_{0.32}Ga_{0.59}N/Ga_N structure exhibits a single peak at the same diffraction angle of Ga_N (36.4°), which indicates that the grown InAlGa_N layer is lattice-matched with the underlying Ga_N layer. The bandgap of InAlGa_N layer measured by cathodeluminescence was 3.46 eV. Thus, the bowing parameter for InGa_N was calculated to be relative large value of 2.3 eV.

The schematic cross section and the cross sectional transmission electron microscope (TEM) images of the fabricated device is shown in Figs. 2.6 and Fig. 2.7, respectively. The sheet resistance (r_{sh}) of the HFET with the InAlGa_N capping layer is $400 \Omega/\square$. The recessed structure was formed on the epitaxial wafer by the inductively coupled plasma (ICP) dry etching, followed by device isolation using selective oxidation [38]. After Ti/Al alloy ohmic electrodes formation, Pd-Si gate electrode was formed in the recessed area by evaporation and lift-off [6]. The gate length (L_g) and the gate-source spacing (L_{sg}) were 1 and $4 \mu\text{m}$, respectively. The width of the recessed area was $5 \mu\text{m}$. The measured drain current-voltage characteristics of the fabricated HFET with the InAlGa_N capping layer are shown in Fig. 2.8. Relatively low source resistance (R_s) of $4.8 \Omega\text{mm}$ and on-state resistance (R_{on}) of $11.6 \Omega\text{mm}$ were obtained.

2.3.3 Analysis of Parasitic Resistance

To analyze in detail the resistive components in the fabricated HFETs, the contact resistance and the sheet resistance were measured by the transfer-length method (TLM) for both recessed and non-recessed structures as shown in Fig. 2.9. The measured sheet resistance and specific contact resistance are denoted as r_{sh} and ρ_c for the non-recessed structure, r_{sh2} and $\rho_{c \text{ 2DEG}}$ for the recessed structure. Table 2.2 summarizes the results. Typical values for HFETs with the conventional Ga_N capping layers are also listed in Table 2.2 for comparison.

As for the contact resistance between the Ti/Al ohmic electrodes and the capping layer (ρ_c), a low value of $1.0 \times 10^{-6} \Omega\text{cm}^2$ was obtained on the InAlGa_N capping layer. This reduction of ρ_c might suggest the larger electron affinity of InAlGa_N than that of Ga_N. Furthermore, the actual specific contact resistance to the 2DEG ($\rho_{c \text{ 2DEG}}$) of the HFET with the InAlGa_N capping layer was $4.7 \times 10^{-5} \Omega\text{cm}^2$, which was one third as low as that of the HFET with the conventional Ga_N capping layer. The suppression of the depletion at the heterojunction interface should lead to effective lowering of the hetero barrier height, resulting in the low contact resistance. The expected band structure is shown in Fig. 2.10, comparing with that of the HFET with the conventional Ga_N capping layer.

To confirm the reduction of the parasitic resistance at the heterojunction, the measured parasitic

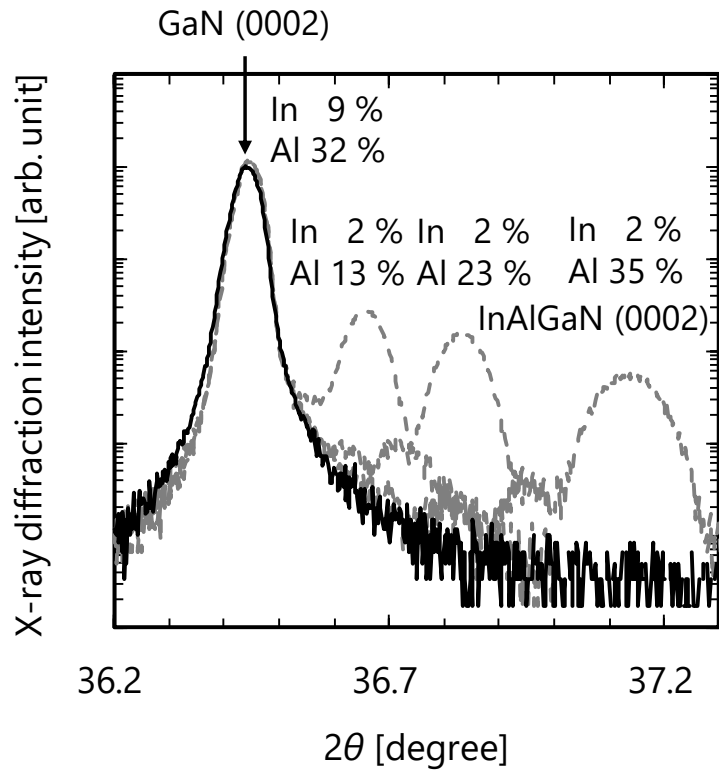


Figure 2.4: X-ray ω - 2θ spectra of InAlGaN/GaN heterostructures with various conditions.

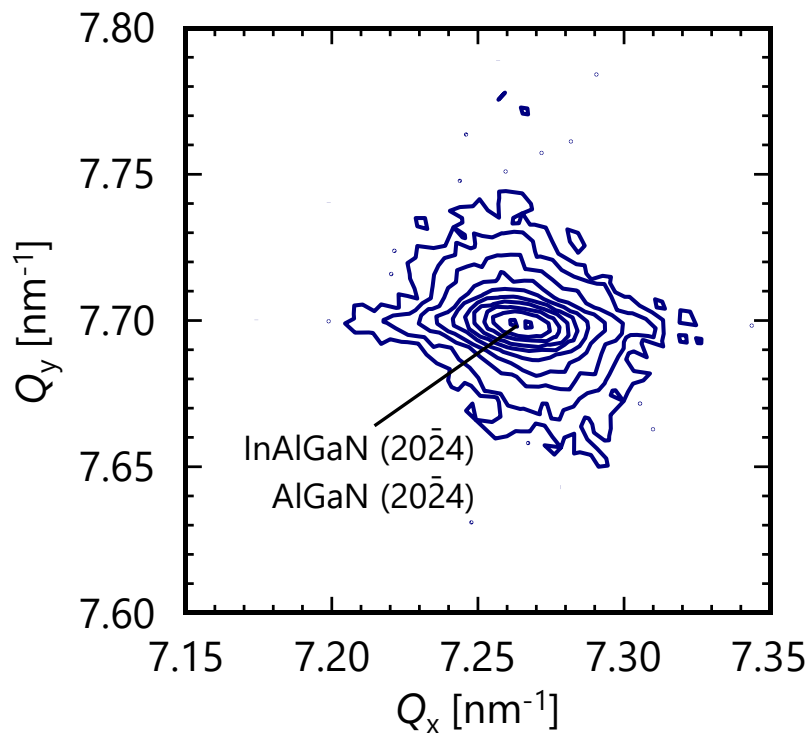


Figure 2.5: Reciprocal space map of the $\text{In}_{0.09}\text{Al}_{0.32}\text{Ga}_{0.59}\text{N}/\text{GaN}$ heterostructure.

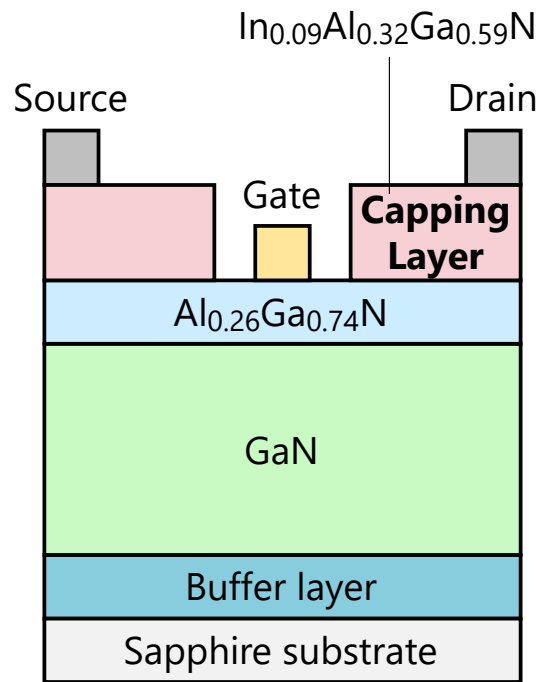


Figure 2.6: Schematic cross section of the fabricated HFET with the InAlGaN capping layers.

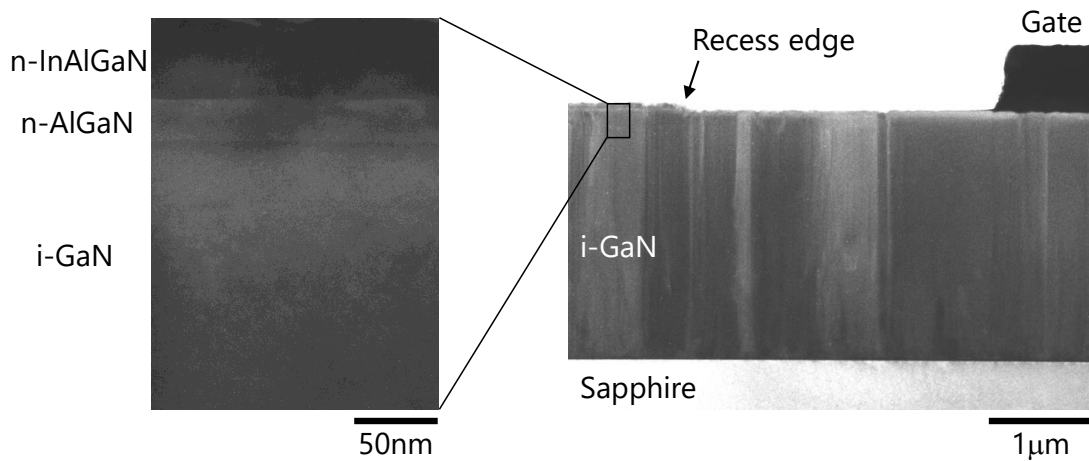


Figure 2.7: Cross-sectional TEM image of the fabricated HFET.

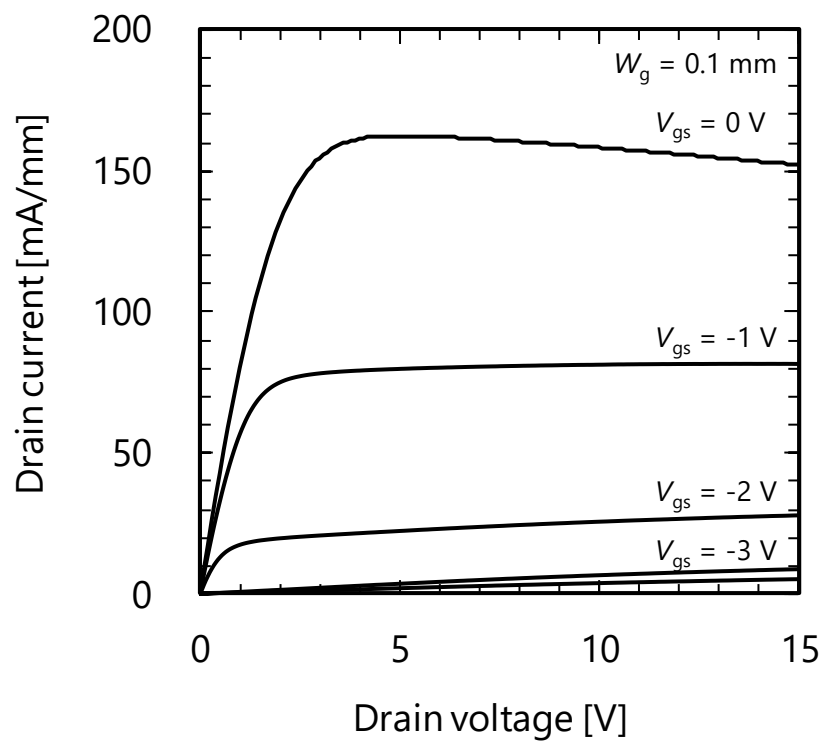


Figure 2.8: Drain current-voltage characteristics of the fabricated HFET with the InAlGaN capping layer.

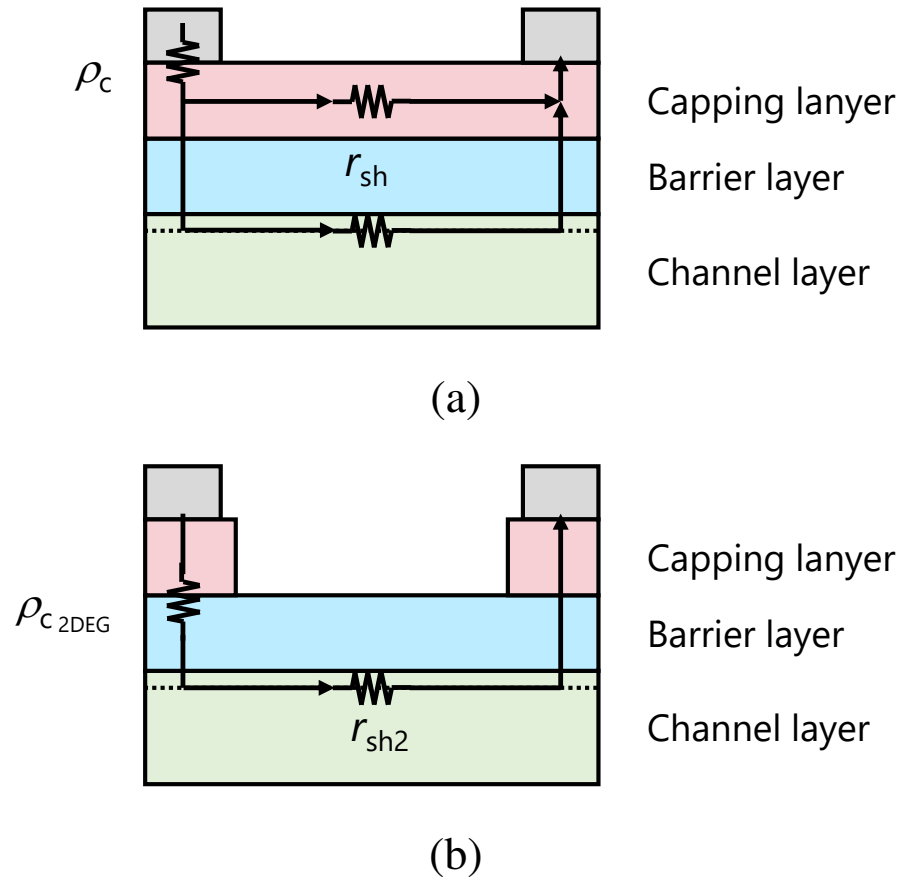


Figure 2.9: (a) Non-recessed and (b) recessed structures for the TLM measurements.

Table 2.2: Measured sheet resistance and specific contact resistance for the non-recessed structure (r_{sh} and ρ_{c}) and for the recessed structure (r_{sh2} and $\rho_{\text{c 2DEG}}$).

	Capping layer	InAlGaN	GaN
Sheet resistance of the whole epitaxial layer	$r_{\text{sh}} [\Omega/\square]$	400	180
Specific contact resistance to a capping layer	$\rho_{\text{c}} [\Omega \text{ cm}^2]$	1.0×10^{-6}	3.2×10^{-6}
Sheet resistance of 2DEG	$r_{\text{s2}} [\Omega/\square]$	550	450
Specific contact resistance to 2DEG	$\rho_{\text{c 2DEG}} [\Omega \text{ cm}^2]$	4.7×10^{-5}	1.4×10^{-4}

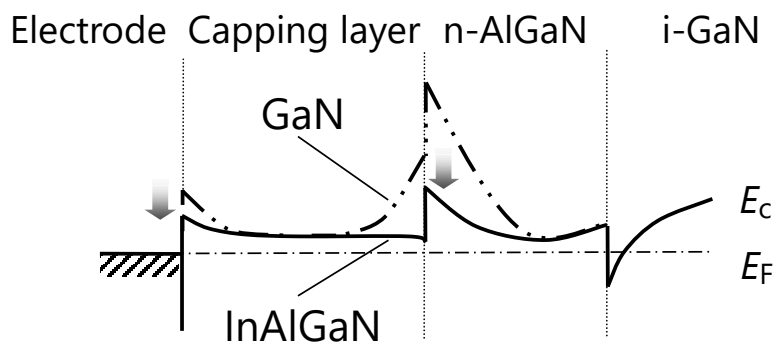


Figure 2.10: Expected band diagram of the HFET with InAlGaN and GaN capping layers.

resistance was analyzed by using the two layer model shown in Fig. 2.11, enabling the separation of the parasitic resistive elements of a FET with a capping layer [39]. In this model, the total resistance between point A and B is given by

$$R_{\text{total}} = \frac{r_{\text{sh1}} r_{\text{sh2}}}{r_{\text{sh1}} + r_{\text{sh2}}} L + \frac{1}{r_{\text{sh1}} + r_{\text{sh2}}} \frac{2r_{\text{sh1}} r_{\text{sh2}} + (r_{\text{sh1}}^2 + r_{\text{sh2}}^2) \cosh kL + (r_{\text{sh1}} + r_{\text{sh2}}) \rho_c k \sinh kL}{k \sinh kL}, \quad (2.11)$$

where

$$k = \sqrt{\frac{r_{\text{sh1}} + r_{\text{sh2}}}{\rho_h}}. \quad (2.12)$$

In these equations, r_{sh1} and r_{sh2} represent the sheet resistance of the capping layer and the 2DEG, respectively, L represents the length between the edge of the electrode and that of the recessed area, and ρ_h is the parasitic resistance at the heterojunction. Actual contact resistance (R_{total}) is expressed with the measured $\rho_{\text{c total}}$ and r_{sh2} in Table 2.2 by the following equation:

$$R_{\text{total}} = \sqrt{\rho_{\text{c 2DEG}} r_{\text{sh2}}}. \quad (2.13)$$

The sheet resistance of the capping layer (r_{sh1}) is calculated with the measured r_{sh2} and r_{sh} by the following equation:

$$r_{\text{sh1}} = \frac{r_{\text{sh2}} r_{\text{sh}}}{r_{\text{sh2}} - r_{\text{sh}}}. \quad (2.14)$$

By using Eq. (2.11), (2.13) and (2.14), R_{total} , r_{sh1} and ρ_h shown in Fig. 2.11 were calculated. The calculated resistance are summarized in Table 2.3. Compared with the GaN capping layer, the InAlGa_N capping layer enables lower ρ_h by a factor of one fifth. The presented sheet resistance of the InAlGa_N capping layer (about 1470 $\Omega/\square$) is more than 8 times higher than that of the GaN capping layer (about 180 $\Omega/\square$). This implies that further reduction of R_{total} is expected by reducing the resistivity of InAlGa_N, which could be realized by optimization of the growth condition. If the sheet resistance of the InAlGa_N capping layer is reduced to the same level with the GaN capping layer, the source resistance of 0.9 Ωmm could be achieved, which is one third as low as the source resistance of the conventional GaN capping layer. Since the measured bowing parameter is larger, resulting in smaller bandgap than expected, more incorporation of In and Al to increase bandgap of InAlGa_N would further reduce the hetero barrier and the source resistance.

2.4 Summary

In this chapter, effects of the polarization charges on the performance of GaN-base devices. To reduce source resistance in AlGa_N/GaN heterostructures, introduction of capping layers using InAlGa_N

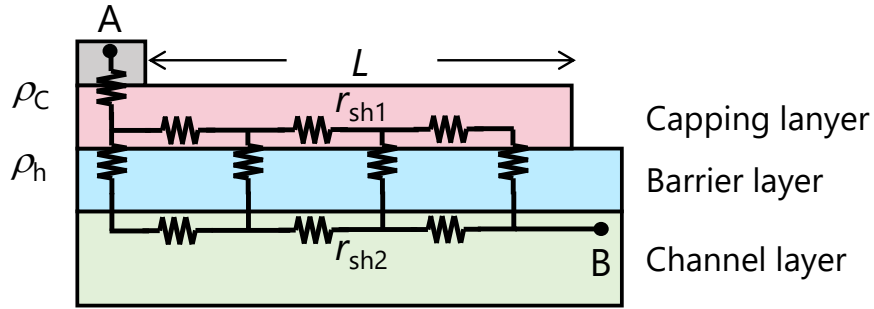


Figure 2.11: Equivalent circuit model of the capping layer and the channel regions of an HFET.

Table 2.3: Calculated values of the actual contact resistance (R_{total}), the sheet resistance of the capping layer (r_{sh1}) and the parasitic contact resistance at the heterojunction (ρ_{h}).

	Capping layer	InAlGaN	GaN
Contact resistance to 2DEG	R_{total} [Ω mm]	1.6	2.5
Sheet resistance of capping layers	r_{sh1} [$\Omega/\square$]	1470	180
Parasitic resistance at the heterojunction	ρ_{h} [Ω cm ²]	7.8×10^{-6}	4.1×10^{-5}

quaternary alloys was demonstrated. The composition of the InAlGaN alloys was designed to be lattice-matched with GaN to serve enough thickness, and to have close band gap and total polarization as compared with an underlying AlGaN barrier layer so that electron depletion and a potential barrier were eliminated at the InAlGaN/AlGaN interfaces. Detailed analysis of source resistance revealed that parasitic resistance at the InAlGaN/AlGaN interfaces was $7.8 \times 10^{-6} \Omega\text{cm}^2$, which was one-fifth as low as at the conventional GaN/AlGaN interfaces. Thus, use of the InAlGaN quaternary alloys as a capping layer for AlGaN/GaN HFETs is promising technique to reduce the source resistance enabling improved device performance.

References

- [1] R. Bernardini, V. Fiorentini, and D. Vanderbilt, *Phys. Rev. B* **56**, 10024 (1997).
- [2] A. Bykhovski, B. Gelmont, and M. Shur, *J. Appl. Phys.* **74**, 6734 (1993).
- [3] K. Joshin, T. Kikkawa, H. Hayashi, T. Maniwa, S. Yokokawa, M. Yokoyama, N. Adachi and M. Takikawa, *IEDM Tech. Dig.*, 2003, p. 983.
- [4] R. Quay, A. Tessmann, R. Kiefer, R. Weber, F. van Raay, M. Kuri, M. Riessle, H. Massler, S. Muller, M. Shlechtweg and G. Weinmann, *IEDM Tech. Dig.*, 2003, p. 567.
- [5] T. Hussain, A. Kurdoghlian, P. Hashimoto, W.-S. Wong, M. Wetzel, J-S. Moon, L. McCray and M. Micovic, *IEDM Tech. Dig.*, 2001, p. 581.
- [6] Y. Hirose, Y. Ikeda, M. Ishii, T. Murata, K. Inoue, T. Tanaka, H. Ishikawa, T. Egawa and T. Jimbo, *IEICE Trans. Electron.* **E86-C**, 2058 (2003).
- [7] H. Ishida, Y. Hirose, T. Murata, A. Kanda, Y. Ikeda, T. Matsuno, K. Inoue, Y. Uemoto, T. Tanaka and D. Ueda, *IEDM Tech. Dig.*, 2003, p. 583.
- [8] M. Kanamura, T. Kikkawa, N. Adachi, T. Kimura, S. Yokogawa, M. Nagahara, N. Hara, and K. Joshin, *Ext. Abstr. Solid State Devices and Materials*, 2003, p. 916.
- [9] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, *J. Appl. Phys.* **85**, 3222 (1999).
- [10] I. P. Smorchkove, C. R. Elsass, J. P. Ibbetson, R. Vetury, B. Heying, P. Fini, E. Haus, S. P. DenBaars, J. S. Speck, and U. K. Mishra, *J. Appl. Phys.* **86**, 4520 (1999).
- [11] L. Hsu and W. Walukiewicz, *J. Appl. Phys.* **89**, 1783 (2001).
- [12] F. Bernardini and V. Fiorenini, *Phys. Rev. B* **56**, R10 024 (1997).
- [13] T. Detchprohm, K. Hiramatsu, K. Itoh, and I. Akasaki, *Jpn. J. Appl. Phys.* **31**, L1454 (1992).
- [14] T. L. Tansley and C. P. Foley, *J. Appl. Phys.* **59**, 3241 (1986).
- [15] D. Nilsson, E. Janzén, and A. Kakanakova-Georgieva, *J. Phys. D: Appl. Phys.* **49**, 175108 (2016).
- [16] A. Zoroddu, F. Bernardini, P. Ruggerone, and V. Fiorentini, *Phys. Rev. B* **64**, 45208 (2001).
- [17] A. F. Wright, *J. Appl. Phys.* **82**, 2833 (1997).

- [18] E. T. Yu, G. J. Sullivan, P. M. Asbeck, C. D. Wang, D. Qiao, and S. S. Lau, *Appl. Phys. Lett.* **71**, 2794 (1997).
- [19] C. H. Chen, S. Keller, G. Parish, R. Ventury, P. Kozodoy and Y. Wu, *Appl. Phys. Lett.* **73**, 3147 (1998).
- [20] D. Qiao, Z. F. Guan, J. Carlton, S. S. Lau and G. J. Sullivan, *Appl. Phys. Lett.* **74**, 2652 (1999).
- [21] K. O. Schweitz, P. K. Wang, S. E. Mohny and D. Gotthold, *Appl. Phys. Lett.* **80**, 1954 (2002).
- [22] T. Tanaka, H. Furukawa, H. Takenaka, T. Ueda, T. Fukui, and D. Ueda, *IEEE Trans. Electron Devices* **44**, 354 (1997).
- [23] Y.-L. Lai, E. Y. Chang, C.-Y. Chang, T. H. Liu, and S. P. Wang, *Jpn. J. Appl. Phys.* **36**, 1856 (1997).
- [24] H. P. Maruska and J. J. Tietjen, *Appl. Phys. Lett.* **15**, 327 (1969).
- [25] T. Detchprohm, K. Hiramatsu, K. Itoh, and I. Akasaki, *Jpn. J. Appl. Phys.* **31**, L1454 (1992).
- [26] G. A. Jeffrey and G. S. Parry, *J. Chem. Phys.* **23**, 406 (1955).
- [27] H. Schulz and K. H. Thiemann, *Solid State Comm.* **23**, 815 (1977).
- [28] I. C. Huseby, *J. Am. Ceram. Soc.* **66**, 217 (1983).
- [29] T. L. Tansley and C. P. Foley, *J. Appl. Phys.* **59**, 3241 (1986).
- [30] R. B. Zetterstrom, *J. Mater. Sci.* **5**, 1102 (1970).
- [31] J. I. Pankove, H. P. Maruska and J. E. Berkeyheiser, *Appl. Phys. Lett.* **17**, 197 (1970).
- [32] W. M. Yim, E. J. Stofko, P. J. Zanzucchi, J. I. Pankove, M. Ettenberg and S. L. Gilbert, *J. Appl. Phys.* **44**, 292 (1973).
- [33] V. Yu. Davydov, A. A. Klochikhin, R. P. Seisyan, V. V. Emtsev, S. V. Ivanov, F. Bechstedt, J. Furthmuller, H. Harima, A. V. Mudryi, J. Aderhold, O. Semchinova, and J. Graul, *Phys. Stat. Solidi (b)* **229**, r1 (2002).
- [34] F. Yun, M. A. Reshchikov, L. He, T. King, H. Morkoç, S. W. Novak, and L. Wei, *J. Appl. Phys.* **92**, 4837 (2002).
- [35] S. Nakamura, *J. Vac. Sci. Tech. A* **13**, 705 (1995).
- [36] M. E. Aumer, S. F. LeBoeuf, F. G. McIntosh, and S. M. Bedair, *Appl. Phys. Lett.* **75**, 3315 (1999).

- [37] E. Monroy, N. Gogneau, F. Enjalbert, F. Fossard, D. Jalabert, E. Bellet-Amalric, L. S. Dang, and B. Daudin, *J. Appl. Phys.* **94**, 3121 (2003).
- [38] H. Masato, Y. Ikeda, T. Matsuno, K. Inoue and K. Nishii, *IEDM Tech. Dig.*, 2000, p.377.
- [39] M. D. Feuer, *IEEE Trans. Electron Devices* **ED-32**, 7 (1985).

Chapter 3

AlGaN/GaN HFETs for High Frequency Applications

3.1 Introduction

AlGaN/GaN heterojunction field effect transistors (HFETs) have been widely investigated for high frequency and high power applications owing to the superior material properties such as the high saturated electron velocity and the high breakdown voltage [1–6]. In the development of the AlGaN/GaN HFETs for microwave power applications, one of the most critical issues to be overcome was the transient decrease of a drain current or/and the increase of the on-state resistance observed after applying high drain voltage referred to as “current collapse” [7–11]. Since the current collapse has severely limited the performance of the AlGaN/GaN HFETs, it should be suppressed for the practical applications. Among the various approaches to suppress the current collapse, one of the most effective ones is the adoption of the field plates, the additional electrodes formed on a dielectric layer at the drain side of the AlGaN/GaN HFETs [12–16]. The relief of the electric field crowding at the drain side of gate edge by the field plates results in the suppression of the carrier trapping effect causing current collapse as well as the increase of the breakdown voltage [17, 18].

At present, AlGaN/GaN microwave power transistors on SiC substrates have been commercialized taking advantage of better lattice matching of SiC to GaN and the high thermal conductivity of SiC [20]. Although use of SiC substrates for the GaN-based transistors is promising, the high cost and the small wafer size are potential obstacle for the wide spread use in the future. Recent progress of the epitaxial growth of GaN on cost-effective Si substrates in a large diameter is expected to overcome the issue [21–24]. However, the high frequency performance of GaN transistors on Si is not yet satisfactory in terms of the output power and the gain as compared with those on SiC [25–27].

In this chapter, the effects of the field plates on the high frequency performance was investigated to achieve the AlGaN/GaN HFETs on Si substrates exhibiting high power together with high gain. The design of the field plate structure using the device parameters extracted from the small signal characteristics based on the equivalent circuit is described.

3.2 High Power, High Gain AlGaIn/GaN HFETs

3.2.1 Structure of AlGaIn/GaN HFETs with Field Plates

The schematic cross section and the scanning electron microscope (SEM) image of the AlGaIn/GaN HFET with the filed plates are shown in Figs. 3.1 and 3.2, respectively. AlGaIn/GaN heterostructures were grown on highly resistive Si substrates by metal-organic chemical vapor deposition (MOCVD). Owing to the optimized growth conditions, the high mobility of $1900 \text{ cm}^2/(\text{V}\cdot\text{s})$ as well as the low sheet resistance of $340 \text{ }\Omega/\square$ was achieved. Ti/Al was used as ohmic contacts for the source and the drain, while Ni/Au was used for the gate electrode. Field plates connected to the source electrodes were placed over the SiN passivation [28, 29]. Electroplated Au layers were formed as a part of the interconnections. The gate length (L_g) and the gate-drain spacing (L_{gd}) were 0.6 and $3.0 \text{ }\mu\text{m}$, respectively. The length between the drain side of the gate edge and the edge of the field plate is defined as the field plate length (L_{fp}).

The fabricated device typically exhibits the maximum drain current and the on-state resistance of 850 mA/mm and $4.0 \text{ }\Omega\cdot\text{mm}$, respectively. Figure 3.3 shows the pulsed current-voltage (I - V) characteristics of the fabricated AlGaIn/GaN HFET. The off-state stress for the pulsed I - V measurements was given by the biasing condition with the gate-source voltage (V_{gs}) of -5 V and the drain-source voltage (V_{ds}) of 50 V . The I - V curves with and without the off-state stress are identical, indicating that the device does not suffer from current collapse.

3.2.2 Design of Field Plates

Prior to the detailed designing of the field plates, large signal performance of the fabricated AlGaIn/GaN HFETs were characterized by load-pull measurement at 2.5 GHz to examine the effect of the field plate. In this measurement, the ends of the field plate was placed in the middle of the gate-drain spacing ($L_{fp} = 1.5 \text{ }\mu\text{m}$), which was expected to reduce the maximum electric field around the gate at best [15, 30]. Figure 3.4 shows the measured power characteristics of the HFETs with and without field plates. It is seen that the field plate increases the gain at low input power. The maximum output power, however, is not much increased because of the gradual reduction of the gain at the increased input power as seen in Fig. 3.4, even though the output matching is adjusted to serve the highest output power. The output impedance of the fabricated HFETs with and without field plates at various drain voltages is shown in Fig. 3.5, where it is found that the variation is significant for the device with the field plate. Increasing the input power leads to the larger swing of the drain voltage. Thus, the observed variation of the output impedance by the introduction of the field plate results in the increase of the matching loss at the output side for higher input power. Consequently, the gain is gradually reduced for the increased input power as shown in Fig. 3.4. Thus, the suppression of the change of the output impedance should be critical to attain high maximum output power maintaining

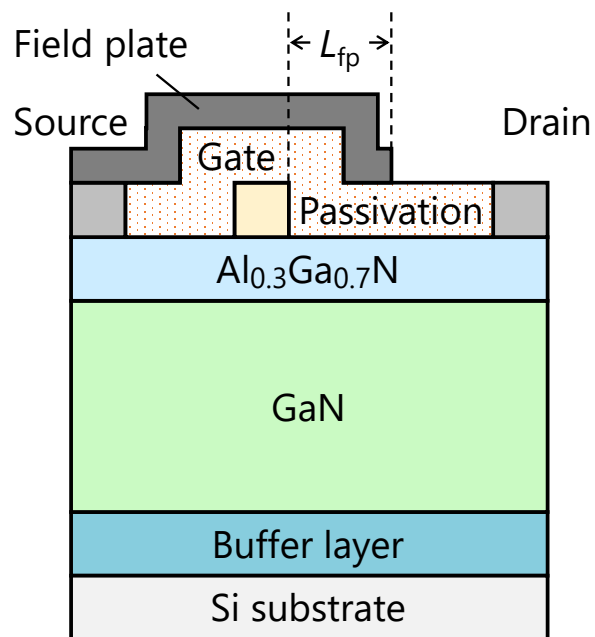


Figure 3.1: Schematic cross section of the fabricated AlGaN/GaN HFET.

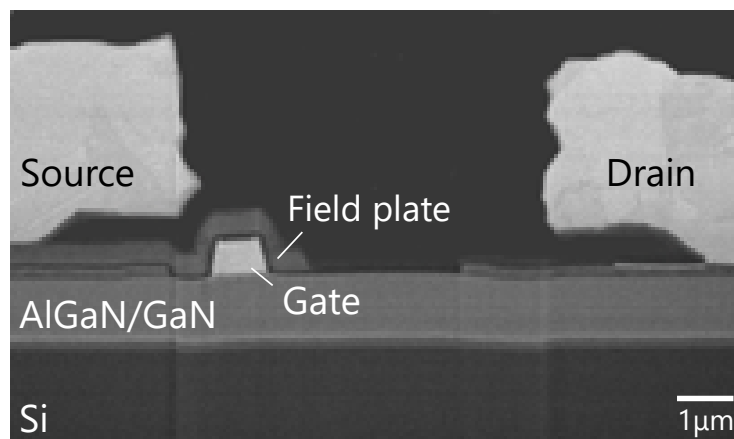


Figure 3.2: Cross sectional SEM image of the fabricated AlGaN/GaN HFET.

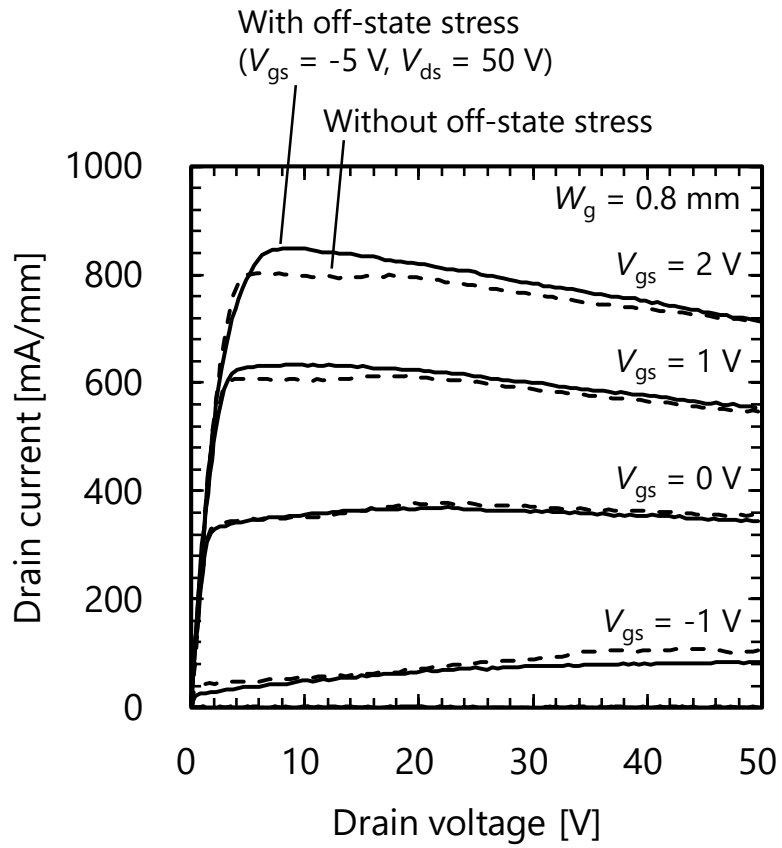


Figure 3.3: Pulsed I - V characteristics of the fabricated AlGaIn/GaN HFET with and without the off-state stress.

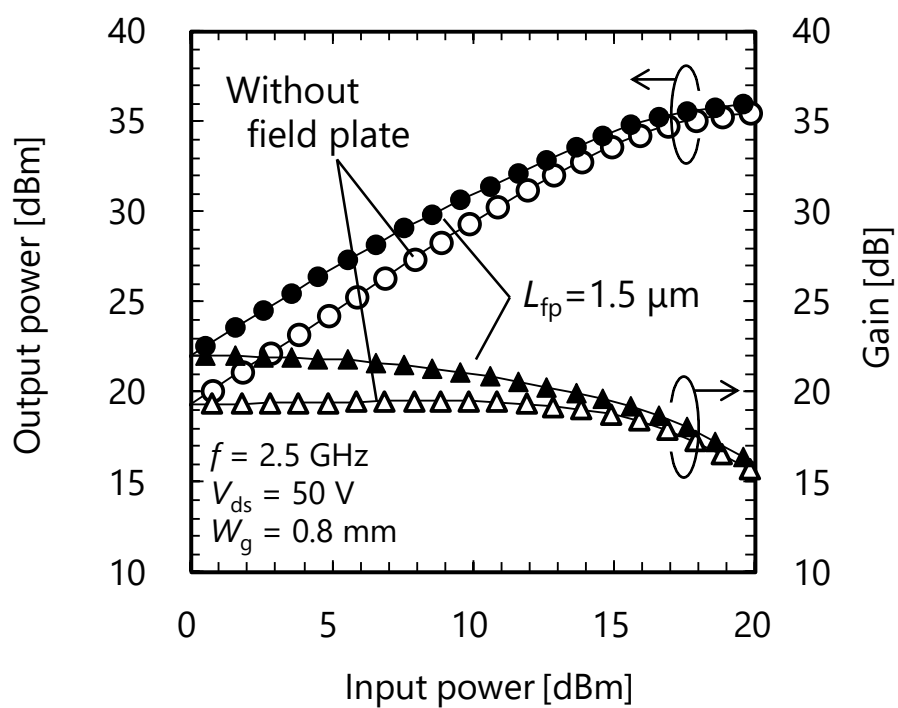


Figure 3.4: Power characteristics of the AlGaIn/GaN HFETs with $1.5 \mu\text{m}$ field plates and without field plates.

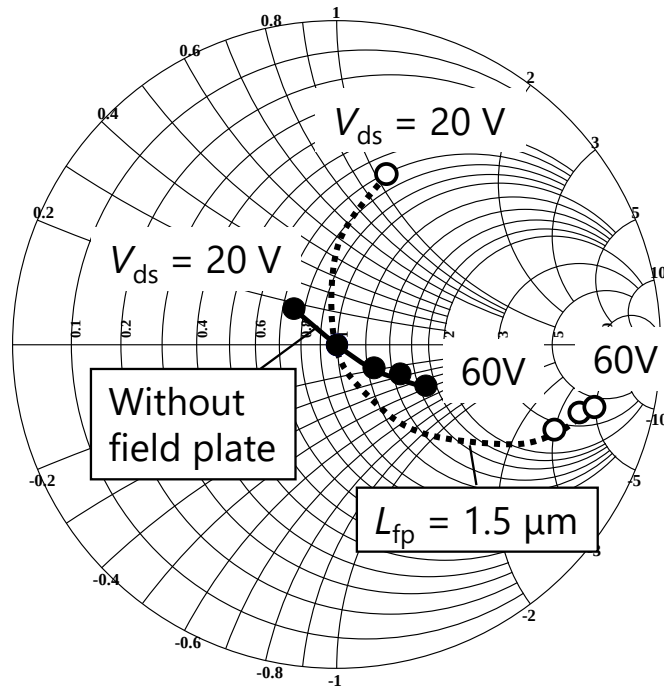


Figure 3.5: Change of the output impedance (S_{22}) for the variation of the drain voltage (V_{ds}). Dotted line represents the variation for the device with the field plate length (L_{fp}) of $1.5 \mu\text{m}$, while solid line represents that for the device without the field plate.

the high gain.

To clarify the reason for the variation of the output impedance, S -parameter measurements were performed and the device parameters were analyzed by using the equivalent circuit shown in Fig. 3.6. Besides the conventional gate-to-source capacitance (C_{gs}) and the drain-to-source capacitance (C_{ds}), the additional capacitance are added onto the conventional equivalent circuit to describe the effects of the field plates in this model, which are denoted as C_{gs_fp} and C_{ds_fp} , respectively. Based on this circuit model, the device parameters were extracted for the various bias conditions from the measured S -parameters [31, 32].

Figures 3.7 and 3.8 show the extracted gate-to-drain capacitance (C_{gd}) and the total source-to-drain capacitance ($C_{ds} + C_{ds_fp}$) as a function of the drain voltage for the various field plate lengths, respectively. The C_{gd} , which acts as a feedback capacitance, is reduced by the field plates regardless their lengths, supporting the experimentally observed increase of the gain at the low input power. The source-to-drain capacitance varies dramatically at higher drain voltage in the HFETs with longer field plates. It is found that the variation can be suppressed by shortening the field plates down to $0.6 \mu\text{m}$. It is also noted that the C_{ds} in Fig. 3.8 without field plates ($L_{fp} = 0 \mu\text{m}$) is less than 40 fF up to 60 V of the drain voltage. The values are not changed for the variation of the drain voltages and the values are far smaller than the extracted C_{ds_fp} originated from the field plates. Thus, the variation of the source-to-drain capacitance can be the origin of the above-mentioned change of the output impedance so that the variation of the output impedance can be suppressed by shortening the field plates.

The change of the output impedance by the variation of the drain bias was measured for the HFETs with shorter field plate length as shown in Fig. 3.9. The change is suppressed by shortening the field plate length down to $0.6 \mu\text{m}$ from the conventional one with the length of $1.5 \mu\text{m}$ as seen in the figure. The suppression of the change should help to increase the output power of the HFETs while maintaining the high linear gain.

Figure 3.10 shows the measured and simulated values of the maximum output power (P_{max}) and the linear gain for the HFETs with the gate width of 0.8 mm plotted as a function of L_{fp} . The simulation was carried out by using the commercially available EEHEMT large signal model with the device parameters shown in Fig. 3.6. In Fig. 3.10, symbols represent the experimental values, while dashed lines represent the simulated ones. The output power where the gain deviates from the linear gain by 3 dB, referred to as $P_{3\text{dB}}$, is defined as the maximum output power. The experimental values well agree with the simulated ones, where the $0.6 \mu\text{m}$ of the field plate length is the optimum to achieve both the high gain and the high output power.

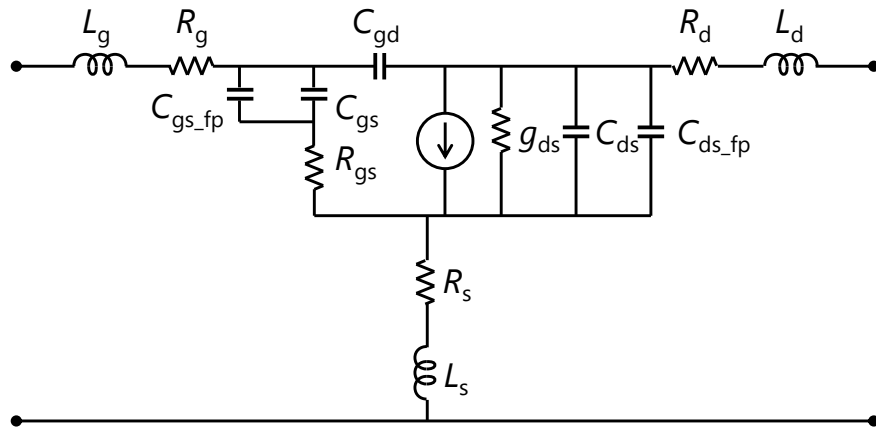


Figure 3.6: Equivalent circuit model used for the extraction of the device parameters of the Al-GaN/GaN HFET.

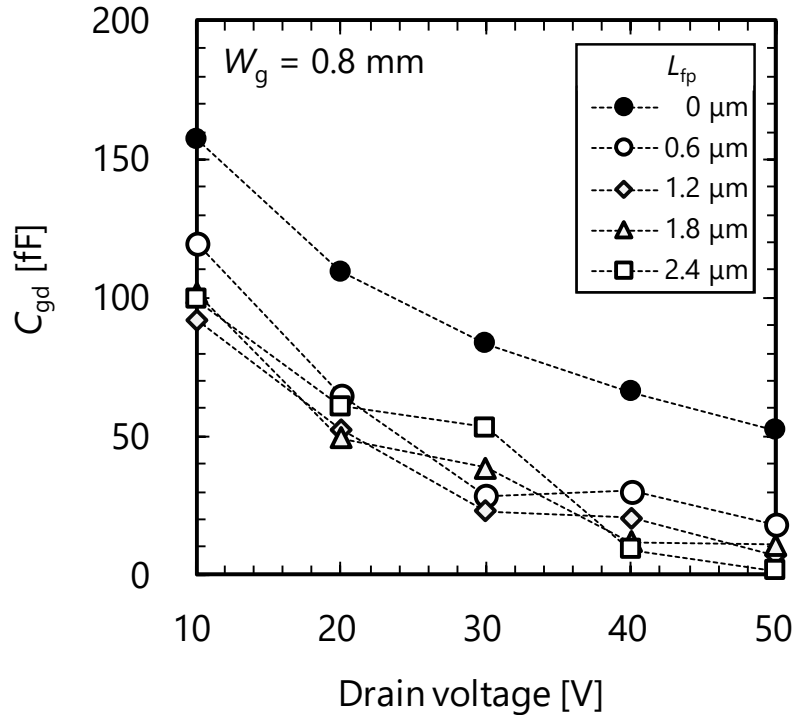


Figure 3.7: Extracted gate-to-drain capacitance (C_{gd}) as a function of the drain voltage for the various field plate lengths.

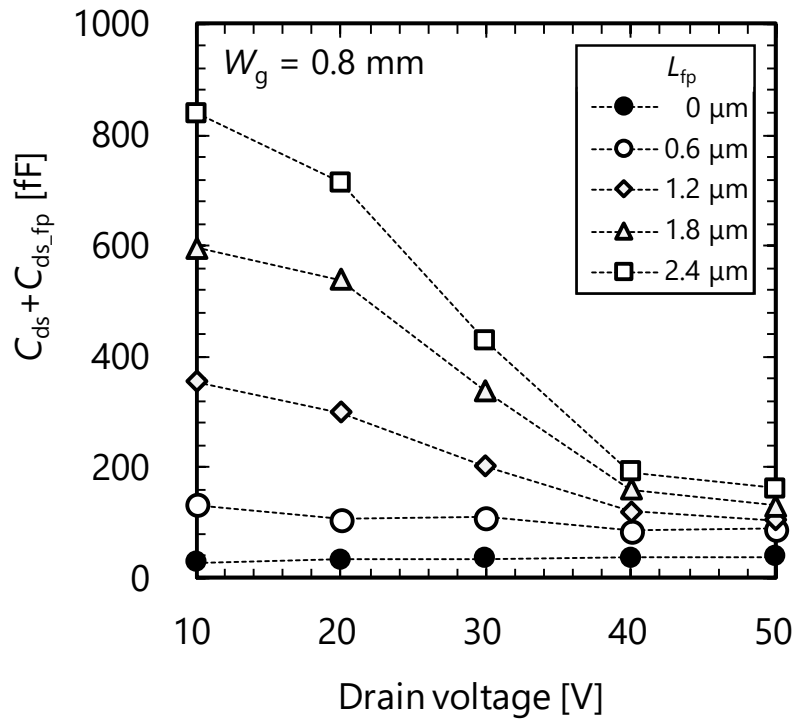


Figure 3.8: Extracted source-to-drain capacitance ($C_{ds} + C_{ds_fp}$) as a function of the drain voltage for the various field plate lengths.

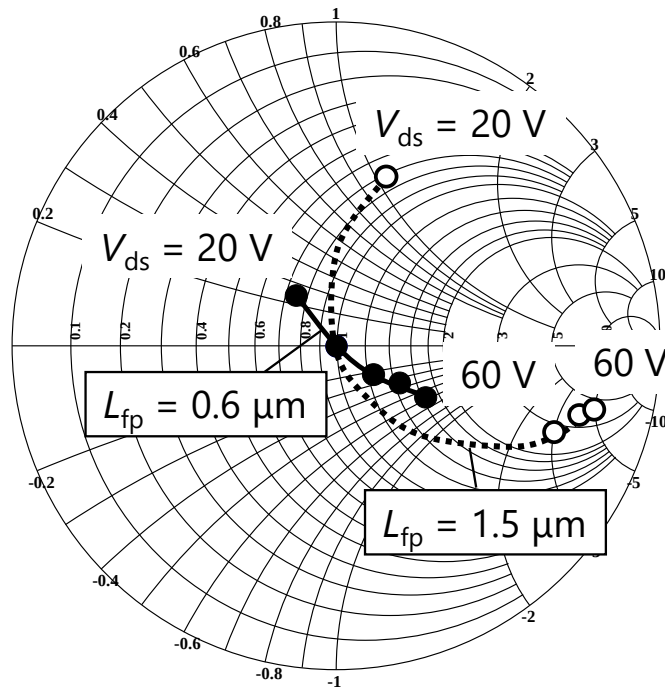


Figure 3.9: Change of the output impedance (S_{22}) for the variation of the drain voltage (V_{ds}). Solid line represents the variation for the device with the L_{fp} of $0.6 \mu\text{m}$, while dotted line represents the variation for the device with the L_{fp} of $1.5 \mu\text{m}$.

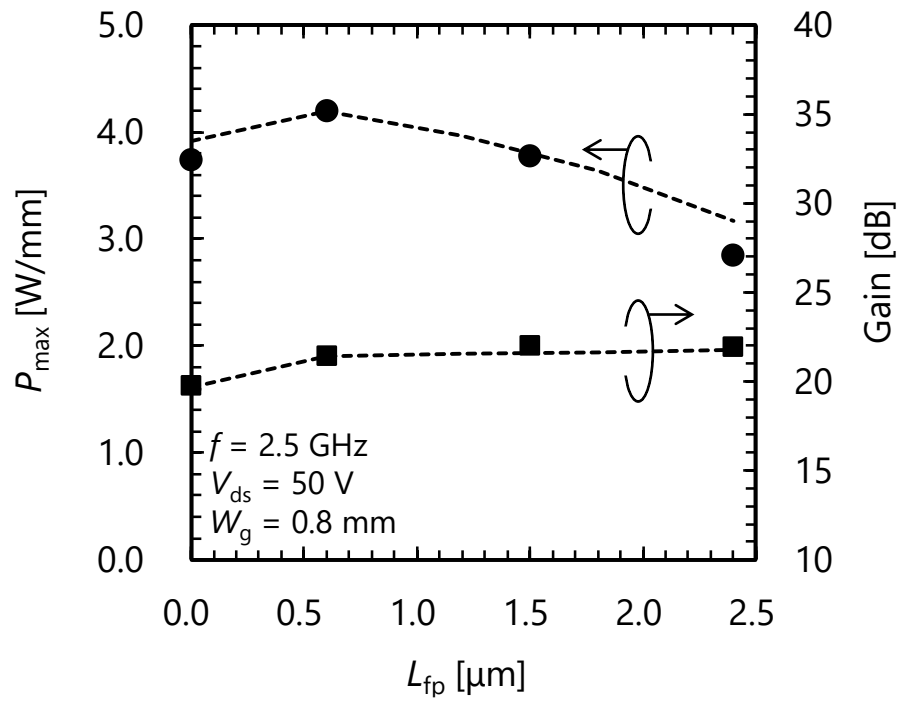


Figure 3.10: Simulated and experimental values of the maximum output power (P_{max}) and the linear gain for the HFETs with the gate width of 0.8 mm plotted as a function of the field plate length (L_{fp}). Symbols represent experimental values, while dashed lines represent simulated ones.

3.3 Performance of Fabricated AlGaIn/GaN HFETs

To demonstrate the higher absolute output power with the high gain for practical applications, the power measurements of the AlGaIn/GaN HFET with the gate width of 48 mm were performed. Figure 3.11 shows an experimentally obtained output power and a gain together with power-added efficiency (PAE) of the fabricated AlGaIn/GaN HFET on a Si substrate with the field plate length of 0.6 μm . Here, the PAE is given by the following equation:

$$\text{PAE} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}}, \quad (3.1)$$

$$= \frac{P_{\text{out}}}{P_{\text{DC}}} \left(1 - \frac{1}{G_p}\right), \quad (3.2)$$

where P_{in} and P_{out} represent the input and output power, P_{DC} represents the supplied DC power, and G_p is a gain. A maximum output power of 203 W and a linear gain of 16.9 dB were achieved at 2.5 GHz. High drain voltage of 50 V can be applied, which helps to attain the high output power. High PAE of 64 % was confirmed, which is attributed to less reduced gain even at a high input power due to the short field plate length since PAE is related to a gain as derived from Eq. (3.2).

3.4 Discussion

Figure 3.12 shows the maximum output power of the fabricated AlGaIn/GaN HFET with gate width of 48 mm measured for various drain voltages. Since the output power is still increased up to 50 V, further increase of an output power is expected by increasing breakdown voltage while providing sufficient thermal managements. Power consumption of HFETs is denoted by

$$P = P_{\text{DC}} + P_{\text{in}} - P_{\text{out}}. \quad (3.3)$$

Substituting Eq. (3.1) into Eq. (3.4) results in

$$P = P_{\text{DC}}(1 - \text{PAE}). \quad (3.4)$$

Since this power consumption is converted into heat, high PAE associated with high gain is important in terms of thermal managements. A device with lower PAE requires more severe heat dissipation design such as thinning substrates and enlargement of heat sink to avoid device destruction, which makes device fabrication more complicate.

In measurement of power performance, a matching condition for achieving high output power and that for achieving high efficiency are generally different, rather in a trade-off relation. Since this difference originates in the on-state resistance of HFETs, it is important to reduce the on-state resistance to achieve a high output power together with high efficiency [33]. For instance,

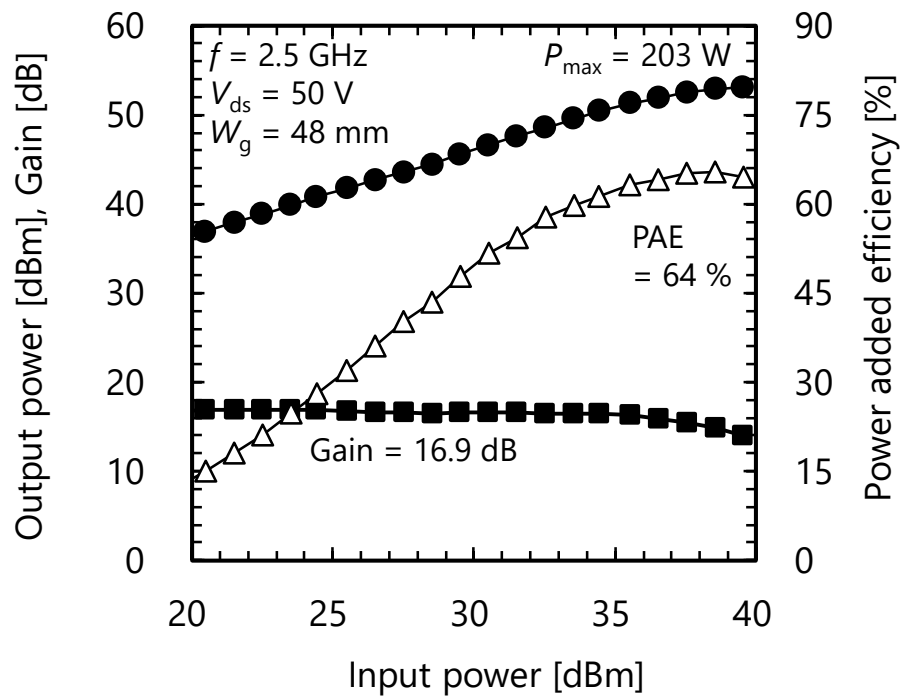


Figure 3.11: Power characteristics of the fabricated AlGaN/GaN HFET with the gate width of 48 mm.

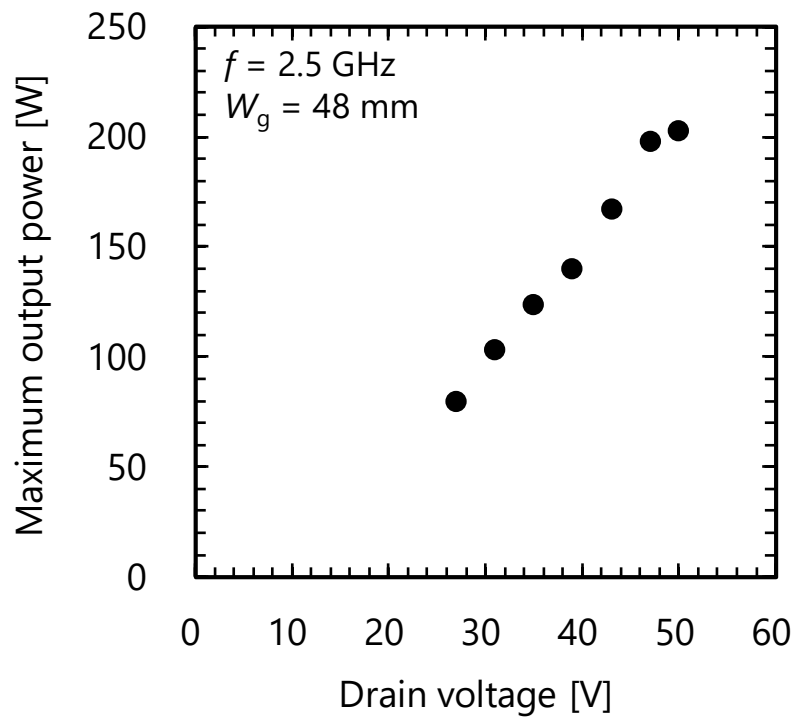


Figure 3.12: Maximum output power of the fabricated AlGaIn/GaN HFET with the gate width of 48 mm as a function of the drain voltage.

introduction of InAlGa_N capping layer would be effective for reduction of the on-state resistance

Combining the adequate design of field plates, which leads to high power with high efficiency, and reduction of on-state resistance will enable further improvement in the power performance.

3.5 Summary

High output power with high linear gain at 2.5 GHz by AlGa_N/Ga_N HFETs on Si have been demonstrated. The field plates, which reduce the feedback capacitance, were designed using the device parameters extracted from the small signal RF performance. In general, length of a field plate is a half of gate-drain spacing, which is most effective to relieve an electric field crowding at a gate edge, whereas it was experimentally found that such long field plates caused significant change of output impedance by variation of drain voltage, resulting in reduction of a maximum output power. The equivalent circuit analysis revealed that change of drain-source capacitance caused the change of the output impedance which could be suppressed by shortening the field plates. The fabricated HFETs with field plate length of 0.6 μm shorter than the conventional length exhibited the high output power of 203 W with high linear gain of 16.9 dB at 2.5 GHz. The presented AlGa_N/Ga_N HFETs have demonstrated the highest linear gain among the reported 100 W-class Ga_N-based power amplifiers on Si, demonstrating that they would lower the system cost and make the system smaller with the reduced number of the power amplifier stages. Thus, the presented HFETs are promising for various microwave applications including cellular base stations taking advantages of the superior performance.

References

- [1] H. Xing, S. Keller, Y.-F. Wu, L. McCarthy, I. P. Smorchkova, D. Buttari, R. Coffie, D. S. Green, G. Parish, L. Shen, N. Zhang, J. J. Xu, B. P. Keller, S. P. DenBaars, and U. K. Mishra, *J. Phys.: Condens. Matter* **13**, 7139 (2001).
- [2] K. Joshin, T. Kikkawa, H. Hayashi, T. Maniwa, S. Yokokawa, M. Yokoyama, N. Adachi, and M. Takikawa, *IEDM Tech. Dig.*, 2003, p. 983.
- [3] Y. Okamoto, Y. Ando, K. Hataya, T. Nakayama, H. Miyamoto, T. Inoue, M. Senda, K. Hirata, M. Kosaki, N. Shibata, and M. Kuzuhara, *IEEE Trans. Microwave Theory Tech.* **52**, 2536 (2004).
- [4] T. Ueda, Y. Uemoto, T. Tanaka, and D. Ueda, *Int. J. High Speed Electron. Syst.* **19**, 145 (2009).
- [5] M. Yanagihara, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, *Phys. Status Solidi A* **206**, 1221 (2009).
- [6] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, *IEEE Trans. Microw. Theory Tech.* **60**, 1764 (2012).
- [7] M. A. Khan, M. S. Shur, Q. C. Chen, and J. N. Kuznia, *Electron. Lett.* **30**, 2175 (1994)
- [8] S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, *IEEE Trans. Electron Devices* **48**, 465 (2001).
- [9] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, *IEEE Trans. Electron Devices* **48**, 560 (2001).
- [10] I. Daumiller, D. Theron, C. Gaqui è re, A. Vescan, R. Dietrich, A. Wieszt, H. Leier, R. Vetury, U. K. Mishra, I. P. Smorchkova, S. Keller, N. X. Nguyen, C. Nguyen, and E. Kohn, *IEEE Electron Device Lett.* **22**, 62 (2001).
- [11] A. F. M. Anwar, S. S. Islam, and R. T. Webster, *Appl. Phys. Lett.* **84**, 1970 (2004).
- [12] B. M. Green, K. K. Chu, E. M. Chambers, J. A. Smart, J. R. Shealy, and L. F. Eastman, *IEEE Electron Device Lett.* **21**, 268 (2000).
- [13] T. Hashizume, S. Ootomo, S. Oyama, M. Konishi, and H. Hasegawa, *J. Vac. Sci. Technol. B* **19**, 1675 (2001).
- [14] T. Mizutani, Y. Ohno, M. Akita, S. Kishimoto, and K. Maezawa, *IEEE Trans. Electron Devices* **50**, 2015 (2003).

- [15] Y. Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue, and M. Kuzuhara, *IEEE Electron Device Lett.* **24**, 289 (2003).
- [16] A. Chini, D. Buttari, R. Coffie, S. Heikman, S. Keller, and U. K. Mishra, *Electron. Lett.* **40**, 73 (2004).
- [17] A. S. Grove, O. Leistiko Jr., and W. W. Hooper, *IEEE Trans. Electron Devices* **ED-14**, 157 (1967).
- [18] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, *IEEE Trans. Electron Devices* **54**, 1825 (2007).
- [19] Y. Ando, A. Wakejima, Y. Okamoto, T. Nakayama, K. Ota, K. Yamanoguchi, Y. Murase, K. Kasahara, K. Matsunaga, T. Inoue, and H. Miyamoto, *IEDM Tech. Dig.*, 2005, p. 576.
- [20] G. L. Harris: *Properties of Silicon Carbide* (Inspec, London, 1995) EMIS Datareviews Series, No. 13, p. 5.
- [21] H. Ishikawa, G. -Y. Zhao, N. Nakada, T. Egawa, T. Jimbo and M. Umeno, *Jpn. J. Appl. Phys.* **38**, L492 (1999).
- [22] H. Marchand, L. Zhao, N. Zhang, B. Moran, R. Coffie, U. K. Mishra, J. S. Speck, S. P. DenBaars, and J. A. Freitas, *J. Appl. Phys.* **89**, 7846 (2001).
- [23] A. Ubukata, K. Ikenaga, N. Akutsu, A. Yamaguchi, K. Matsumoto, T. Yamazaki, and T. Egawa, *J. Cryst. Growth* **298**, 198 (2007).
- [24] K. Cheng, M. Leys, S. Degroote, J. Derluyn, B. Sijmus, P. Favia, O. Richard, H. Bender, M. Germain, and G. Borghs, *Jpn. J. Appl. Phys.* **47**, 1553 (2008).
- [25] E. M. Chumbes, A. T. Schemer, J. A. Smart, D. Hogue, J. Komiak, and J. R. Shealy, *IEDM Tech. Dig.*, 1999, p. 397.
- [26] A. Krost and A. Dadgar, *Phys. Status Solidi A* **194**, 361 (2002).
- [27] N. Vellas, C. Gaquiere, A. Minko, V. Hoel, J. C. De Jaeger, Y. Cordier, and F. Semond, *IEEE Microwave Wireless Components Lett.* **13**, 99 (2003).
- [28] A. Wood, C. Dragon, and W. Burger, *IEDM Tech. Dig.*, 1996, p. 87.
- [29] E. Lan, S. Klingbeil, P. Fisher, B. Green, P. Li, C. Weitzel, E. Johnson, M. DeBaca, and H. Le, *Proc. CSMantech Dig.*, 2004, p. 35.
- [30] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura, and H. Ohashi, *IEEE Trans. Electron Devices* **50**, 2528 (2003).

- [31] G. Dambrine, A. Cappy, F. Heliodore, and E. Playes, IEEE Trans. Microwave Theory Tech. **36**, 1151 (1988).
- [32] G. Chen, V. Kumar, R. S. Schwindt, and I. Adesida, IEEE Trans. Microwave Theory Tech. **54**, 2949 (2006).
- [33] Y. Takayama, IEICE Trans. Electron. **e80-c**, 726 (1997).

Chapter 4

Interface Properties in $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ Metal-Insulator-Semiconductor Diodes

4.1 Introduction

$\text{AlGaIn}/\text{GaIn}$ heterojunction field-effect transistors (HFETs) are promising for power switching applications, owing to the superior properties of GaIn based materials [1–3]. From a fail-safe viewpoint, such applications require normally-off operations of the $\text{AlGaIn}/\text{GaIn}$ HFETs, mainly achieved by the design of the gate structures. Among the various gate structures proposed [4–7], a metal-insulator-semiconductor (MIS) gate should be the most promising since the introduction of gate insulators effectively reduces the gate leakage current and enhances the gate-voltage-swing, which is indispensable for such applications [8–13]. Among the various insulators, Al_2O_3 is one of the most suitable choices because of its large dielectric constant, high breakdown electric field and large offset of the conduction band energy between Al_2O_3 and GaIn [14–16]. The atomic layer deposition (ALD) is widely used to form Al_2O_3 , which is advantageous due to its good controllability of thickness with good uniformity.

However, the interfaces between $\text{AlGaIn}/\text{GaIn}$ heterostructures and Al_2O_3 insulators have never been stable enough to use GaIn-based MIS transistors for practical applications because of lack of good thermal oxide as in Si device. In addition, fabrication processes such as dry etching additionally affect the interfaces, causing an undesired hysteresis in transfer characteristics which needs to be solved for practical use.

In this chapter, effects of device fabrication processes on the MIS interface properties were investigated for the purpose of achieving technical directions to obtain the stable MIS interfaces. The interface states at the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ MIS interfaces and fixed charges in Al_2O_3 insulators were characterized by analyzing the C - V characteristics of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MIS heterojunction diodes.

4.2 Characterization Method of AlGaIn/GaIn MIS Heterostructures

Characterization of the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ MIS interface properties, including the extraction of the charge density in the insulators and interface state density at the MIS interfaces, were carried out by fitting calculated C - V curves with experimental ones. The calculations were performed by numerically solving the Poisson equation, taking account of the polarization charges at the AlGaIn/GaIn heterointerfaces, the interface state charges at the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ MIS interfaces and fixed charges in the Al_2O_3 films [17–19]. Figure 4.1 shows the calculated C - V curves for $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MIS diodes composed of 30-nm-thick Al_2O_3 films and 45-nm-thick AlGaIn layers, illustrating that each kind of charges has different effects on C - V curves. In this figure, increase of negative charges or reduction of positive charges is assumed, leading to a shift of C - V curves in a positive direction. In the opposite case, C - V curves shift in a negative direction. Among these charges, the polarization charges alter only the first step of the C - V curve corresponding to the threshold voltage (V_{th}) as shown in Fig. 4.1 (a), while the fixed charges in the Al_2O_3 films shift the whole curve as shown in Fig. 4.1 (b). The acceptor-type states at the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interfaces produce negative charges by capturing electrons, mainly exhibiting less steeper slope of the second step in the C - V curve corresponding the trapped electron density with sweeping gate voltage as shown in Fig. 4.1 (c). Although the deep acceptor-type states with long emission time constants remain negatively charged even under a large reverse bias and act as negative fixed charges [18], the effect is indistinguishable from the effect of the pure fixed charges in the Al_2O_3 films. Sum of these negative fixed charges and the fixed charges in the Al_2O_3 films are therefore considered as the effective fixed charges in this study.

4.3 Charge Engineering at MIS Interfaces during Device Fabrication Processes

4.3.1 Effects of Dry Etching Process

To achieve normally-off operations together with low on-state resistance in AlGaIn/GaIn HFETs, a combination of the MIS and recessed gate structures is promising. The recessed gate structures, where AlGaIn barrier layers are thinned selectively under the gate electrodes, are generally formed by dry etching [5, 20]. Several reports, however, have pointed out that a dry etching process induces deteriorative damage on the GaIn and AlGaIn surfaces [21–24]. Although such damage should affect the MIS interfaces formed on the dry-etched surfaces, there have been only a few reports on the characterization of the MIS interface properties formed on the dry-etched GaIn and AlGaIn surfaces. Hence the effects of the dry etching process on the MIS interfaces was investigated.

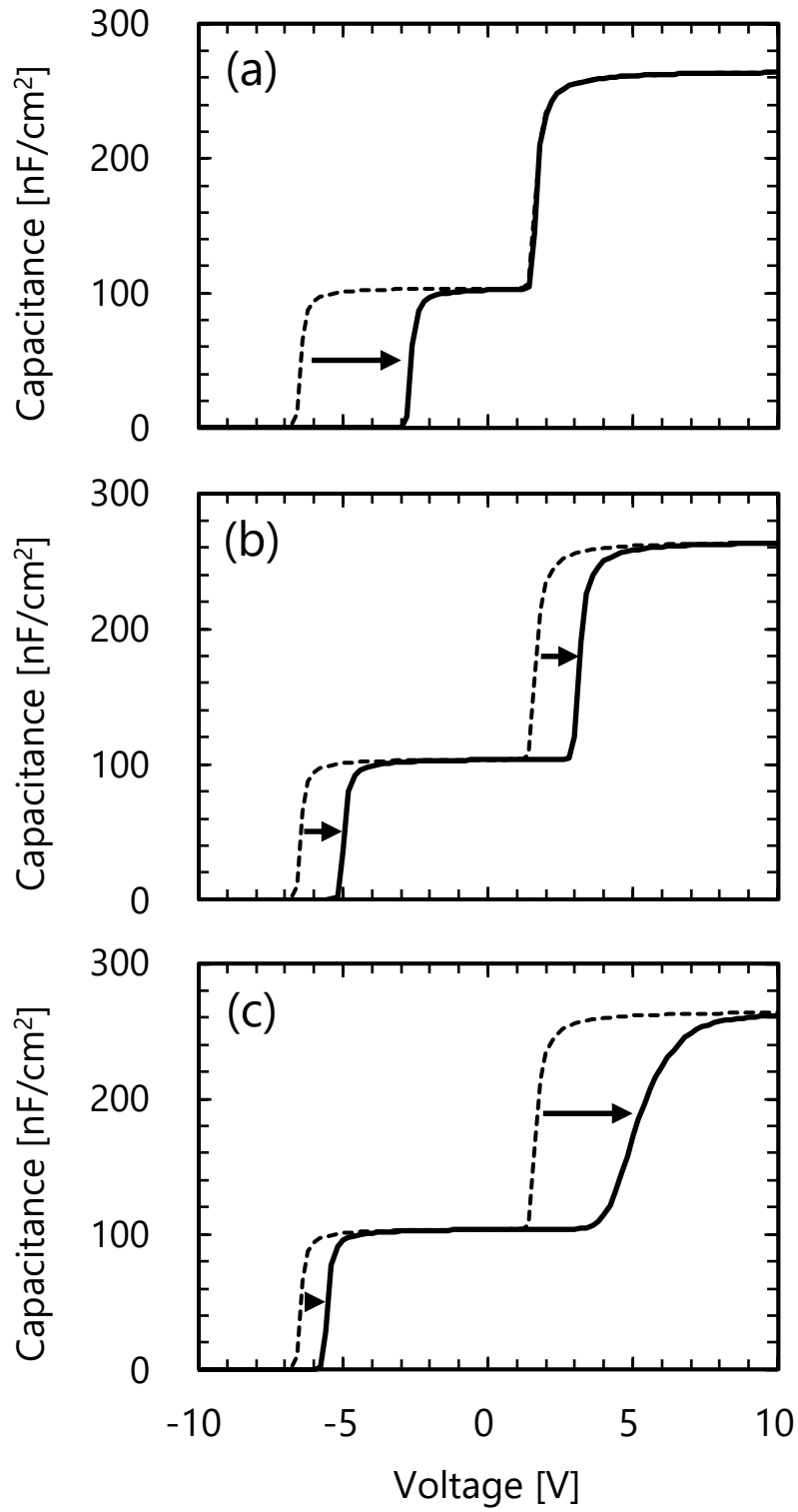
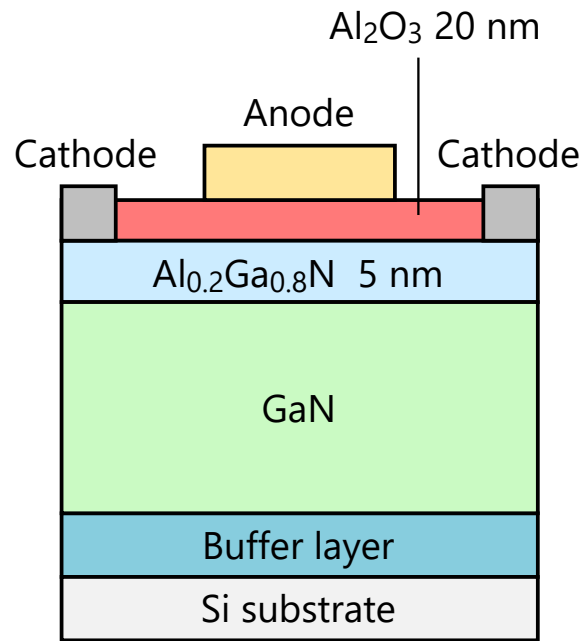


Figure 4.1: Schematic illustration about effects of (a) polarization charges at the heterointerfaces, (b) fixed charges in Al₂O₃, and (c) interface state charges at the Al₂O₃/AlGaN MIS interfaces on the C-V characteristics of Al₂O₃/AlGaN/GaN MIS heterojunction diodes. Dashed lines represent the calculated C-V curves without interface charges (ideal curves), while solid lines represent ones with taking each charge into account.

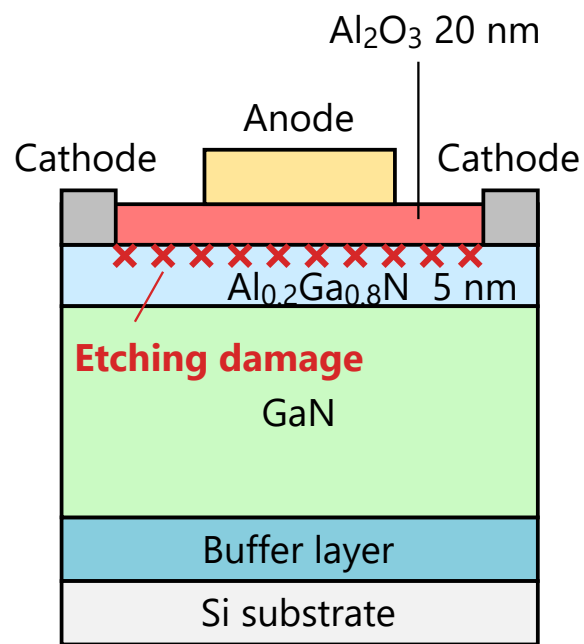
Two types of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MIS heterojunction diodes shown in Fig. 4.2 were used to examine the effect of the dry etching. Although both structures have the same AlGaIn thickness of 5 nm, the MIS structures were formed on dry etched surfaces in one diode (Fig. 4.2(b)) while on as-grown surfaces in the other (Fig. 4.2(a)). The $\text{Al}_{0.2}\text{Ga}_{0.8}\text{In}/\text{GaIn}$ heterostructures were grown on Si substrates by metal organic chemical vapor deposition (MOCVD) using the optimized growth conditions to obtain high-quality epitaxial heterostructures on Si substrates [25]. The thickness of AlGaIn layers for the diodes with and without dry etching process were 45 and 5 nm, respectively. Then, the 45-nm-thick AlGaIn layer was thinned down to 5 nm by Cl_2 -based inductively coupled plasma (ICP) etching. The AlGaIn layer thickness was thus 5 nm in both devices, which is expected to attain normally-off operations. 20-nm-thick Al_2O_3 films were then deposited on both structures by the ALD at the substrate temperature of 300 °C. In the ALD process, trimethylaluminum (TMA) was used as the Al precursor and oxygen plasma was used as the oxidant. After insulator deposition, cathode (Ti/Al) and anode electrodes (Ni/Au) were formed by electron beam evaporation.

Figure 4.3 shows the C - V characteristics of the fabricated $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MIS diodes with and without dry etching on the AlGaIn surfaces. The C - V measurements were carried out at room temperature (RT) at a measurement frequency of 100 kHz, and anode bias was swept from 8 to -2 V. The MIS diodes fabricated on AlGaIn/GaIn heterostructures generally show C - V curves with two steps, which correspond to the capacitance of insulators and the series capacitance of insulators and AlGaIn layers [26, 27]. In contrast, C - V curves in Fig. 4.3 show one step, which is attributed to the thin AlGaIn layers designed to attain normally-off operations. In this case, the value of the series capacitance becomes almost the same as that of the capacitance of the insulator and thus the C - V curve shows one step. In addition, the Fermi level crosses the interface state level near a threshold voltage in MIS heterojunction diodes with such thin AlGaIn barrier layers as shown in Fig. 4.4 (a), which enables the extraction of the information on the interface states from the slope of C - V curves near the threshold voltage. This is in contrast to the C - V curves of MIS heterojunction diodes with thick AlGaIn layers, the slopes in which no longer reflect the interface states because the Fermi level is far below the valence band maximum of AlGaIn at the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interfaces around the threshold voltage as shown in Fig. 4.4 (b). The MIS diode without dry etching exhibits a steeper slope of the C - V curve near the threshold voltage as shown in Fig. 4.3, indicating lower trap density at the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interfaces.

To examine the MIS interface properties in detail, the C - V characteristics of both diodes were measured at various frequencies. Figure 4.5 compares the C - V characteristics of both diodes with and without dry etching measured at the frequency varying from 10 Hz to 100 kHz. Here, a larger dispersion is observed in the MIS diode with dry etching, which should be a reflection of the poorer interface quality [Fig. 4.5 (b)]. In addition, a ledge is observed in the C - V curve measured at low frequencies near the threshold voltage. Since interface states with long emission time constants can respond to a measurement signal at the low frequency, the measured capacitance contains more



(a)



(b)

Figure 4.2: $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MIS heterojunction diodes fabricated (a) without and (b) with a dry etching process.

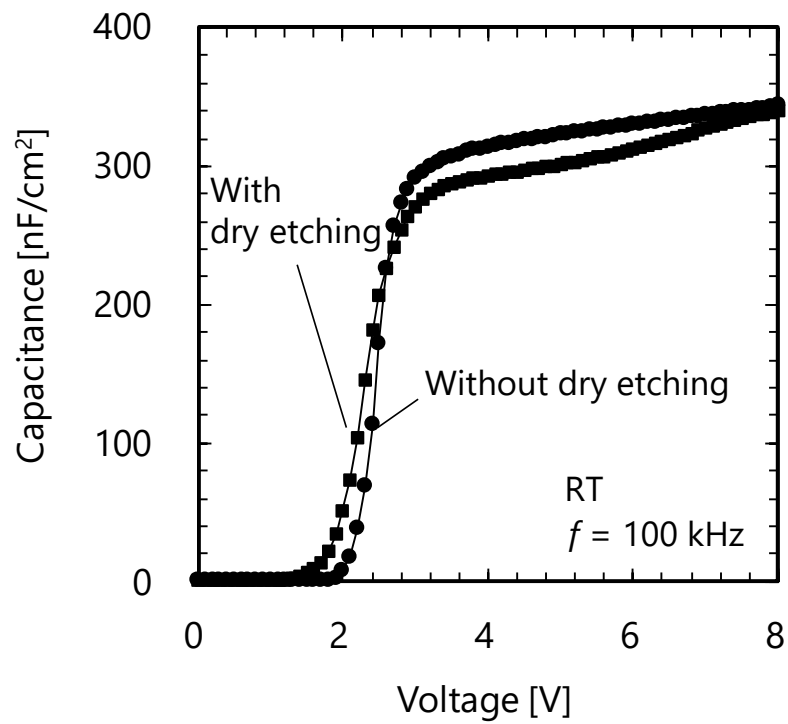
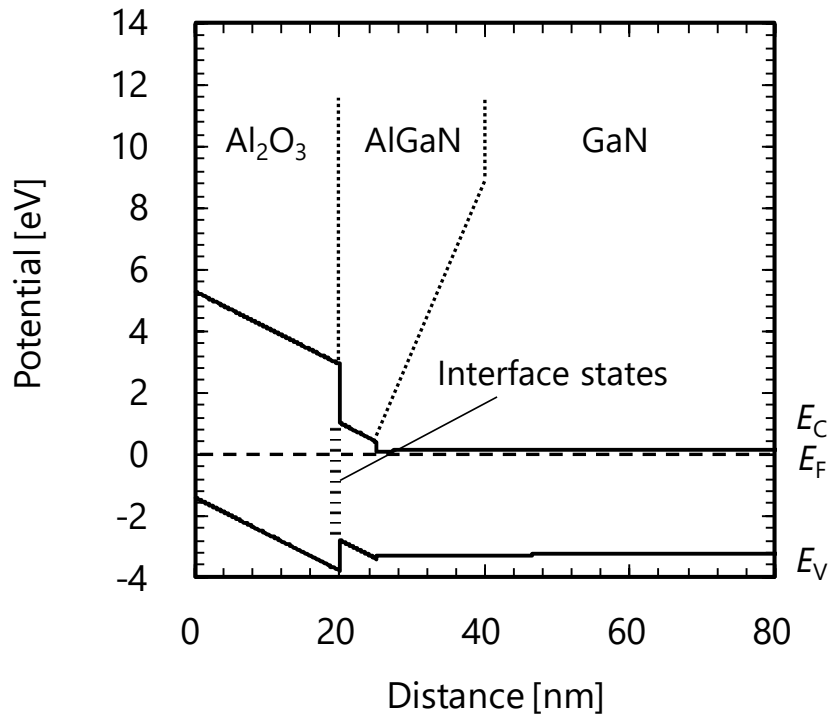
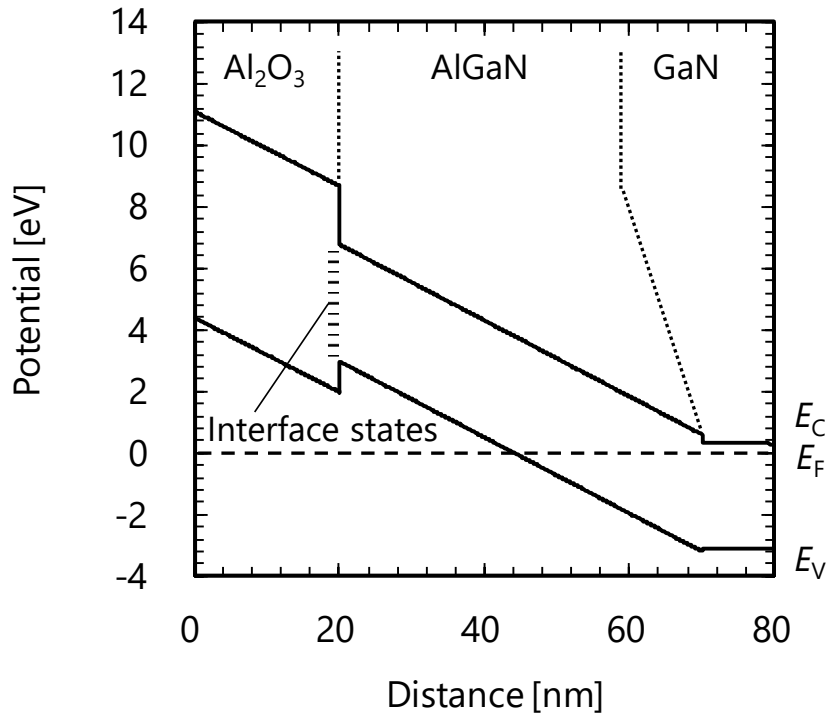


Figure 4.3: C - V characteristics of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MIS diodes with and without dry etching on the AlGaIn surfaces.

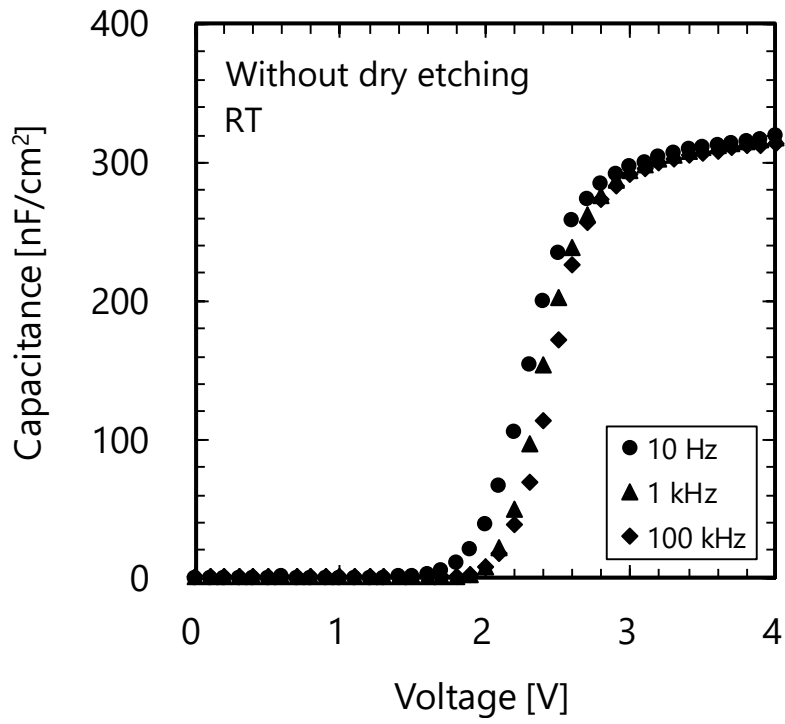


(a)

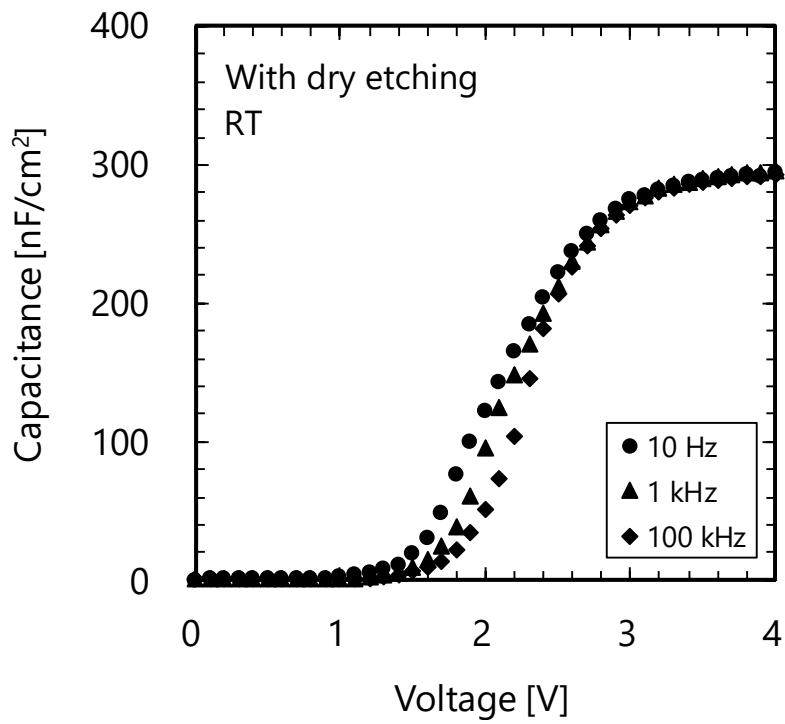


(b)

Figure 4.4: Comparison of the band diagrams for the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MIS-HFETs with (a) thin AlGaIn barrier layer and (b) thick AlGaIn barrier layer near the threshold voltage.



(a)



(b)

Figure 4.5: C - V characteristics of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MIS diodes (a) without and (b) with dry etching on the AlGaIn surfaces at the measurement frequency varying from 10 Hz to 100 kHz.

accurate information about deep interface states. The observed ledge thus indicates the existence of relatively deep traps besides continuous states at the MIS interface.

To estimate the interface states quantitatively, the interface state density was then evaluated by fitting a calculated C - V curve with an experimental one. Figure 4.6 shows a comparison of the calculated and experimental C - V curves of both MIS diodes with and without dry etching. The calculated curves well agree with the experimental ones. Extracted interface-state-density distributions, that is, the interface state distributions assumed in the C - V curve calculations, are shown in Fig. 4.7. The distributions are based on the disorder-induced gap state model assuming donor-like states below the charge neutrality level and acceptor-like states above it [28]. The best fitting result reveals that dry etching increased interface state density especially around 0.4 eV below the conduction band edge of AlGaIn. Since the energy level corresponds to the reported values [29–31], this increase is probably related to nitrogen vacancy near the AlGaIn surfaces, which would be induced by reaction between highly active Cl-based radicals and nitrogen atoms near the AlGaIn surfaces.

4.3.2 Effects of Annealing Process

Control of V_{th} of Al_2O_3 based GaN-MIS devices toward normally-off operations is one of the most critical issues to be solved, the values of which tend to be lower than the designed ones presumably due to the presence of positive fixed charges at the MIS interfaces or/and in the Al_2O_3 films [32, 33]. While several groups have reported the effects of the post-deposition annealing (PDA) on the fixed charges in Al_2O_3 /GaN MIS diodes [34–36], understanding about effects on Al_2O_3 /AlGaIn/GaN MIS heterostructures is required to achieve practical GaN-based MIS-HFETs. For this purpose, effects of the PDA on V_{th} of AlGaIn/GaN MIS heterojunction diodes with the ALD- Al_2O_3 insulators using H_2O vapor and O_2 plasma as the oxidants were investigated.

Figure 4.8 shows the schematic cross section of the fabricated Al_2O_3 /AlGaIn/GaN MIS heterojunction diodes. AlGaIn/GaN heterostructures were grown on Si substrates by metal-organic chemical vapor deposition (MOCVD). 30-nm-thick Al_2O_3 films were deposited on the AlGaIn/GaN heterostructures by ALD at 300 °C, using TMA as the aluminum source, H_2O vapor and O_2 plasma (p - O_2) as the oxidants. To investigate the effects of the PDA, some samples were annealed at 750 °C in a mixture of O_2 and N_2 atmosphere for a period of 90 or 180 min. Ti/Al and Ni/Au electrodes were formed for cathode and anode contacts, respectively. Circular MIS diodes with a diameter of 200 μm were fabricated for the C - V measurements. The anode-cathode spacing was 5 μm .

Figure 4.9 shows the measured C - V characteristics of the fabricated AlGaIn/GaN MIS diodes with (a) H_2O - Al_2O_3 and (b) p - O_2 - Al_2O_3 annealed for different periods. The calculated C - V curves are also plotted with solid lines in Fig. 4.9, in good accordance with the measured ones. Ideal curves calculated without any interface state charges nor fixed charges in the Al_2O_3 films are also shown as references. The extracted fixed charge densities and polarization charge densities plotted as a function of the annealing time are shown in Fig. 4.10. Without annealing, the H_2O - Al_2O_3 contains

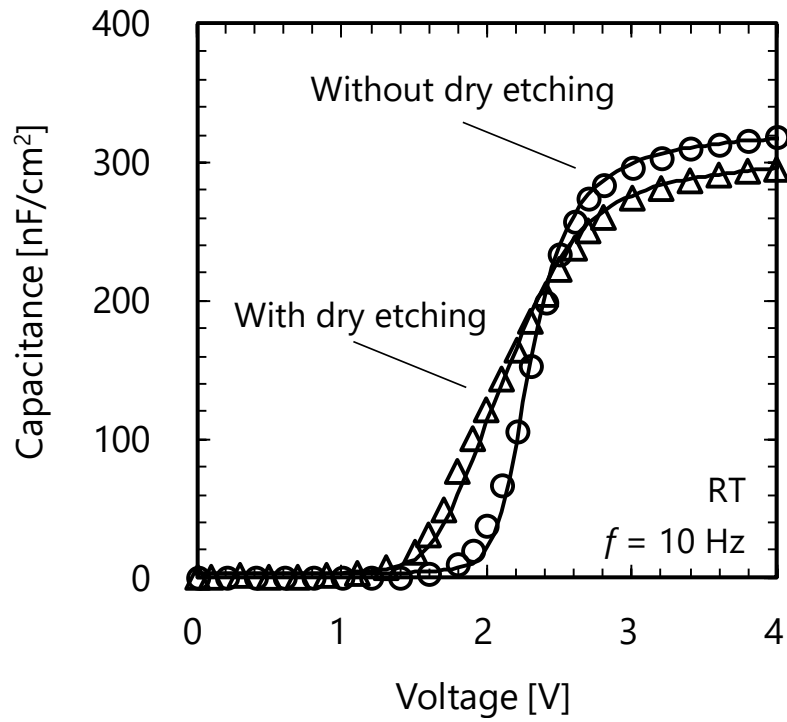


Figure 4.6: Comparison of the calculated and experimental C - V characteristics of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MIS diodes with and without dry etching.

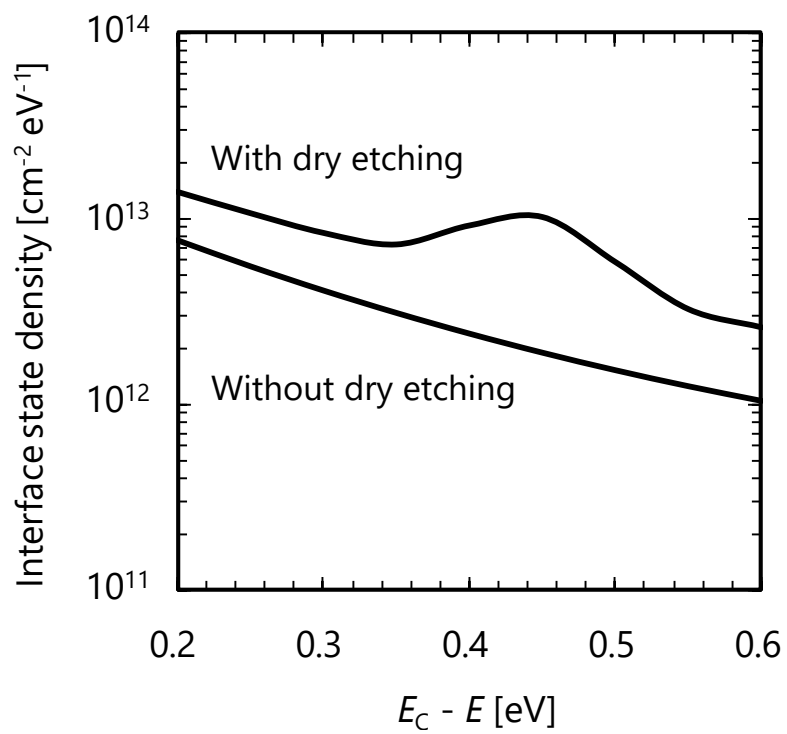


Figure 4.7: Extracted interface-state-density distributions of the Al_2O_3 / AlGaIn/GaN MIS diodes with and without dry etching.

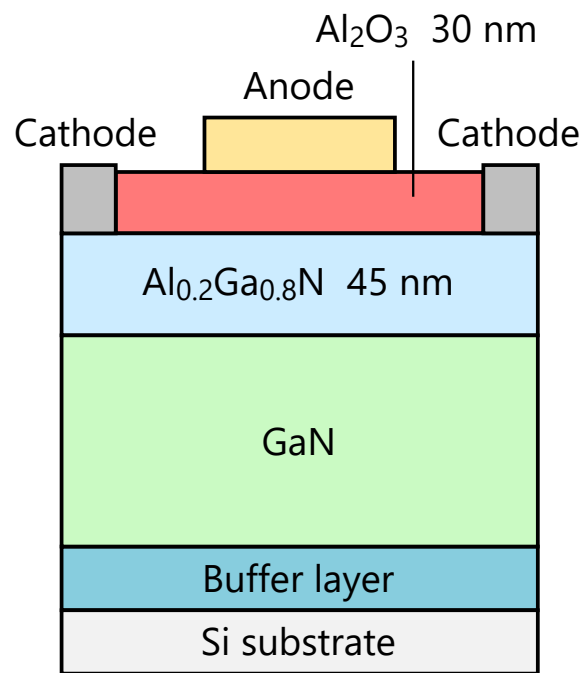
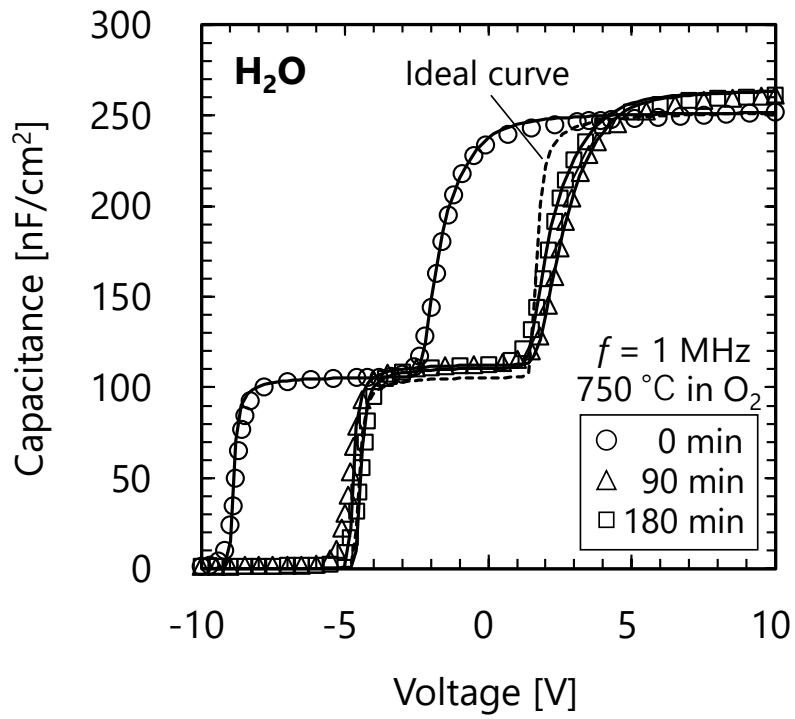
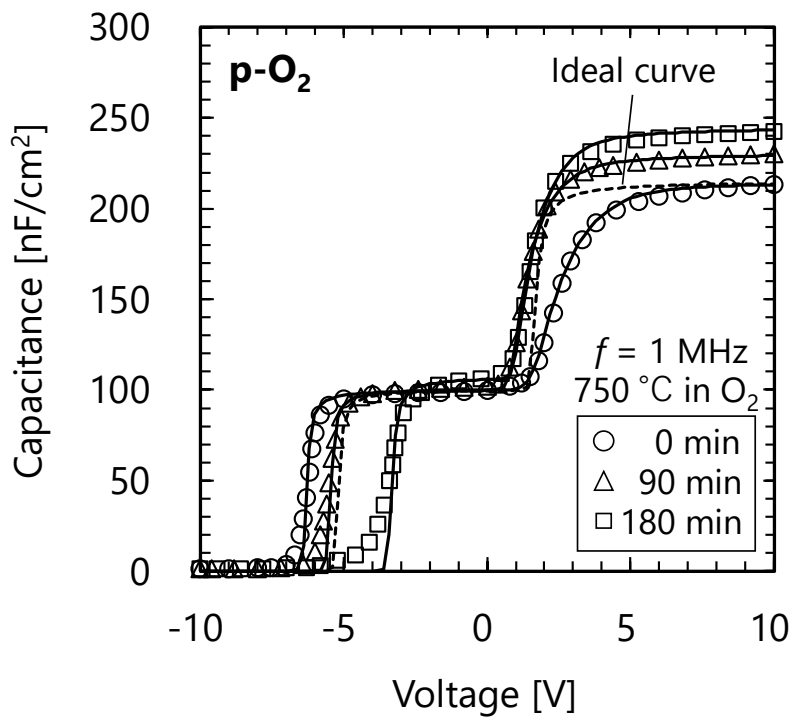


Figure 4.8: Schematic cross section of the fabricated $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MIS heterojunction diodes.



(a)



(b)

Figure 4.9: C - V characteristics of the MIS-diodes with (a) $\text{H}_2\text{O-Al}_2\text{O}_3$ and (b) $\text{p-O}_2\text{-Al}_2\text{O}_3$ for various annealing time. Symbols represent measured curves, while solid lines represent calculated ones.

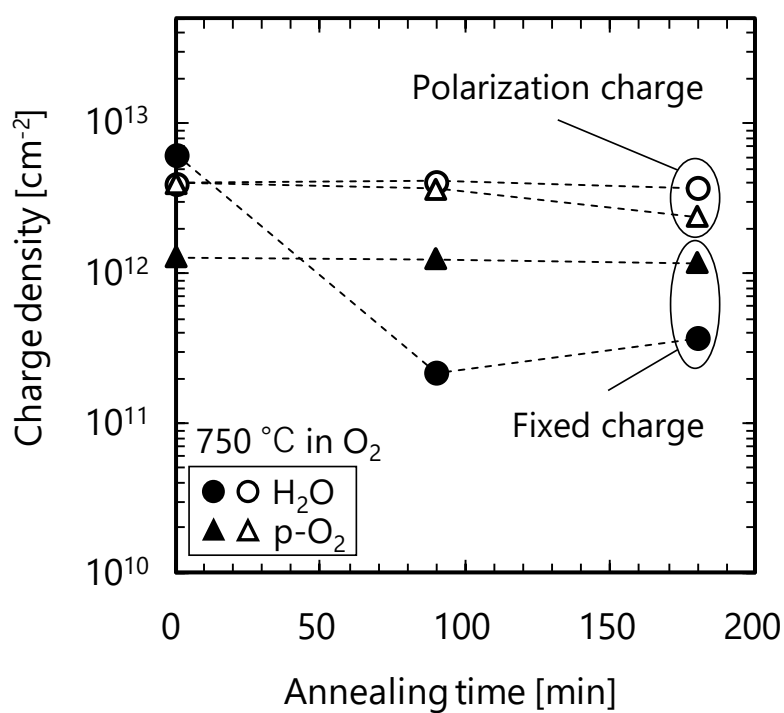


Figure 4.10: Variation of the effective fixed charge density in the Al_2O_3 films and the polarization charge density at the $\text{AlGaIn}/\text{GaIn}$ interfaces as a function of the annealing time.

the higher density of positive fixed charges ($6.2 \times 10^{12} \text{ cm}^{-2}$) than the p-O₂-Al₂O₃ ($1.3 \times 10^{12} \text{ cm}^{-2}$), which results in the lower V_{th} of the MIS-diode with the H₂O-Al₂O₃. According to the first-principles study of Al₂O₃, point defects related to the oxygen deficiency in Al₂O₃, such as oxygen vacancies and aluminum dangling bonds, exhibit positively charged states [37,38]. The H₂O oxidant provides lower reactivity than the p-O₂ oxidant in the ALD process [39–41], which causes the oxygen deficiency leading to the higher density of the positive fixed charges.

By applying the PDA with the annealing time of 90 min, the C - V curve of the H₂O-Al₂O₃ exhibits parallel shift of +4.0 V as shown in Fig. 4.9 (a), corresponding to the reduction of the positive fixed charge density from 6.2×10^{12} to $2.2 \times 10^{11} \text{ cm}^{-2}$. The reduction is probably due to the compensation for the oxygen deficiency with the annealing process in the O₂ atmosphere. In contrast, the fixed charge density in the p-O₂-Al₂O₃ does not change by the PDA, which results in the small V_{th} shift, as shown in Fig. 4.9 (b). This insensitivity to the PDA in O₂ atmosphere should originate from the less deficient situation of oxygen in the as-deposited p-O₂-Al₂O₃. The second step of the C - V curve shifts in the negative direction with its slope getting steeper by the PDA, indicating the reduction of the MIS interface state density. The extracted interface state density in the p-O₂-Al₂O₃/AlGaN MIS interface with the PDA ranged from 9×10^{11} to $2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ near the conduction band edge, which is less than a quarter of that in the as-deposited p-O₂-Al₂O₃/AlGaN MIS interface. The frequency dispersion in the C - V characteristics was observed only in the p-O₂-Al₂O₃-MIS diode without the PDA, which should support this tendency. The increase of capacitance value by the PDA at the gate voltage over 5 V corresponds to the decrease of the Al₂O₃ thickness from 32 nm to 30 nm confirmed through the transmission electron microscope analysis. Instead of the reduction in the fixed charge density in Al₂O₃, the reduction in the polarization charge density from 3.6×10^{12} to $2.5 \times 10^{12} \text{ cm}^{-2}$ yielded the V_{th} shift of +2.0 V in the p-O₂-Al₂O₃ MIS-diodes by the PDA with the longer annealing time of 180 min. Because the p-O₂-Al₂O₃/AlGaN MIS interface was exposed to the highly reactive p-O₂ at the beginning of the Al₂O₃ deposition, oxidation of the AlGaN surface should be more promoted as compared with the H₂O oxidant as reported in the Al₂O₃/GaN MIS interface [42]. The excessive oxygen atoms substitute for the nitrogen sites in AlGaN while forming deep electron traps [43], which can reduce the sheet carrier density at the AlGaN/GaN interface [44]. Hence the author believes that the reduction of the polarization charge density in the p-O₂-Al₂O₃ MIS diode reflects the reduced sheet carrier density in this manner. Assuming that all the reduction of the sheet carrier density is attributed to electron capturing by the deep traps, the trap density is $1.1 \times 10^{12} \text{ cm}^{-2}$, which is almost comparable to the previously reported value [45]. Further investigation is required to confirm the validity of this speculation.

4.3.3 Effects of Nitrogen Incorporation into Al₂O₃

To obtain the stable MIS interface properties, improvement in the properties of insulator is of vital importance. Several reports have pointed out the relations between traps in Al₂O₃ films and

instabilities in V_{th} [46–48], mentioning the importance of reducing traps in Al_2O_3 films as well as interface state density at MIS interfaces. As for reduction of traps in Al_2O_3 films, it has been reported that nitrogen incorporation into Al_2O_3 is effective to reduce the number of electron traps in the Al_2O_3 gate insulators of Si and SiC MISFET [49, 50]. Thus effects of the nitrogen incorporation into Al_2O_3 on AlGaIn/GaN heterostructures were investigated to examine its validity in GaN based MIS devices.

The structures of the fabricated MIS diodes are basically same as Fig. 4.8 except that nitrogen is incorporated into the Al_2O_3 films. The nitrogen incorporated Al_2O_3 is hereinafter referred to as AlON (Aluminum OxyNitride). AlGaIn/GaN heterostructures grown on Si substrates were used in this study. 30-nm-thick AlON films were deposited on the AlGaIn/GaN heterostructures by ALD at 300 °C. Incorporation of nitrogen into Al_2O_3 films was performed by combining deposition of Al_2O_3 and AlN. The precursors were TMA and O_2 plasma for Al_2O_3 , while TMA and NH_3 plasma were used for AlN. The nitrogen content in the deposited AlON films was 10 %, which was confirmed by X-ray photoelectron spectroscopy (XPS).

Figure 4.11 compares the C - V characteristics of the fabricated MIS diodes with AlON and Al_2O_3 gate insulators, where the calculated C - V curves are also plotted with solid lines. The AlON MIS diodes exhibit steeper slope at the second step in the measured C - V curve than the Al_2O_3 MIS diodes, indicating lower interface state density at the MIS interfaces. The extracted interface state density at the AlON/AlGaIn MIS interfaces was $8 \sim 9 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ near the conduction band edge of AlGaIn, which was one-sixth as low as at the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ MIS interfaces. It has been reported that radical treatment using nitrogen plasma prior to insulator deposition is effective for removing surface contaminations and premature native oxides [46, 51]. Thus, the NH_3 plasma used for incorporating nitrogen should be effective for pretreatment on the AlGaIn surfaces, leading to the lower interface state density.

Figure 4.12 shows the value of the threshold voltage shift in the C - V characteristics as a function of the maximum gate voltage. The threshold voltage shift is effectively suppressed in AlON MIS diodes, indicating that AlON has higher immunity against electron injection than Al_2O_3 . Charge density contributing to the threshold voltage shift is $3 \times 10^{11} \text{ cm}^{-2}$ for AlON at the maximum gate voltage of 6 V, which is less than a half of Al_2O_3 ($8 \times 10^{11} \text{ cm}^{-2}$). According to the results of first-principle calculations, O-vacancies in Al_2O_3 generate a defect level, which can be eliminated by incorporation of nitrogen [52]. The reduction of negative charges in AlON after applying positive gate voltage should be attributed to the reduced defect level as compared with Al_2O_3 . The incorporation of nitrogen into Al_2O_3 is thus promising to obtain stable gate characteristics of GaN-based MIS devices.

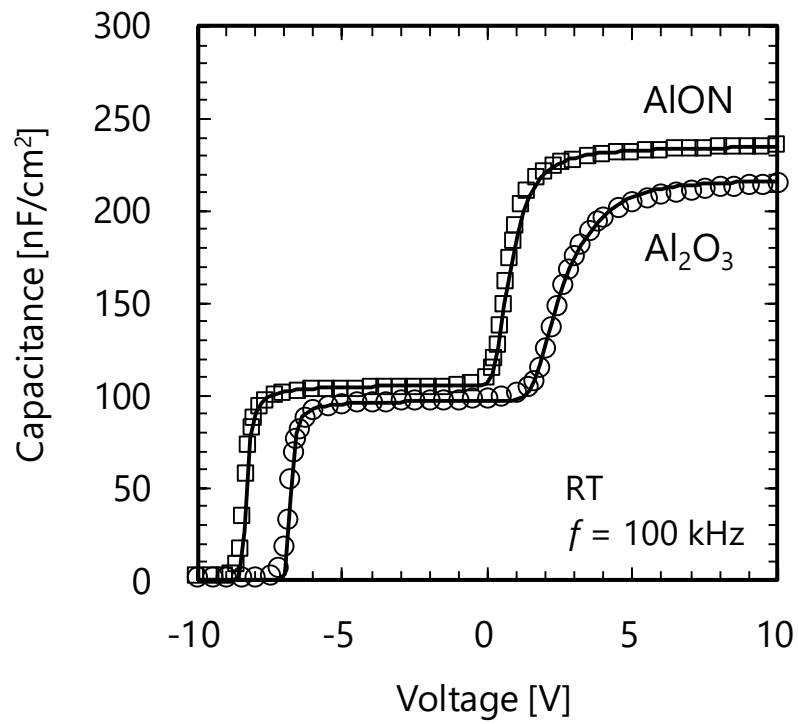


Figure 4.11: Comparison of the C-V characteristics between the AlON/AlGaIn/GaN MIS diode and the Al₂O₃/AlGaIn/GaN MIS diode. Symbols represent measured curves, while solid lines represent calculated ones.

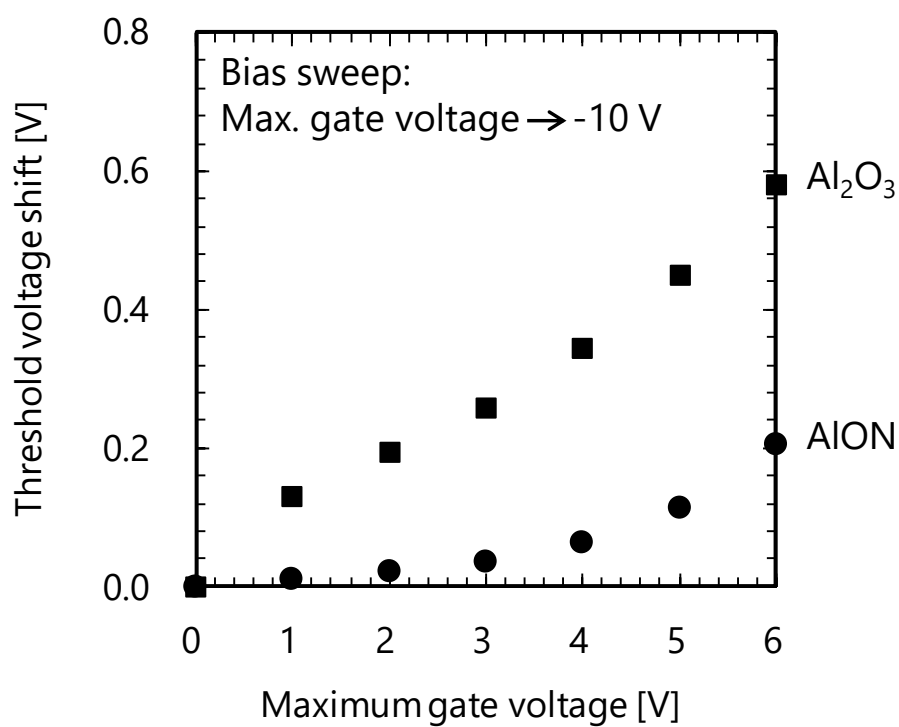


Figure 4.12: The value of the threshold voltage shift in C - V characteristics as a function of the maximum gate voltage.

4.4 Discussion

As described in this chapter, device fabrication processes affect the charges at the MIS interfaces and in the Al_2O_3 films. Here, effects of such charges on the V_{th} is described in detail. The V_{th} of an AlGaIn/GaN MIS-HFET is given by the following equation [53]:

$$V_{\text{th}} = \phi_b - \Delta E_C - \phi_F - \left(\frac{t_{\text{ox}}}{\varepsilon_{\text{ox}}} + \frac{t_{\text{AlGaIn}}}{\varepsilon_{\text{AlGaIn}}} \right) \sigma_{\text{AlGaIn/GaN}} - \frac{t_{\text{ox}}}{\varepsilon_{\text{ox}}} (qN_{\text{surf}} - \sigma_{\text{AlGaIn}}) - \frac{t_{\text{ox}}}{\varepsilon_{\text{ox}}} q \left(N_{\text{it}} + N_{\text{ox,intf}} + \frac{t_{\text{ox}}}{2} N_{\text{ox,bulk}} \right), \quad (4.1)$$

where ϕ_b is the metal barrier height, ΔE_C is the total offset of conduction band edge at $\text{Al}_2\text{O}_3/\text{AlGaIn}$ and AlGaIn/GaN , and ϕ_F is energy difference between the conduction band edge and the Fermi level in the GaN bulk; t is the thickness, ε is the permittivity, and the subscripts ox and AlGaIn refer to the Al_2O_3 and AlGaIn layer, respectively; $\sigma_{\text{AlGaIn/GaN}}$ and σ_{AlGaIn} are the total polarization sheet charges at an AlGaIn/GaN interface and at an AlGaIn surface; N_{surf} is a surface donor density at the AlGaIn surface, N_{it} represents the net charge density of $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface traps below the Fermi level, $N_{\text{ox,intf}}$ and $N_{\text{ox,bulk}}$ are the fixed charge density of near interface traps and bulk traps in the Al_2O_3 film, respectively.

The last term in Eq. (4.1) represents charges at MIS interfaces and in an insulator. N_{it} should be eliminated to achieve the stable gate characteristics because of their unstable properties, while there's room for consideration about negative charges in an insulator since negative charges can shift threshold voltage in a positive direction and they are thus beneficial in terms of normally-off operations as far as the charges are stable. Furthermore, reduction of surface donor density is great potential to achieve high threshold voltage offered by large negative sheet charge originate from polarization of AlGaIn, although the existence of the surface donor is still in debate [54]. While the surface donor is believed to be formed already during growth of the heterostructures, reduction of its density by pretreatment of insulator deposition, deposition of insulators or/and post-deposition annealing would enable the GaN-based MIS-HFETs with the normally-off operations or even much higher threshold voltage.

4.5 Summary

Effects of the device fabrication processes, including dry-etching, post-deposition annealing, and incorporation of nitrogen into Al_2O_3 , on the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ MIS interface properties have been investigated by analyzing C - V characteristics of $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MIS heterojunction diodes the Al_2O_3 insulators of which were deposited by atomic layer deposition (ALD).

The dry-etching process increased an interface state density from the middle of 10^{12} to $10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, especially around 0.4 eV below the conduction band edge of AlGaIn, which would be related to the

nitrogen vacancies. The dry-etching process would induce the desorption of nitrogen atoms from the AlGaIn surface, hence the process should be avoided to obtain the stable MIS interface properties.

The post-deposition annealing (PDA) at 750 °C in O_2 atmosphere reduced the positive fixed charges in the Al_2O_3 films or/and $\text{Al}_2\text{O}_3/\text{AlGaIn}$ MIS interfaces, which causes the positive shift in threshold voltage. Dependency of the reduction on an oxidant used in deposition of Al_2O_3 implied that an origin of the positive fixed charges were oxygen deficiency in Al_2O_3 . The PDA leading to the positive shift in threshold voltage is advantageous for achieving the normally-off operations.

Nitrogen incorporation into Al_2O_3 films was performed by NH_3 -plasma during the ALD process. AlON (N incorporate Al_2O_3) with N composition of 10 % significantly suppressed the threshold voltage shift in the C - V curves. The negative charge density in the AlON insulators contributed to the threshold voltage shift was estimated at $3 \times 10^{11} \text{ cm}^{-2}$ for gate voltage of 6 V, which was a half as low as that in the Al_2O_3 insulators, implying reduction of electron traps in the insulators. The nitrogen incorporation into Al_2O_3 is thus promising for achieving the stable gate characteristics.

References

- [1] B. J. Baliga, *Semicond. Sci. Technol.* **28**, 074011 (2013).
- [2] T. Kachi, *Jpn. J. Appl. Phys.* **53**, 100210 (2014).
- [3] K. J. Chen, O. Häberlen, A. Lidow, C. L. Tsai, T. Ueda, Y. Uemoto, and Y. Wu, *IEEE Trans. Electron Devices* **64**, 779 (2017).
- [4] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, and D. Ueda, *IEEE Trans. Electron Devices* **54**, 3393 (2007).
- [5] V. Kumar, A. Kuliev, T. Tanaka, Y. Otoki, and I. Adesida, *Electron. Lett.* **39**, 1758 (2003).
- [6] Y. Cai, Y. Zhou, K. M. Lau, and K. J. Chen, *IEEE Trans. Electron Devices* **53**, 2207 (2006).
- [7] T. Mizutani, M. Ito, S. Kishimoto, and F. Nakamura, *IEEE Electron Device Lett.* **28**, 549 (2007).
- [8] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Hwang, *Appl. Phys. Lett.* **86**, 063501 (2005).
- [9] T. Oka and T. Nozawa, *IEEE Electron Device Lett.* **29**, 668 (2008).
- [10] S. Sugiura, Y. Hayashi, S. Kishimoto, T. Mizutani, M. Kuroda, T. Ueda, and T. Tanaka, *Solid-State Electron.* **54**, 79 (2010).
- [11] H. Kambayashi, Y. Satoh, S. Ootomo, T. Kokawa, T. Nomura, S. Kato, and T. P. Chow, *Solid-State Electron.* **54**, 660 (2010).
- [12] Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, K. L. Teo, S. C. Foo, V. Sahmuganathan, T. Xu, and C. H. Lee, *IEEE Electron Device Lett.* **31**, 96 (2010).
- [13] T. Hashizume, K. Nishiguchi, S. Kaneki, J. Kuzmìk, and Z. Yatabe, *Mat. Sci. Semicond. Process.* **78**, 85 (2018).
- [14] M. D. Groner, J. W. Elam, F. H. Fabreguette, and S. M. George, *Thin Solid Films* **413**, 186 (2002).
- [15] J. Robertson and B. Falabretti, *J. Appl. Phys.* **100**, 014111 (2006).
- [16] N. V. Nguyen, O. A. Kirillov, W. Jiang, W. Wang, J. S. Suehle, P. D. Ye, Y. Xuan, N. Goel, K. W. Choi, W. Tsai, and S. Sayan, *Appl. Phys. Lett.* **93**, 082105 (2008).
- [17] M. Miczek, C. Mizue, T. Hashizume, and B. Adamowicz, *J. Appl. Phys.* **103**, 104510 (2008).

- [18] Z. Yatabe, Y. Hori, W. C. Ma, J. T. Asubar, M. Akazawa, T. Sato, and T. Hashizume, *Jpn. J. Appl. Phys.* **53**, 100213 (2014).
- [19] K. Nishiguchi, S. Kaneki, S. Ozaki, and T. Hashizume, *Jpn. J. Appl. Phys.* **56**, 101001 (2017).
- [20] W. Saito, Y. Tanaka, M. Kuraguchi, K. Tsuda, and I. Omura, *IEEE Trans. Electron Devices* **53**, 356 (2006).
- [21] H. W. Choi, S. J. Chua, A. Raman, J. S. Pan, and A. T. S. Wee, *Appl. Phys. Lett.* **77**, 1795 (2000).
- [22] K. Remashan, S. J. Chua, A. Raman, S. Prakash, and W. Liu, *Semicond. Sci. Technol.* **15**, 386 (2000).
- [23] D. Basak, Q. Fareed, K. Nishino, and S. Sakai, *J. Vac. Sci. Technol. B* **18**, 2491 (2000).
- [24] J. Kuzmík, P. Javorka, M. Marso, and P. Kordoš, *Semicond. Sci. Technol.* **17**, L76 (2002).
- [25] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda, *IEEE Trans. Electron Devices* **60**, 3053 (2013).
- [26] M. Fagerlind, F. Allerstam, E. Ö. Sveinbjörnsson, N. Rorsman, A. Kakanakova-Georgieva, A. Lundskog, U. Forsberg, and E. Janzén, *J. Appl. Phys.* **108**, 014508 (2010).
- [27] S. Yang, Z. Tang, K. -Y. Wong, Y. -S. Lin, C. Liu, Y. Lu, S. Huang, and K. J. Chen, *IEEE Electron Device Lett.* **34**, 1497 (2013).
- [28] H. Hasegawa and Y. Ohno, *J. Vac. Sci. Technol. B* **4**, 1130 (1986).
- [29] T. Mizutani, H. Makihara, M. Akita, Y. Ohno, S. Kishimoto, and K. Maezawa, *Jpn. J. Appl. Phys.* **42**, 424 (2003).
- [30] Z.-Q. Fang, D. C. Look, X.-L. Wang, J. Han, F. A. Khan, and I. Adesida, *Appl. Phys. Lett.* **82**, 1562 (2003).
- [31] T. Hashizume, S. Ootomo, T. Inagaki, and H. Hasegawa, *J. Vac. Sci. Technol. B* **21**, 1828 (2003).
- [32] M. Esposto, S. Krishnamoorthy, D. N. Nath, S. Bajaj, T.-H. Hung, and S. Rajan, *Appl. Phys. Lett.* **99**, 133503 (2011).
- [33] S. Ganguly, J. Verma, G. Li, T. Zimmermann, H. Xing, and D. Jena, *Appl. Phys. Lett.* **99**, 193504 (2011).
- [34] C. Ostermaier, H.-C. Lee, S.-Y. Hyun, S.-I. Ahn, K.-W. Kim, H.-I. Cho, J.-B. Ha, and J.-H. Lee, *Phys. Status Solidi C* **5**, 1992 (2008).

- [35] T. Marron, S. Takashima, Z. Li, and T. P. Chow, *Phys. Status Solidi C* **9**, 907 (2012).
- [36] H.-S. Kang, M. S. P. Reddy, D.-S. Kim, K.-W. Kim, J.-B. Ha, Y. S. Lee, H.-C. Choi, and J.-H. Lee, *J. Phys. D* **46**, 155101 (2013).
- [37] B. Shin, J. R. Weber, R. D. Long, P. K. Hurley, C. G. Van de Wall, and P. C McIntyre, *Appl. Phys. Lett* **96**, 152908 (2010).
- [38] M. Choi, A. Janotti, and C. G. Van de Walle, *J. Appl. Phys.* **113**, 044501 (2013).
- [39] J. L. van Hemmen, S. B. S. Heil, J. H. Klootwijk, F. Roozeboom, C. J. Hodson, M. C. M. van de Sanden, and W. M. M. Kessels, *J. Electrochem. Soc.* **154**, G165 (2007).
- [40] H. B. Profijt, S. E. Potts, M. C. M. van de Sanden, and W. M. M. Kessels, *J. Vac. Sci. Technol. A* **29**, 050801 (2011).
- [41] K. B. Jinesh, J. L. van Hemmen, M. C. M. van de Sanden, F. Roozeboom, J. H. Klootwijk, W. F. A. Besling, and W. M. M. Kessels, *J. Electrochem. Soc.* **158**, G21 (2011).
- [42] S. Ozaki, T. Ohki, M. Kanamura, N. Okamoto, and T. Kikkawa, *Jpn. J. Appl. Phys.* **52**, 11NG04 (2013).
- [43] T. Mattila and R. M. Nieminen, *Phys. Rev. B* **54**, 16676 (1996).
- [44] S. T. Bradley, A. P. Young, L. J. Brillson, M. J. Murphy, W. J. Schaff, and L. F. Eastman, *IEEE Trans. Electron Devices* **48**, 412 (2001).
- [45] E. Arslan, S. Bütün, S. B. Lisesivdin, M. Kasap, S. Ozelik, and E. Ozbay, *J. Appl. Phys.* **103**, 103701 (2008).
- [46] S. Liu, S. Yang, Z. Tang, Q. Jiang, C. Liu, M. Wang, B. Shen, and K. J. Chen, *Appl. Phys. Lett.* **106**, 051605 (2015).
- [47] T.-L. Wu, D. Marcon, B. Bakeroort, B. D. Jaeger, H. C. Lin, J. Franco, S. Stoffels, M. V. Hove, R. Roelofs, G. Groeseneken, and S. Decoutere, *Appl. Phys. Lett.* **107**, 093507 (2015).
- [48] D. Bisi, S. H. Chan, X. Liu, R. Yeluri, S. Keller, M. Meneghini, G. Meneghesso, E. Zanoni, and U. K. Mishra, *Appl. Phys. Lett.* **108**, 112104 (2016).
- [49] K. Manabe, K. Endo, S. Kamiyama, T. Iwamoto, T. Ogura, N. Ikarashi, T. Yamamoto, and T. Tatsumi, *IEICE Trans. Electron.* **E87-C**, 30 (2004).
- [50] T. Hosoi, S. Azumo, Y. Kashiwagi, S. Hosaka, R. Nakamura, S. Mitani, Y. Nakano, H. Asahara, T. Nakamura, T. Kimoto, T. Shimura, and H. Watanabe, *IEDM Tech. Dig.*, 2012, p. 159.

- [51] J. Son, V. Chobpattana, B. M. McSkimming, and S. Stemmer, *J. Vac. Sci. Technol. A* **33**, 020602 (2015).
- [52] E. Kojima, K. Chokawa, H. Shirakawa, M. Araidai, T. Hosoi, H. Watanabe, and K. Shiraishi, *Appl. Phys. Express* **11**, 061501 (2018).
- [53] M. Ľapajna and J. Kuzmík, *Appl. Phys. Lett.* **100**, 113509 (2012).
- [54] I. P. Smorchkova, C. R. Elsass, J. P. Ibbetson, R. Vetury, B. Heying, P. Fini, E. Haus, S. P. DenBaars, J. S. Speck, and U. K. Mishra, *J. Appl. Phys.* **86**, 4520 (1999).

Chapter 5

AlGaIn/GaN MIS-HFETs for Power Switching Applications

5.1 Introduction

AlGaIn/GaN heterojunction field-effect transistors (HFETs) are very promising for power switching applications owing to their potential for high speed switching that would make the switching system far compact. The metal-insulator-semiconductor (MIS) gate structure is favorable for such applications because introduction of the gate insulators over the heterostructures can reduce the gate leakage current while serving normally-off operations, which enables large gate-voltage swing leading to fast switching operations. However, such fast switching operations by satisfactorily high current and high voltage MIS-gate GaN transistors have never reported presumably due to the instability of the gate characteristics [1, 2]. As described in Chapter 4, device fabrication processes affect the stability of the gate characteristics in the MIS-gate devices. Combining the appropriate processes will enable the fabrication of the AlGaIn/GaN MIS-HFETs with the stable gate characteristics.

In this chapter, a normally-off AlGaIn/GaN MIS-HFET on a Si substrate with high current and high voltage capability exhibiting the stable gate characteristics is demonstrated. Based on the results in Chapter 4, a novel fabrication process flow is proposed to achieve stable gate characteristics, including a process to form recessed gate structures, deposition of gate insulators, and post deposition annealing. The resultant device performance such as stable gate characteristics and fast switching operations exhibited by the fabricated AlGaIn/GaN MIS-HFETs is described.

5.2 Normally-off AlGaIn/GaN MIS-HFETs

5.2.1 Device Structure

The schematic cross section of the fabricated AlGaIn/GaN MIS-HFET is illustrated in Fig. 5.1. The AlON gate insulators, which is nitrogen incorporated Al_2O_3 , suppress the threshold voltage shifts and

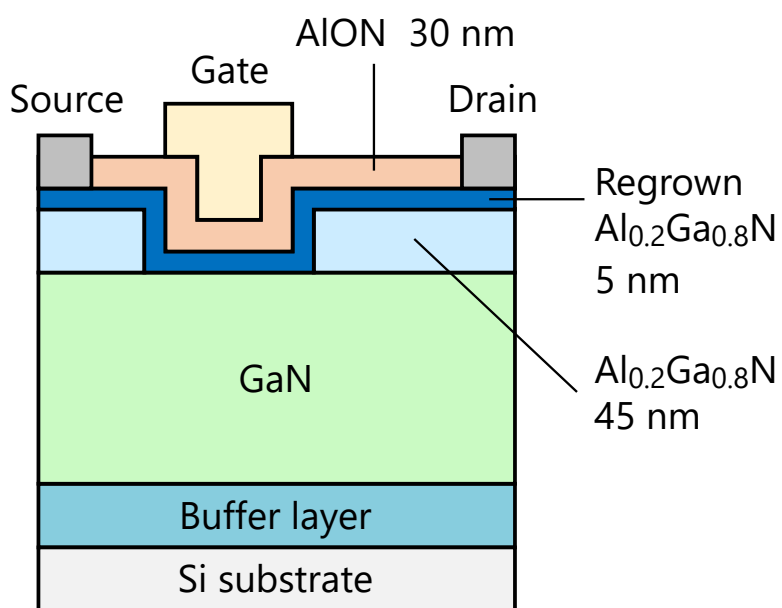


Figure 5.1: Schematic cross section of the fabricated AlGaN/GaN MIS-HFET.

reduce hysteresis in the transfer characteristics as described in Chapter 4. The recessed gate structures are introduced to reduce the parasitic resistance while achieving the normally-off operations. Since the sheet carrier density at the AlGaIn/GaN heterojunction depends on the AlGaIn thickness, thinning the AlGaIn layer is required to obtain the normally-off operations. The on-state resistance, however, increases with the reduction of the sheet carrier density in access regions in the conventional planar structures [3–5]. The recessed gate structures, where the AlGaIn layer is thinned only under the gate electrodes, are thus effective to break this trade-off. To avoid introducing processing damage into the MIS interfaces, a regrowth technique was adopted to form the structures.

5.2.2 Device Fabrication Process

The fabrication process flow of the presented AlGaIn/GaN MIS-HFETs is shown in Fig. 5.2. The $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}/\text{GaN}$ heterostructure was epitaxially grown on a Si substrate by MOCVD. After the AlGaIn layer was removed selectively in gate regions by ICP dry etching, 5-nm-thick AlGaIn layers were regrown over the grooved structures of the AlGaIn/GaN epitaxial layers by MOCVD. This process enables fabrication of the recessed gate structures without introducing the processing damage deteriorative for the MIS interface characteristics described in Chapter 4. In addition, this regrowth process provides more precise control of the AlGaIn layer than the conventional dry etching process, resulting in the good reproducibility of the threshold voltage [6]. A 30-nm-thick AlON insulator was then deposited by ALD, nitrogen composition of which was 10 %. The post deposition annealing (PDA) was carried out in oxygen atmosphere at 750 °C for 180 min. As described in Chapter 4, this PDA process causes the positive shift of the threshold voltage, ensuring the normally-off operations of the fabricated AlGaIn/GaN MIS-HFETs. Ti/Al for source and drain electrodes, and Ni/Au for gate electrodes were formed by electron beam evaporation. Figure 5.3 shows a cross-sectional transmission electron microscopic (TEM) image of the fabricated AlGaIn/GaN MIS-HFET. A gate length and gate-drain spacing are designed to be 2 and 10 μm , respectively, to achieve breakdown voltage over 600 V. A top-view photograph of the fabricated MIS-HFET with the gate width of 100 μm is shown in Fig. 5.4. The above-mentioned fabrication process has enough reproducibility to fabricate such large devices with the chip size of 2.3 mm $\times$ 2.3 mm.

5.3 Performance of Fabricated MIS-HFETs

Figure 5.5 shows the transfer characteristics of the fabricated AlON/AlGaIn/GaN MIS-HFETs with the gate width of 0.1 mm measured for various maximum gate voltages. The MIS-HFETs exhibited the normally-off operations, the threshold voltage V_{th} of which was 1.4 V. In addition, the V_{th} is not changed even by increasing gate voltage up to 10 V. This stable V_{th} should be attributed to AlON gate insulators, enabling application of high gate voltage leading to high speed on-state switching.

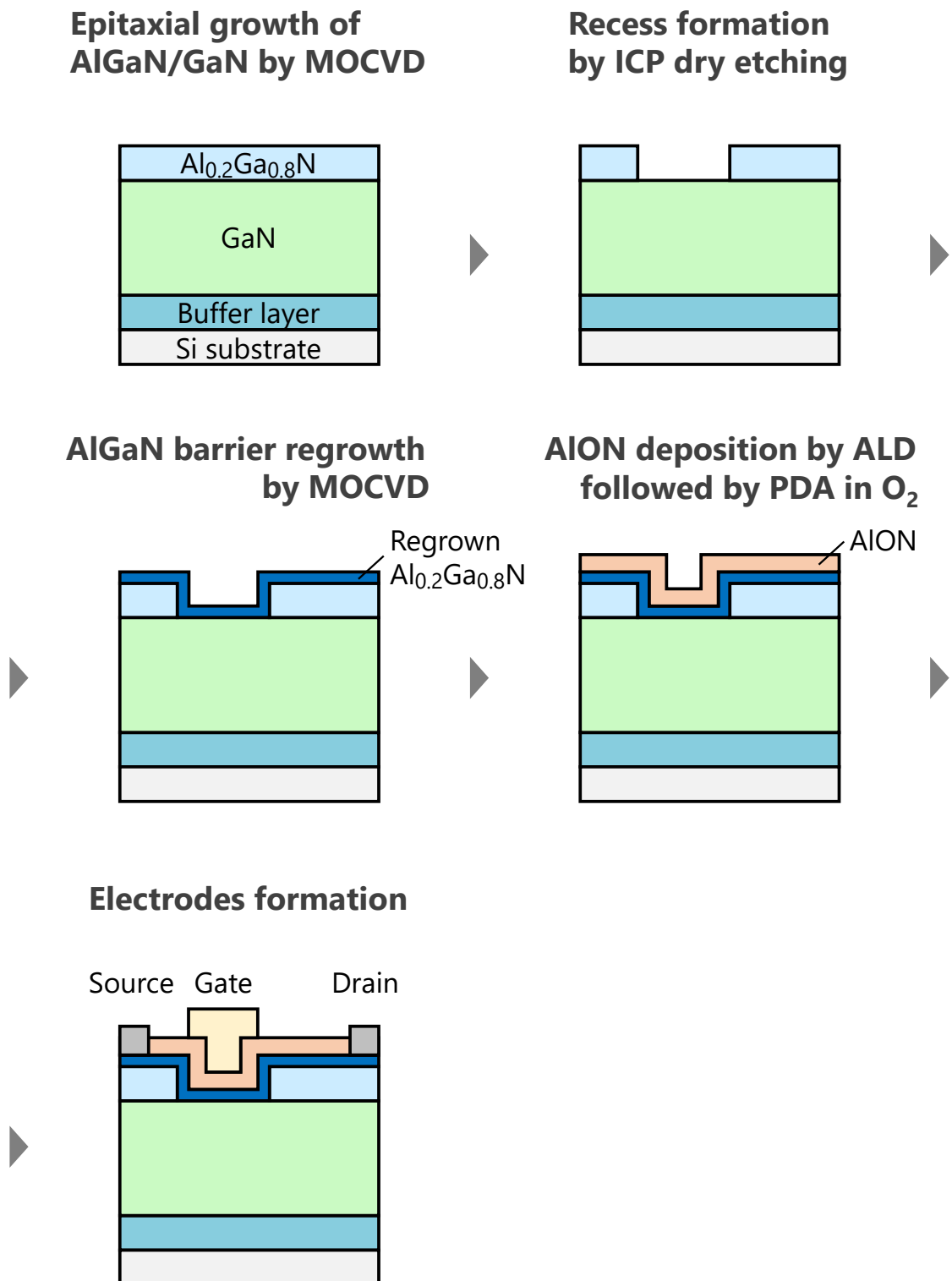


Figure 5.2: Fabrication-process flow of the AlGaN/GaN MIS-HFETs using AlON gate insulator.

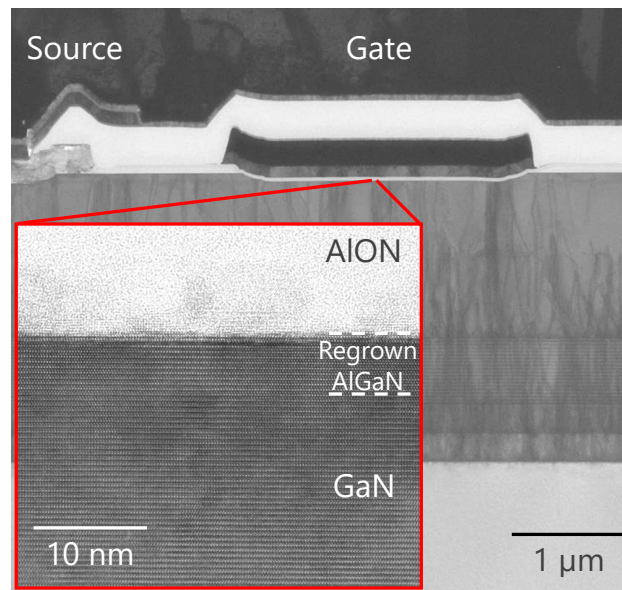


Figure 5.3: Cross-sectional TEM image of the fabricated AlON/AlGaN/GaN MIS-HFET.

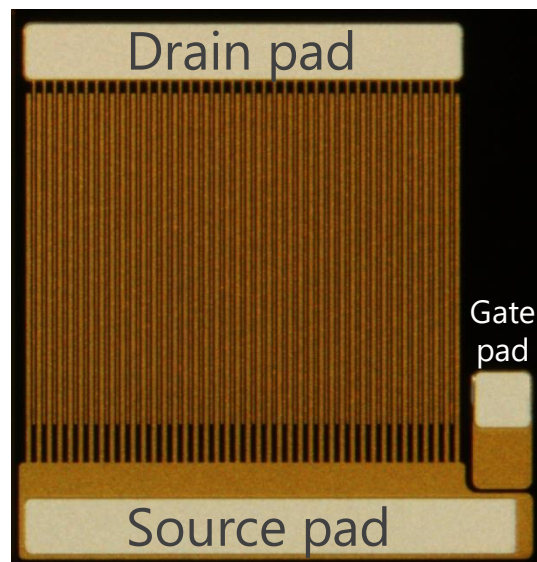


Figure 5.4: Top-view photograph of the fabricated AlON/AlGaN/GaN MIS-HFET with the gate width of 100 nm.

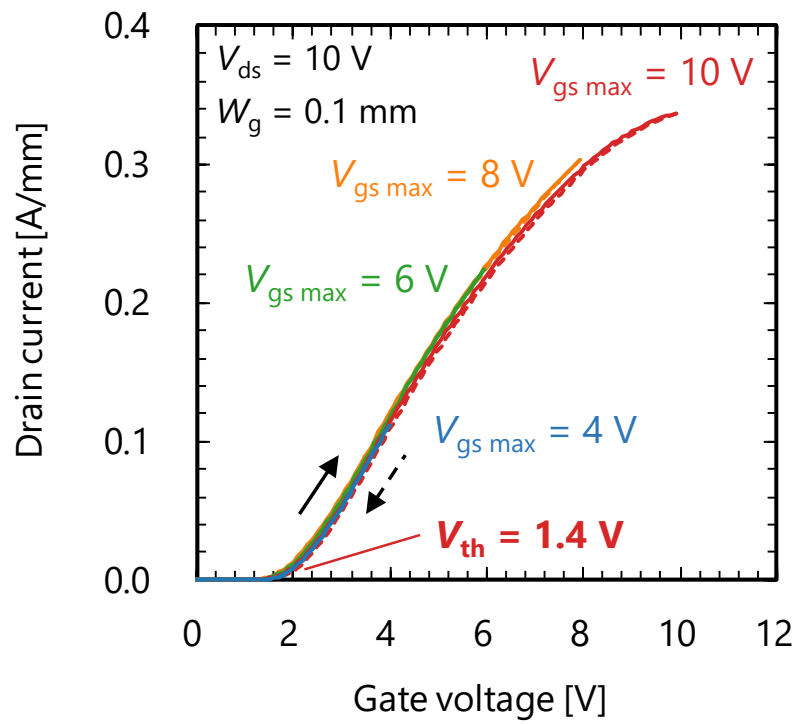


Figure 5.5: Transfer characteristics of the AlON/AlGaIn/GaN MIS-HFETs for various maximum gate voltages.

To confirm switching performance with high current and high voltage, the AlON/AlGaN/GaN MIS-HFETs with the gate width of 100 μm were characterized. Figure 5.6 shows the gate current-voltage ($I_{\text{gs}}-V_{\text{gs}}$) characteristics of the fabricated MIS-HFET. The gate leakage current is as low as 1 μA at the gate voltage of 15 V, indicating that the fabricated device has enough high gate breakdown voltage for the measurement of switching performance. The on-state and off-state drain current-voltage ($I_{\text{ds}}-V_{\text{ds}}$) characteristics are shown in Figs. 5.7 and 5.8, respectively. The maximum drain current reaches 25 A at the V_{gs} of 10 V. The obtained on-state resistance (R_{on}) is as low as 270 m Ω that is reduced by 84 % by introducing the recessed gate structures as compared with the conventional planar devices. The off-state leakage current is successfully reduced by the process optimization and the breakdown voltage reaches 730 V.

The switching characteristics were measured for the 25 A / 730 V devices with an off-state drain voltage of 400 V, an on-state drain current of 10 A, and an inductive load by using the test circuit the schematic diagram of which is shown in Fig. 5.9. The devices were packaged in the surface-mount packages to minimize parasitic inductance. Figure 5.10 shows the measured switching characteristics at gate voltage of 10 V, where very fast switching operations with both turn-on and turn-off transition time as short as a few nanoseconds were experimentally confirmed. The measured switching speed (dV/dt) for the turn-on and turn-off transitions are 151 V/ns and 154 V/ns, respectively. Here, the switching speed is defined as the drain voltage change during the time it takes to fall from 90 to 10 % or to rise from 10 to 90 % of the maximum drain voltage. High current density thanks to the material properties of GaN enables a shrink of device size for a certain rated current as compared with conventional Si devices, leading to reduction of parasitic capacitance and thus shortening of switching time. These values are sufficiently fast for practical use in power conversion systems operating in a MHz range.

5.4 Discussion

The fabricated AlON/AlGaN/GaN MIS-HFETs exhibited the stable threshold voltage for increasing gate voltage up to 10 V, which enables shortening of switching time for turn-on transitions. Figure 5.11 shows switching time for turn-on, that is the sum of delay time and transition time, as a function of gate voltage. The switching time is reduced from 8 to 4 ns by increasing the gate voltage from 5 to 10 V.

The delay time for turn-on (t_d) is given by

$$t_d = R_g(C_{\text{gs}} + C_{\text{gd}}) \ln \frac{V_{\text{gs}}}{V_{\text{gs}} - V_{\text{th}}}, \quad (5.1)$$

where R_g is external gate resistance, C_{gs} and C_{gd} are gate-source and gate-drain parasitic capacitance, V_{th} and V_{gs} are threshold voltage and applied gate voltage [7]. Substituting the measured V_{th} results

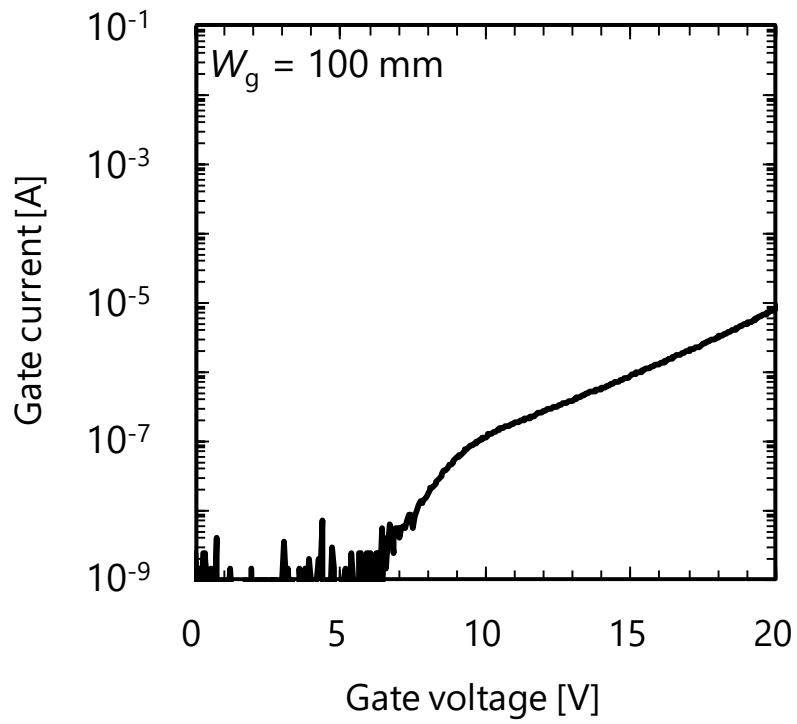


Figure 5.6: Gate current-voltage characteristics of the fabricated AlON/AlGaIn/GaN MIS-HFET with the gate width of 100 mm.

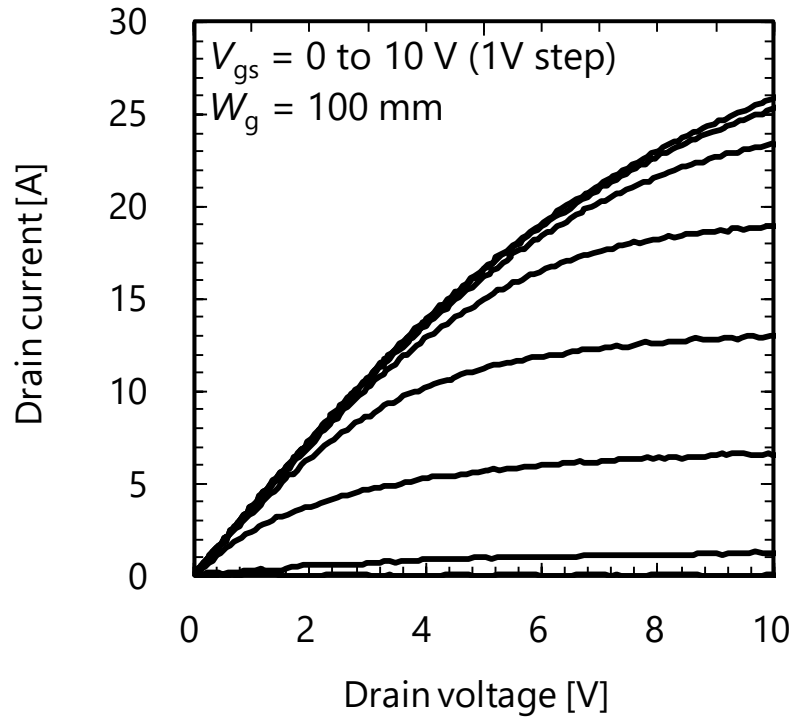


Figure 5.7: On-state drain current-voltage characteristics of the fabricated AlON/AlGaIn/GaN MIS-HFET.

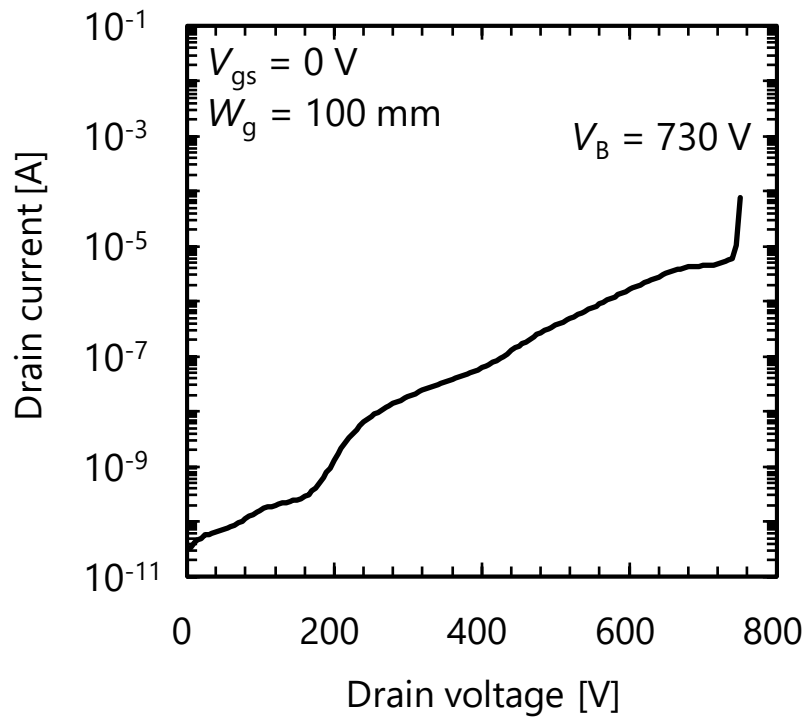


Figure 5.8: Off-state drain current-voltage characteristics of the fabricated AlON/AlGaIn/GaN MIS-HFET measured at the gate voltage (V_{gs}) of 0 V.

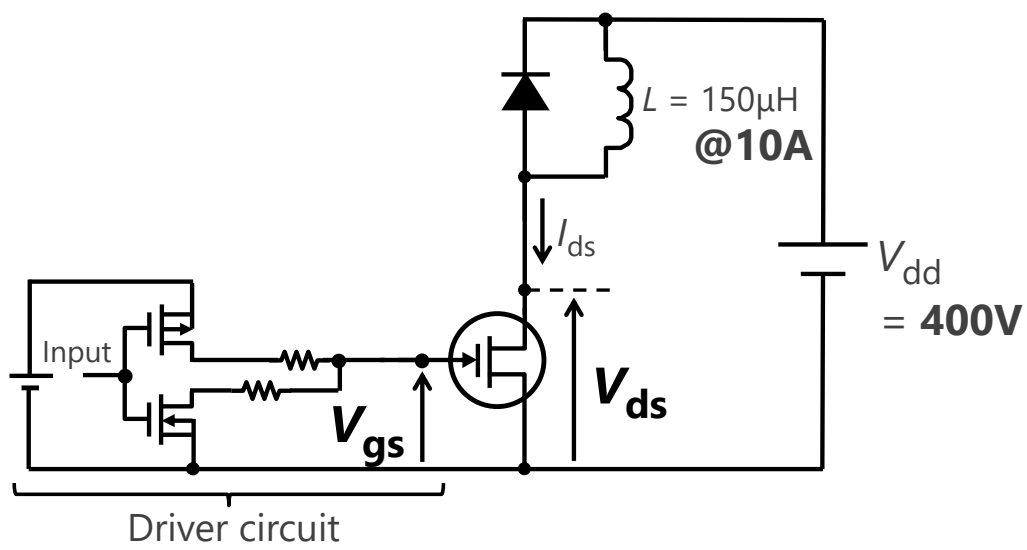
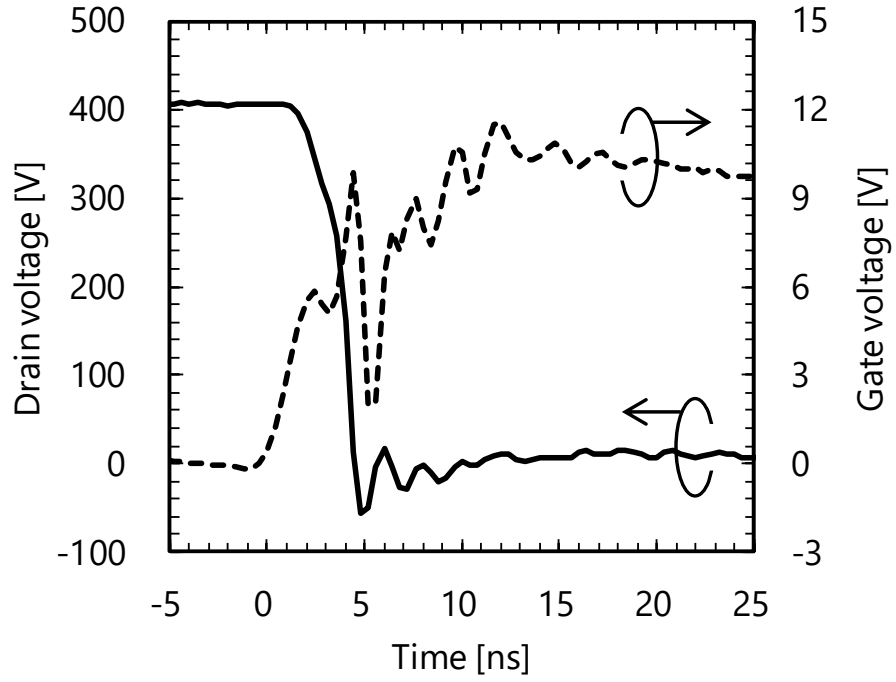
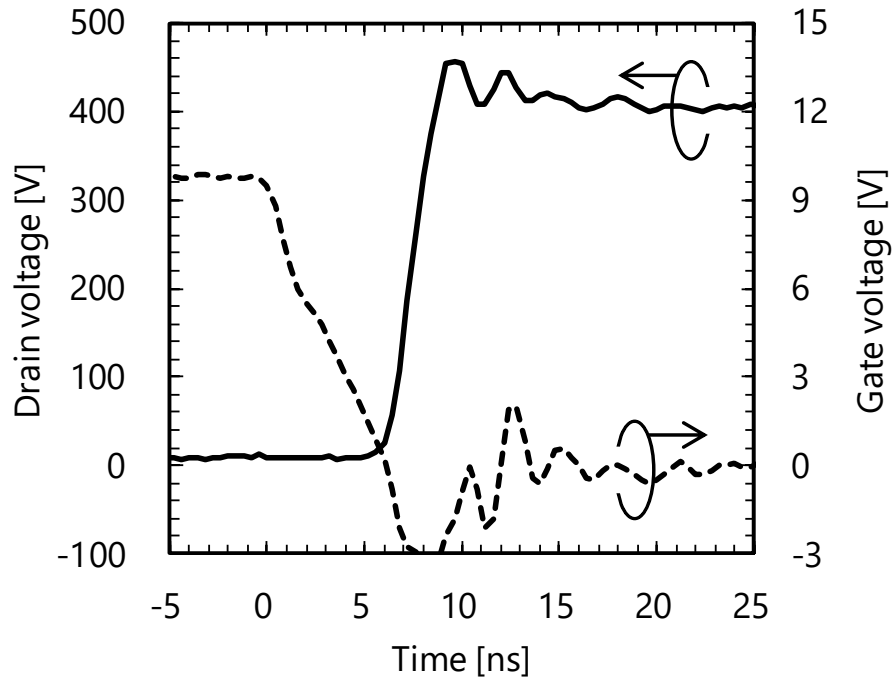


Figure 5.9: Schematic test circuit diagram for the measurement of the switching characteristics.

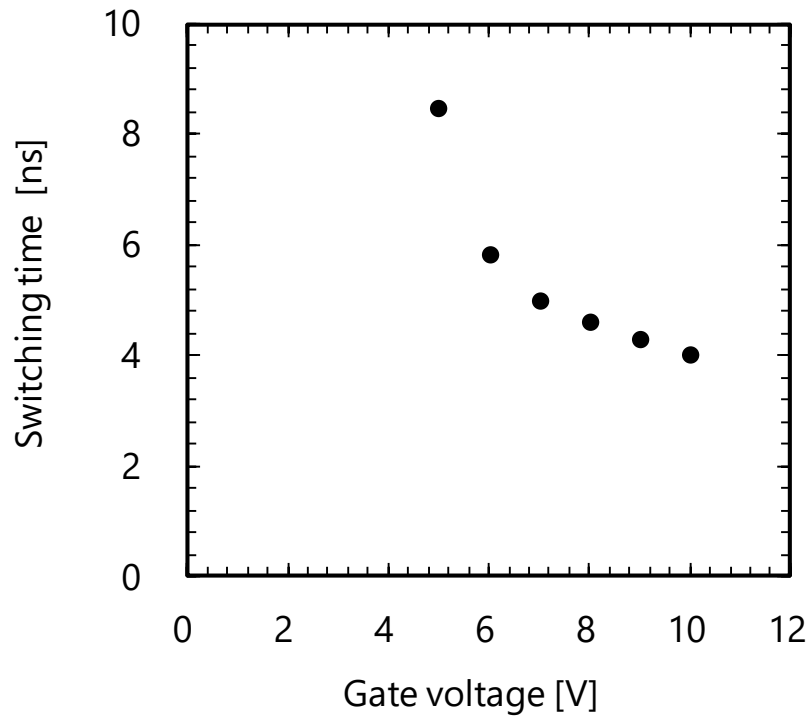


(a)

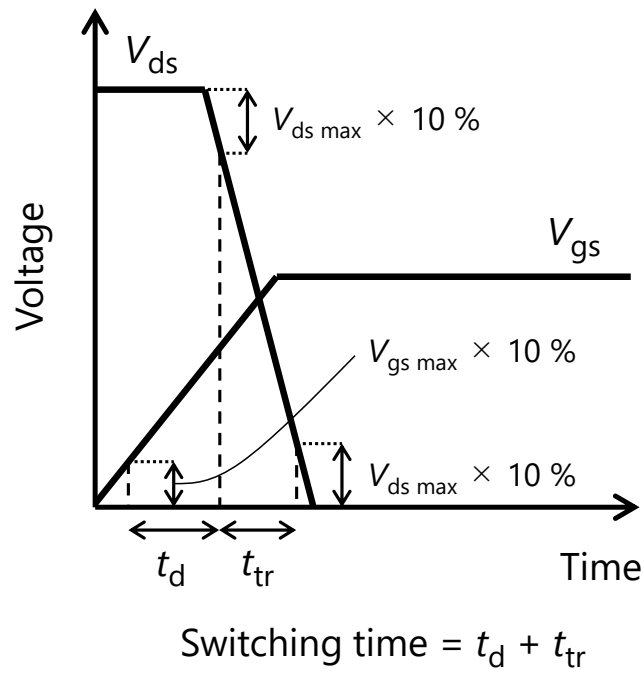


(b)

Figure 5.10: Switching waveform of (a) turn-on and (b) turn-off transitions exhibited by the fabricated AlON/AlGaIn/GaN MIS-HFET.



(a)



(b)

Figure 5.11: (a) Switching time for the turn-on operations as a function of gate voltage and (b) a schematic waveform for a turn-on operation showing definitions of delay time (t_d) and transition time (t_{tr}).

in 55 % reduction of delay time for the increasing V_{gs} from 5 to 10 V, which agrees well with the experimentally observed reduction of switching time. Since two gate capacitances (C_{gs} and C_{gd}) are charged by a gate current caused by applying gate voltage to the external gate resistance in this period, the delay time is reduced by increasing the gate voltage. Meanwhile, the transition time for turn-on is given by

$$t_{tr} = \frac{C_{ds} + (1 + g_m R_g) C_{gd}}{I_D + g_m V_{th}} V_{DD}, \quad (5.2)$$

where I_D and V_{DD} are on-state drain current and off-state drain voltage, g_m is transconductance of the devices, and C_{ds} is source-drain parasitic capacitance [7]. Equation (5.2) indicates that the transition time is independent of gate voltage. Thus, the fast switching operations exhibited by the fabricated AlON/AlGaIn/GaN MIS-HFETs resulted from the shortening of delay time by applying high gate voltage. To achieve further faster switching operations, reduction of parasitic capacitance (C_{gs} , C_{gd} , and C_{ds}) is required.

5.5 Summary

In this chapter, the normally-off AlGaIn/GaN MIS-HFETs on Si substrates with high-current and high-voltage capability exhibiting the stable gate characteristics were demonstrated. The AlON gate insulators with the nitrogen composition of 10 % and formation of the recessed gate structures using the regrowth process contribute suppression of the threshold voltage shift and the hysteresis in the transfer characteristics. The O_2 annealing performed at 750 °C after deposition of AlON shifts V_{th} in the positive direction, resulting in the normally-off operations. The fabricated devices are almost free from the threshold voltage shift and the hysteresis in the transfer characteristics, ensuring applicable gate voltage as high as 10 V. The experimentally confirmed switching speed for off-state drain voltage of 400 V and on-state drain current of 10 A with an inductive load is very fast with dV/dt of 151 V/ns and 154 V/ns for turn-on and turn-off transitions, respectively. In particular, the switching time for the turn-on transitions are reduced from 8 to 4 ns by increasing gate voltage from 5 to 10 V, taking advantage of the stable gate characteristics of the fabricated MIS-HFETs. The achieved switching performance indicates that the presented AlON/AlGaIn/GaN MIS-HFETs are very promising for practical power switching applications.

References

- [1] C. Mizue, Y. Hori, M. Miczek, and T. Hashizume, *Jpn. J. Appl. Phys.* **50**, 021001 (2011).
- [2] S. Huang, S. Yang, J. Roberts, and K. J. Chen, *Jpn. J. Appl. Phys.*, **50**, 110202 (2011).
- [3] M. A. Khan, Q. Chen, C. J. Sun, and J. W. Yang, *Appl. Phys. Lett.* **68**, 514 (1996).
- [4] A. Endoh, Y. Yamashita, K. Ikeda, M. Higashiwaki, K. Hikosaka, T. Matsui, S. Hiyamizu, and T. Mimura, *Jpn. J. Appl. Phys.* **43**, 2255 (2004).
- [5] T. Hashizume, S. Anantathanasarn, N. Negoro, E. Sano, H. Hasegawa, K. Kumakura, and T. Makimoto, *Jpn. J. Appl. Phys.* **43**, L777 (2004).
- [6] H. Okita, M. Hikita, A. Nishio, T. Sato, K. Matsunaga, H. Matsuo, M. Tsuda, M. Mannoh, S. Kaneko, M. Kuroda, M. Yanagihara, A. Ikoshi, T. Morita, K. Tanaka, and Y. Uemoto, *IEEE Trans. Electron Devices* **64**, 1026 (2017).
- [7] D. A. Grant and J. Goward, *Power MOSFETs: Theory and Applications* (Wiley, New York, 1989).

Chapter 6

Conclusions

6.1 Conclusions

In this thesis, effects of the interfacial charges, such as the polarization charges at the heterojunctions and the charges at MIS interfaces of III-nitride semiconductors, on the device performance were investigated to improve the performance of the AlGaIn/GaN HFETs.

In Chapter 2, effects of the polarization charges at the heterojunctions of the III-nitride semiconductors on the device performance were described. The polarization charge is one of the most important features in the III-nitride semiconductors, which provides a high density of 2DEG with a high mobility, at the heterointerface, for example, at the AlGaIn/GaN interface. Meanwhile, the polarization charge at the GaN/AlGaIn interface caused the depletion at the interface, which led to the increase of the parasitic resistance in AlGaIn/GaN HFETs with a GaN capping layer. The InAlGaIn quaternary capping layer was proposed to suppress the depletion at the interface between the capping layer and the barrier layer. The composition of the InAlGaIn layer was designed to be lattice matched with GaN serving enough thickness and to have equal or larger polarization than that of the underlying AlGaIn barrier layer. The InAlGaIn layer with designed compositions was grown on AlGaIn/GaN heterostructures by MOCVD. The resultant parasitic resistance at the InAlGaIn/AlGaIn heterojunction was $7.8 \times 10^{-6} \Omega\text{cm}^2$, which was one-fifth as low as in the GaN/AlGaIn interface.

In Chapter 3, improvement of the output power together with a higher gain in the AlGaIn/GaN HFETs on the Si substrates for high frequency applications was demonstrated. So far, high frequency performance of AlGaIn/GaN HFETs on Si substrates are not yet satisfactory in terms of an output power and a gain as compared with HFETs on SiC substrates, partly because of poorer crystal quality of GaN on Si, limiting operating voltage. To improve the device performance of the HFETs on Si, effects of the field plates on the device performance was investigated. In general, field plates are introduced to enhance breakdown voltage by relieving electric field crowding and their ends are designed to be placed in the middle of gate-drain spacing. This study revealed that such a long field plate caused significant variation of the output impedance by the change of the drain voltage and thus limited the maximum output power. The small-signal equivalent circuit analysis revealed that

the variation of the drain-source capacitance caused that of the output impedance, which could be suppressed by shortening the field plate. The fabricated AlGaIn/GaN HFET on the Si substrate with a field-plate length of $0.6\ \mu\text{m}$ and gate width of $48\ \mu\text{m}$ exhibited an output power of $203\ \text{W}$ together with a linear gain of $16.9\ \text{dB}$ at $2.5\ \text{GHz}$, which was high enough to be practically applied to power amplifiers for the cellular base stations.

In Chapter 4, effects of the device fabrication processes, such as dry-etching, deposition of insulators, and post-deposition annealing, on the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ MIS interface properties were investigated by analyzing the C - V characteristics of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MIS heterojunction diodes. Al_2O_3 was deposited by Atomic Layer Deposition (ALD), using TMA as a precursor and O_2 -plasma and H_2O as oxidant. The interface state density was increased from the middle of 10^{12} to $10^{13}\ \text{cm}^{-2}\ \text{eV}^{-1}$ by the dry-etching process especially around $0.4\ \text{eV}$ below the conduction band edge, which would be attributed to a trap related to N-vacancy on the underlying AlGaIn surface. The N-vacancy is generated possibly with dissociation of nitrogen from the AlGaIn surface while producing volatile N-based products during dry-etching process. The threshold voltage shift in the positive direction was caused by post-deposition annealing in the oxygen atmosphere at 750°C due to reduction of the positive charges at the MIS interface or/and in the Al_2O_3 films. The reduction of the positive charges was more significant in Al_2O_3 deposited using H_2O oxidant ($6 \times 10^{12}\ \text{cm}^{-2}$) than O_2 -plasma (almost no change was observed), implying that the positive charges are related to oxygen deficiency in Al_2O_3 . AlON was deposited by incorporating nitrogen into Al_2O_3 by NH_3 -plasma during the ALD process. AlON with nitrogen composition of $10\ \%$ exhibited the suppressed threshold voltage shift of $0.2\ \text{V}$ at the anode bias of $6\ \text{V}$ as compared with Al_2O_3 ($0.6\ \text{V}$). The captured electron density of AlON was estimated $3 \times 10^{11}\ \text{cm}^{-2}$, which is less than half of Al_2O_3 , indicating of reduction in electron trap density in accordance with the reported result of first-principle calculation. These results are instructive for designing threshold voltage of AlGaIn/GaN MIS-HFET and achieve the stable gate characteristics.

In Chapter 5, AlGaIn/GaN MIS-HFETs on Si substrates with stable gate characteristics were demonstrated. The fabrication process was based on the results described in Chapter 4, including the formation of the recessed gate structures with the barrier layer regrowth, the adoption of the AlON (nitrogen incorporated Al_2O_3) as the gate insulator, and the post-deposition annealing in the oxygen atmosphere. The structure of the fabricated MIS-HFET was AlON $30\ \text{nm}/\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}\ 50\ \text{nm}/\text{GaN}/\text{Si}$, and thickness of AlGaIn layer under gate electrode was $5\ \text{nm}$. N composition in an AlON insulator was $10\ \%$. The fabricated AlGaIn/GaN MIS-HFETs exhibited normally-off operation with threshold voltage of $1.4\ \text{V}$, to which the gate voltage as high as $10\ \text{V}$ was applicable without causing the hysteresis and the threshold voltage shift. The switching measurement at the off-state drain voltage of $400\ \text{V}$ and the on-state drain current of $10\ \text{A}$ with an inductive load was carried out using the fabricated AlON/AlGaIn/GaN MIS-HFET with gate width of $100\ \mu\text{m}$ which exhibited a maximum drain current of $25\ \text{A}$ and off-state breakdown voltage of $730\ \text{V}$. The experimentally confirmed

switching speed was 151 and 154 V/ns for turn-on and turn-off transitions. The turn-on time was reduced from 8 to 4 ns by increasing the gate voltage from 5 to 10 V, taking advantage of the stable gate characteristics. The achieved switching speed and turn-on time were fast enough for MHz-class switching applications.

6.2 For Future Work

This thesis has shed light on the effects of the interface charges on the device characteristics, particularly the parasitic resistance at the heterojunctions and threshold voltage of the AlGaIn/GaN MIS-HFETs to improve the device performance. In this section, the author would like to refer to the remaining issues together with the suggestions for the future work to achieve further improvement in the performance of AlGaIn/GaN HFETs.

In terms of the high frequency applications, the following items should help to achieve further improvement of the device performance.

- Although reduction of the parasitic resistance by balancing the polarization charges at the heterojunctions between the capping layer and barrier layer was achieved, the improvement in the high frequency performance of AlGaIn/GaN HFETs has not been demonstrated. Introduction of the InAlGaIn capping layer to the AlGaIn/GaN HFETs with the source field plates will exhibit higher gain with higher efficiency owing to the reduced source resistance.
- Applying the lattice-matched InAlGaIn alloy to a barrier layer instead of a capping layer of the GaN-based HFETs can produce higher density of sheet carriers than the conventional AlGaIn barrier layer without causing deteriorating cracks in the barrier layers, which should increase the drain current and thereby the output power.

As for the power switching applications, the following items should be clarified to put the GaN-based MIS devices into practical use.

- The MIS-HFETs proposed in this thesis exhibit a practical switching speed for MHz-class switching applications, whereas their on-state resistance is relatively high and the channel resistance has turned out to be dominant. Since the low on-state resistance is required to attain the highly efficient operations, effects of the MIS interface properties on the channel resistance should be investigated to reduce it.
- Although the presented MIS-HFETs exhibit the stable threshold voltage even after the continuous switching operations, the long-term reliability has not been characterized. There have been no reports on effects of the GaN MIS interface charges on such reliability, which should be investigated to implement the GaN-based MIS devices.

Finally, the author believes further progress of the material and device technology should realize the comfort and convenient society together with sustainability.

List of Publications

A. Full Length Papers and Letters

- (1) S. Nakazawa, T. Ueda, K. Inoue, T. Tanaka, H. Ishikawa, and T. Egawa,
“Recessed-gate AlGa_N/Ga_N HFETs with lattice-matched InAlGa_N quaternary alloy capping layers”,
IEEE Trans. Electron Devices **52**, 2124 (2005).
- (2) T. Takizawa, S. Nakazawa, and T. Ueda,
“Crystalline SiN_x Ultrathin Films Grown on AlGa_N/Ga_N Using *In Situ* Metalorganic Chemical Vapor Deposition”,
J. Electron. Mater. **37**, 628 (2008).
- (3) T. Ueda, T. Murata, S. Nakazawa, H. Ishida, Y. Uemoto, K. Inoue, T. Tanaka,
and D. Ueda,
“Polarization Engineering in Ga_N Power Transistors”,
phys. stat. sol. (b) **247**, 1735 (2010).
- (4) S. Nakazawa, N. Tsurumi, M. Nishijima, Y. Anda, M. Ishida, T. Ueda, and T. Tanaka,
“200 W Output Power at S-Band in AlGa_N/Ga_N Heterojunction Field Effect Transistors with Field Plates on Si Substrates”,
Jpn. J. Appl. Phys. **51**, 081801 (2012).
- (5) S. Nakazawa, N. Shiozaki, N. Negoro, N. Tsurumi, Y. Anda, M. Ishida, and T. Ueda,
“Improved hysteresis in a normally-off AlGa_N/Ga_N MOS heterojunction field-effect transistor with a recessed gate structure formed by selective regrowth”,
Jpn. J. Appl. Phys. **56**, 091003 (2017).
- (6) S. Nakazawa, H.-A. Shih, N. Tsurumi, Y. Anda, T. Hatsuda, T. Ueda, T. Kimoto,
and T. Hashizume,
“Effects of post-deposition annealing in O₂ on threshold voltage of Al₂O₃/AlGa_N/Ga_N MOS heterojunction field-effect transistors”,
Jpn. J. Appl. Phys. **58**, 030902 (2019).

- (7) S. Nakazawa, H.-A. Shih, N. Tsurumi, Y. Anda, T. Hatsuda, T. Ueda, M. Nozaki, T. Yamada, T. Hosoi, T. Shimura, H. Watanabe, T. Hashizume, and T. Kimoto, “AlON/AlGa_N/Ga_N MIS-HFETs for High-Frequency Switching Applications”, in preparation.

B. Proceedings of International Conferences

- (1) D. Ueda, T. Murata, M. Hikita, S. Nakazawa, M. Kuroda, H. Ishida, M. Yanagihara, K. Inoue, T. Ueda, Y. Uemoto, T. Tanaka, and T. Egawa, “AlGa_N/Ga_N devices for future power switching systems”, 2005 IEEE Int. Electron Devices Meeting (IEDM) Tech. Dig., 2005, p. 377. (*IEEE Int. Electron Devices Meeting 2005*, Washington, DC, USA, 2005.)
- (2) D. Ueda, M. Hikita, S. Nakazawa, K. Nakazawa, H. Ishida, M. Yanagihara, K. Inoue, T. Ueda, Y. Uemoto, T. Tanaka, and T. Egawa, “Present and Future Prospects of Ga_N-based Power Electronics”, Proc. of 9th Int. Conf. on Solid-State and Integrated-Circuit Tech. (ICSICT), 2008, p. 1078. (9th Int. Conf. on Solid-State and Integral-Circuit Technology, Beijing, China, 2008.)
- (3) S. Nakazawa, H.-A. Shih, N. Tsurumi, Y. Anda, T. Hatsuda, T. Ueda, M. Nozaki, T. Yamada, T. Hosoi, T. Shimura, H. Watanabe, and T. Hashizume, “Fast Switching Performance by 20 A / 730 V AlGa_N/Ga_N MIS-HFET Using AlON Gate Insulator”, 2017 IEEE Int. Electron Devices Meeting (IEDM) Tech. Dig., 2017, p. 605. (*IEEE Int. Electron Devices Meeting 2017*, San Francisco, CA, USA, 2017.)

C. Presentation at International Conferences

- (1) S. Nakazawa, T. Ueda, T. Tanaka, H. Ishikawa, and T. Egawa, “Low Ohmic Contact Resistance on Lattice-matched InAlGa_N Quaternary Alloy Capping Layers over AlGa_N/Ga_N Heterojunction Field Effect Transistors”, Abstr. of 6th Topical Workshop on Heterostructure Microelectronics, 2005, p. 98. (6th Topical Workshop on Heterostructure Microelectronics, Awaji Island, Hyogo, Japan, 2005).
- (2) T. Morita, S. Nakazawa, T. Ueda, and T. Tanaka, “Current Collapse-Free Vertical Submicron Channel Ga_N-based Transistors with InAlGa_N Quaternary Alloy Contact Layer”, Proc. 64th IEEE Device Research Conference, 2006, p. 97. (64th IEEE Device Research Conference, Pennsylvania, PA, USA, 2006).

- (3) M. Kuroda, T. Murata, S. Nakazawa, T. Takizawa, M. Nishijima, M. Yanagihara, T. Ueda, and T. Tanaka,
 “High $f_{\max}$ with high breakdown voltage in AlGaIn/GaN MIS-HFETs using *in-situ* SiN as gate insulators”,
 2008 IEEE Compound Semiconductor IC Symposium, 2008, O3.
 (2008 IEEE Compound Semiconductor IC Symposium, Monterey, CA, USA, 2008).
- (4) S. Nakazawa, N. Tsurumi, M. Nishijima, Y. Anda, M. Ishida, T. Ueda, and T. Tanaka,
 “High-Power and High-Gain S-band AlGaIn/GaN HFETs with Source Field Plates on Si Substrate”,
 Ext. Abst. of Int. Conf. on Solid State Devices and Materials 2011, 564 (2011).
 (Int. Conf. on Solid State Devices and Materials 2011, Nagoya, Aichi, Japan, 2011).
- (5) S. Nakazawa, N. Shiozaki, N. Negoro, N. Tsurumi, Y. Anda, M. Ishida, and T. Ueda,
 “AlGaIn/GaN MOS-HFETs Exhibiting Improved Hysteresis in Transfer Characteristics with Recessed Gate Structures Formed by Selective Regrowth”,
 Ext. Abstr. of Int. Conf. on Solid State Devices and Materials 2015, 1044 (2015).
 (Int. Conf. on Solid State Devices and Materials 2015, Sapporo, Hokkaido, Japan, 2015).
- (6) S. Nakazawa, H.-A. Shih, N. Tsurumi, Y. Anda, T. Hatsuda, T. Ueda, M. Nozaki, T. Yamada, T. Hosoi, T. Shimura, H. Watanabe, and T. Hashizume,
 “GaN-based Metal-Insulator-Semiconductor Transistors on Si for Power Switching Applications”,
 19th Int. Conf. on Metalorganic Vapor Phase Epitaxy Tech. Dig., 5B-1.1 (2018).
 (19th Int. Conf. on Metalorganic Vapor Phase Epitaxy, Nara, Japan, 2018).

D. Related Publications

- (1) T. Kimoto, S. Nakazawa, K. Hashimoto, and H. Matsunami,
 “Reduction of doping and trap concentrations in 4H-SiC epitaxial layers grown by chemical vapor deposition”,
 Appl. Phys. Lett. **79**, 2761 (2001).
- (2) S. Nakazawa, T. Kimoto, K. Hashimoto, and H. Matsunami,
 “High-purity 4H-SiC epitaxial growth by hot-wall chemical vapor deposition”,
 J. Cryst. Growth **237-239**, 1213 (2002).
- (3) T. Kimoto, T. Hirao, S. Nakazawa, H. Shiomi, and H. Matsunami,
 “Homoepitaxial growth of 4H-SiC (0001) and nitrogen doping by chemical vapor deposition”,
 J. Cryst. Growth **249**, 208 (2003).

- (4) E. Ogawa, T. Hashizume, S. Nakazawa, T. Ueda, and T. Tanaka,
“Chemical and Potential Bending Characteristics of $\text{SiN}_x/\text{AlGaN}$ Interface Prepared by *In situ* Metal-Organic Chemical Vapor Deposition”,
Jpn. J. Appl. Phys. **46**, L590 (2007).
- (5) R. Asahara, M. Nozaki, T. Yamada, J. Ito, S. Nakazawa, M. Ishida, T. Ueda, A. Yoshigoe, T. Hosoi, T. Shimura, and H. Watanabe,
“Effect of nitrogen incorporation into Al-based gate insulators in AlON/AlGaN/GaN metal-oxide-semiconductor structures”,
Appl. Phys. Express **9**, 101002 (2016).
- (6) K. Watanabe, M. Nozaki, T. Yamada, S. Nakazawa, Y. Anda, M. Ishida, T. Ueda, A. Yoshigoe, T. Hosoi, T. Shimura, and H. Watanabe,
“Design and control of interface reaction between Al-based dielectrics and AlGaN layer in AlGaN/GaN metal-oxide-semiconductor structures”,
Appl. Phys. Lett. **111**, 042102 (2017).
- (7) T. Yamada, J. Ito, R. Asahara, K. Watanabe, M. Nozaki, S. Nakazawa, Y. Anda, M. Ishida, T. Ueda, A. Yoshigoe, T. Hosoi, T. Shimura, and H. Watanabe,
“Comprehensive study on initial thermal oxidation of GaN(0001) surface and subsequent oxide growth in dry oxygen ambient”,
J. Appl. Phys. **121**, 035303 (2017).
- (8) M. Nozaki, K. Watanabe, T. Yamada, H.-A. Shih, S. Nakazawa, Y. Anda, T. Ueda, A. Yoshigoe, T. Hosoi, T. Shimura, and H. Watanabe,
“Implementation of atomic layer deposition-based AlON gate dielectrics in AlGaN/GaN MOS structure and its physical and electrical properties”,
Jpn. J. Appl. Phys. **57**, 06KA02 (2018).
- (9) T. Yamada, K. Watanabe, M. Nozaki, H.-A. Shih, S. Nakazawa, Y. Anda, T. Ueda, A. Yoshigoe, T. Hosoi, T. Shimura, and H. Watanabe,
“Physical and electrical characterizations of AlGaN/GaN MOS gate stacks with AlGaN surface oxidation treatment”,
Jpn. J. Appl. Phys. **57**, 06KA07 (2018).