

**Study on Channel Mobility
and Threshold Voltage
Towards SiC CMOS Devices**

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Abstract

Progress of human society over the last few decades has been driven by advancements in semiconductor technology, and applications of semiconductors are expected to expand continuously. Silicon (Si) is the most commonly used semiconductor material and is found in a wide range of applications. However, Si technology faces some limitations in specific areas, particularly in power electronics and high-temperature electronics, due to the material properties of Si. Wide bandgap (WBG) semiconductor materials have gained significant attention as a solution to these issues, and recently, part of Si power devices have been replaced by WBG semiconductor devices.

Silicon carbide (SiC) is regarded as one of the most promising WBG materials in power electronics and high-temperature electronics due to its superior material properties: A high critical electric field (2.5 MV/cm) and a wide bandgap (3.26 eV). The more mature material growth and device processing technology for SiC, compared to other WBG materials, enabled mass production and commercialization of SiC devices. SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) are currently used for next-generation low-loss and high-voltage power devices. In addition to power applications, SiC MOSFETs are expected to be used for complementary MOS (CMOS) integrated circuits (ICs) operating at high temperatures beyond 300°C; however, they have not been implemented in this area. One of the obstacles to the implementation is the lack of studies on SiC p-channel MOSFETs, which are the core components of CMOS devices that consist of n- and p-channel MOSFETs.

So far, SiC n-channel MOSFETs have been extensively investigated for power devices. In other words, the fundamental knowledge of SiC p-channel MOSFETs is lacking, causing difficulties in designing CMOS devices. Although SiC/silicon dioxide (SiO₂) interface states, channel mobility, and threshold voltage mainly dominate the characteristics of SiC MOSFETs, they are not understood well for SiC p-channel MOSFETs. Thus, the author focused on the interface states near the valence band edge because they affect the hole conduction in SiC p-channel MOSFETs. In addition, since channel mobility and threshold voltage are generally changed by the increasing body doping accompanied by CMOS scaling down, the body doping dependencies of channel mobility and threshold voltage were investigated. The threshold voltage in SiC n-channel MOSFETs was also investigated because of extremely poor understanding.

In Chapter 2, the interface state density (D_{it}) near the valence band edge (E_V) was investigated by using the high-low, $C-\psi_S$, and conductance methods. The $C-\psi_S$ and conductance methods determined an accurate energy distribution of D_{it} near E_V , revealing a density of $\sim 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$, which is comparable to that near the conduction band edge (E_C). The conductance method suggested that the predominant interface states are donor-type states and also revealed that the potential fluctuation of E_V is significantly smaller than that near E_C .

In Chapter 3, SiC (0001) p-channel MOSFETs with various body doping concentrations were fabricated, and the p-channel mobility was discussed by comparing it to the n-channel mobility. When channel mobility was normalized by bulk mobility (electron: $1020 \text{ cm}^2/\text{Vs}$, hole: $95 \text{ cm}^2/\text{Vs}$), it was found that the p-channel mobility is two times higher than the n-channel mobility. This phenomenon originates from the weak quantum confinement effects caused by the effective mass of holes larger than that of electrons. The mobility drop in the high effective normal field (E_{eff}) region is weak for the p-channel MOSFETs but strong for the n-channel MOSFETs. An analysis using the body biasing technique implied that the different mobility behavior against E_{eff} is caused by the difference in dominant carrier scattering due to E_{eff} between the n- and p-channel MOSFETs.

In Chapter 4, p-channel MOSFETs on SiC (11 $\bar{2}$ 0) and (1 $\bar{1}$ 00) were fabricated. The (1 $\bar{1}$ 00) p-channel MOSFETs exhibited a mobility of $28\text{--}31 \text{ cm}^2/\text{Vs}$, which is the highest value ever reported for SiC p-channel MOSFETs. The dependence of p-channel mobility on the crystal face is caused by the crystal face dependence of D_{it} near E_V . Moreover, the nonpolar-face p-channel mobility depends on the channel direction: The mobility perpendicular to the c -axis is higher than that parallel to the c -axis. This anisotropic mobility originates from the anisotropy of the effective mass of holes in the inversion layer, revealed by a numerical calculation considering quantum confinement effects and three different hole bands in SiC.

In Chapter 5, the body doping dependence of threshold voltage was investigated in both n- and p-channel MOSFETs on SiC (0001). The difference between the experimental and theoretical threshold voltages depends on the body doping concentration (N_{Body}), which is significant for the heavily-doped MOSFETs. The threshold voltage discrepancy is caused by doping-dependent fixed charges, which have not been reported in Si MOSFETs. As N_{Body} increases, negative fixed charges increase in the n-body (p-channel) devices, and positive fixed charges increase in the p-body (n-channel) devices. Various control experiments revealed that the density of fixed charges depends not only on the body doping concentration but also on the final annealing temperature. Based on this result, the author proposed a model of the fixed charge generation related to the Fermi level at a final annealing temperature.

In Chapter 6, the author summarizes this thesis and provides outlooks for future work.

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Chapter 1

Introduction

1.1 Background

It is no exaggeration to say that modern human society is heavily dependent on semiconductor technology. Semiconductors are essential components used in a wide range of applications, including electronic devices like smartphones and personal computers, electric transportation such as trains and automobiles, power transmission from power plants to homes, and various household appliances. Semiconductor applications will continue to expand more and more, and power consumption will rapidly increase alongside this expansion. Today's semiconductor devices are predominantly fabricated using silicon (Si) because of mature fabrication technology and cost-efficiency resulting from the availability of large-scale 300 mm Si wafers. Thus, Si semiconductor devices have led the expansion of semiconductor applications to this point. However, in specific applications, Si technology is facing inherent limitations as long as Si remains the material choice.

When we utilize electricity, power conversion from common power sources, such as electric outlets, is required in most cases because different electric devices operate at specific voltage forms. This power conversion is performed using power semiconductor devices (power devices), which is called power electronics [1]. Currently, nearly 10% of electric power is wasted as Joule heat, resulting in a usable range of only 85–95% of the total electric power. These energy losses primarily arise from the conduction and switching losses of Si power devices. Therefore, it is crucial to further reduce power losses by improving the performance of power devices. However, the energy losses of Si power devices is approaching the theoretical limitations determined by the material properties of Si.

In addition to power electronics, semiconductor applications are beginning to extend into high-temperature environments that humans themselves cannot access directly. This field is called high-temperature electronics [2]. These electronics include space exploration to Venus, drilling of underground resources (oil, gas, and geothermal energy), and combustion furnaces. Typical temperatures in these applications exceed 300°C, where Si devices cannot operate inherently due to the material properties of Si. High-temperature electron-

ics also include automobiles when sensors and controls are placed directly on engines where temperatures can be as high as about 200°C. Silicon-on-insulator (SOI) technology has potential in this application [3] because SOI devices have demonstrated high-temperature operation of up to 300°C in the research phase [4]. However, in practical applications, thermal isolation and external cooling systems would be required to prevent thermal runaway caused by both environmental heat and self-heating of Si devices. These thermal measures increase the volume of the entire system and lead to additional energy losses because of the cooling systems [5].

In order to overcome these problems originating from the material properties of Si, wide-bandgap (WBG) semiconductor materials have attracted much attention because of their higher critical breakdown electric field and larger bandgap compared to Si. Among the typical WBG semiconductors, such as silicon carbide (SiC), gallium nitride (GaN), gallium oxide (Ga_2O_3), and diamond, SiC is regarded as one of the most promising materials for both power electronics and high-temperature electronics.

1.2 Silicon Carbide (SiC) and Its Applications

1.2.1 Properties of SiC

SiC is a IV-IV compound semiconductor consisting of 50% Si and 50% carbon (C). The strong chemical bonding between Si and C atoms brings this material high physical robustness, chemical stability, and high thermal conductivity [6]. SiC has various crystal structures (polytypes), such as 3C-SiC, 4H-SiC, and 6H-SiC, due to different stacking sequences of Si-C pairs along the c -axis, keeping its chemical composition. Among more than 200 polytypes of SiC, 4H-SiC is particularly suitable for electronic applications because of its superior material properties [7]. Table 1.1 summarizes the major material properties of Si, 3C-SiC, 4H-SiC, and 6H-SiC [7–19]. 4H-SiC has a high critical electric field (2.5–2.8 MV/cm), wide bandgap (3.26 eV), and high carrier mobility (electron: 1200 cm²/Vs, hole: 95 cm²/Vs). These material properties of 4H-SiC enable low-loss power devices and high-temperature operational devices beyond Si-device limitation. The reasons are described in Sections 1.2.2 and 1.2.3. Hereafter, the term “SiC” refers to 4H-SiC for simplicity.

As previously stated, several kinds of WBG semiconductors exist. The reasons why SiC is regarded as one of the most promising materials will be explained in this paragraph. Among various semiconductor devices with different structures and operating mechanisms, such as bipolar junction transistors (BJTs), metal-semiconductor field-effect transistors (MESFETs), and junction field-effect transistors (JFETs), metal-oxide-semiconductor field-effect transistors (MOSFETs) have become core devices in current semiconductor applications. This is because MOSFETs are unipolar and voltage-driven devices capable of high-speed and low-loss operation. Moreover, complementary MOS (CMOS) devices consisting of two different types (n-channel and p-channel) of MOSFETs have enabled integrated circuits

Table 1.1: Major material properties of Si and common SiC polytypes [7–19].

Properties	Si	3C-SiC	4H-SiC	6H-SiC
Bandgap [eV]	1.12	2.36	3.26	3.02
Electron mobility [cm^2/Vs]	1450	1000	1200 ($\parallel c$) 1020 ($\perp c$)	100 ($\parallel c$) 450 ($\perp c$)
Hole mobility [cm^2/Vs]	450	100	85 ($\parallel c$) 95 ($\perp c$)	100
Electron saturated drift velocity [cm/s]	1×10^7	$\sim 2 \times 10^7$	2.2×10^7	1.9×10^7
Hole saturated drift velocity [cm/s]	8×10^6	$\sim 1.3 \times 10^7$	$\sim 1.3 \times 10^7$	$\sim 1.3 \times 10^7$
Critical electric field [MV/cm]	0.4	1.4	2.5 ($\parallel c$) 2.2 ($\perp c$)	2.8 ($\parallel c$) 1.7 ($\perp c$)
Thermal conductivity [W/cmK]	1.5	3.3–4.9 (not sensitive to SiC polytypes)		
Relative permittivity	11.9	9.72	10.32 ($\parallel c$) 9.76 ($\perp c$)	10.03 ($\parallel c$) 9.66 ($\perp c$)

(ICs) with low power consumption, high-speed operation, and high functionality because of their easy scaling down. Therefore, it is preferred that semiconductor materials satisfy the requirements for MOSFET fabrication. One of the most important requirements is a sufficiently large band offset (> 2 eV) between the oxide and the semiconductor for both conduction and valence band sides (ΔE_C and ΔE_V). Insufficient band offsets lead to a large gate leakage current, raising concerns for a long-term reliability of gate oxides. Figure 1.1 shows the energy-band diagram of silicon dioxide (SiO_2) and typical WBG materials based on several investigations of band offsets and electron affinity for WBG materials [20–23]. The energy-band diagram of Si is also shown in Fig. 1.1 for comparison. Because of the larger bandgap of WBG materials, the ΔE_C and ΔE_V for WBG materials are lower than those for Si. Since SiC and GaN have a larger band offset for both conduction and valence band sides than other WBG materials, they are promising for MOSFET applications. In particular, SiC has a well-balanced band offset of $\Delta E_C \sim 2.8$ eV and $\Delta E_V \sim 2.8$ eV.

In addition to the requirement of band offsets, selective doping by ion implantation is another important requirement for semiconductor materials from the viewpoint of device fabrication. Taking CMOS devices as an example, typical n- and p-type doping densities are 10^{19} – 10^{20} cm^{-3} for contact regions (source, drain, and body), 10^{17} – 10^{18} cm^{-3} for body regions, 10^{16} – 10^{17} cm^{-3} for channel regions, and 10^{16} – 10^{18} cm^{-3} for wells. Since these regions are closely adjacent to one another, selective and wide-range doping control is essential for device fabrication, achieved by ion implantation. Mature ion implantation technology in SiC can control doping densities from 10^{15} cm^{-3} to a very high density of 10^{20} cm^{-3} for both n- and p-type [24–27]. On the other hand, in the case of GaN, wide-range p-type doping by ion implantation is difficult at the present stage. In addition, SiC technology is more mature compared to other WBG materials: Single-crystalline 6–8-inch wafers for mass production and high-quality epitaxial growth with doping density from 10^{14} to 10^{19} cm^{-3} for both n- and p-type [28–32].

1.2.2 Applications in Power Electronics

Ideal switching components show no voltage drop in the ON-state and no current in the OFF-state. However, since realistic power devices have a semiconductor layer blocking high voltages (drift layer), a voltage drop must occur in the ON-state due to the drift layer and other resistances. Moreover, in the OFF-state, a sharp increase in current occurs due to impact ionization when applying a voltage higher than the breakdown voltage. In general, the drift layer resistance is the dominant resistance of power devices, strongly affecting static power dissipation.

Although a reduction in the drift layer resistance is required to suppress energy loss, there is a trade-off relationship between the drift layer resistance per unit area (R_{drift}) and

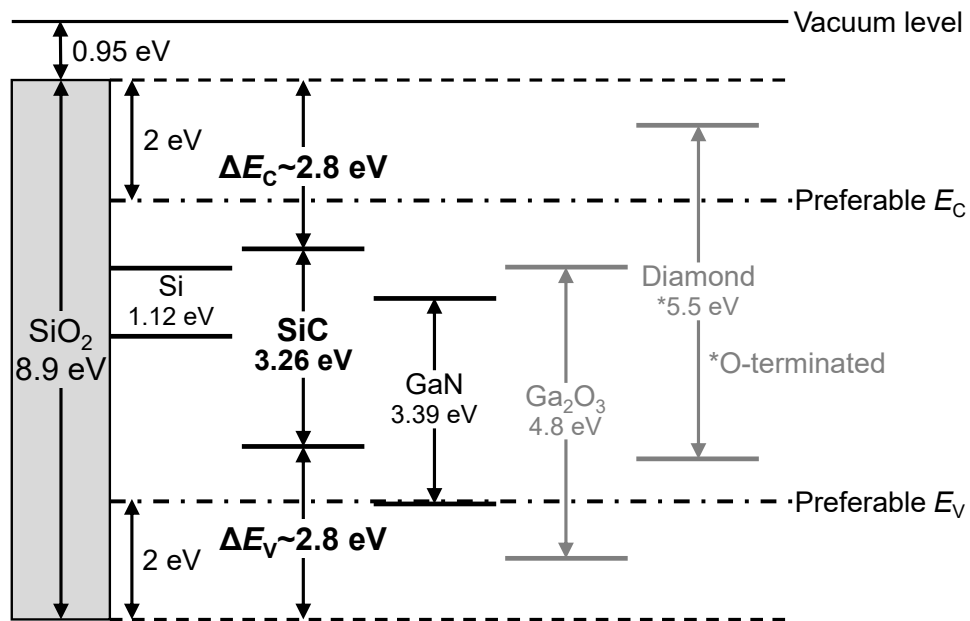


Figure 1.1: Energy-band diagram of SiO₂, Si, and typical WBG semiconductors.

the blocking voltage (V_B) for unipolar devices with a non-punch-through structure [7, 33]:

$$R_{\text{drift}} = \frac{4V_B^2}{\eta\varepsilon_s\mu_{\text{bulk}}E_{\text{cr}}^3} \quad (1.1)$$

where η is the ionization ratio the dopants in a drift layer, ε_s is the permittivity of the semiconductor, μ_{bulk} is the carrier mobility in bulk, and E_{cr} is the critical electric field. This equation indicates that the material properties of semiconductors uniquely determine the drift layer resistance, and the theoretical limitation of the on-resistance per unit area (specific on-resistance) is also determined. Figure 1.2 illustrates the trade-off relationship between the theoretical limitation of specific on-resistance and the blocking voltage for Si and SiC power devices. Since the critical electric field of SiC is about 10 times higher than that of Si, the on-resistance can be reduced by 2–3 orders of magnitude by utilizing SiC power devices, thereby significantly reducing conduction loss.

Another important advantage of SiC power devices is the reduction in switching loss, owing to their high-voltage endurance and unipolar characteristics. In Si technology, insulated-gate bipolar transistors (IGBTs) and gate-turn-off (GTO) thyristors, which are bipolar devices that can reduce the on-resistance by conductivity modulation, have been commercialized in medium- (~ 600 V) to high-voltage (several kV) applications because the on-resistance becomes unacceptably high when unipolar devices like MOSFETs are used. However, bipolar transistors inherently cause large switching losses because minority carriers generate an undesirable tail current after the switching from ON- to OFF-states. On the other hand, SiC enables unipolar devices even for the same voltage-class applications, and the large switching loss of Si IGBTs can be effectively reduced by utilizing SiC power devices.

Figure 1.3 shows the major territories of Si and SiC power devices regarding the rated blocking voltage. For low-voltage (several hundred V) applications, Si unipolar devices are the major choice due to their cost-efficiency and the low drift resistances. For medium- to high-voltage applications, both Si bipolar and SiC unipolar devices are practical choices. At the present stage, since the chip cost of SiC devices is higher than that of Si devices, which Si or SiC devices to use depends on the users and each application. As for ultra-high-voltage (>10 kV) applications, SiC bipolar devices are promising because the on-resistance of SiC unipolar devices becomes very large due to the thick drift layer of the unipolar devices.

1.2.3 Applications in High-Temperature Electronics

Since pn junctions play essential roles in device operation and electrical isolation between semiconductor devices, the leakage currents of the pn junctions should be small. The leakage current in the pn junctions is proportional to the intrinsic carrier density (n_i), which strongly

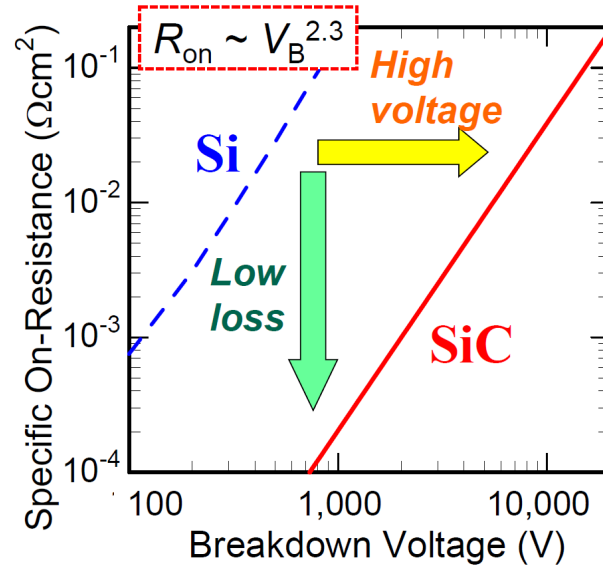


Figure 1.2: Trade-off relationship between the theoretical limitation of specific on-resistance and the blocking voltage for Si and SiC power devices.

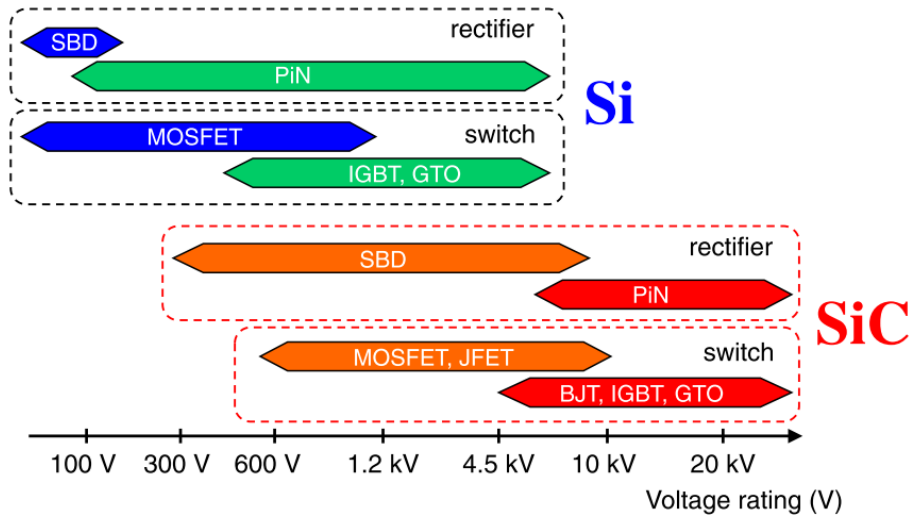


Figure 1.3: Major territories of Si and SiC power devices regarding the rated blocking voltage [34].

depends on the bandgap and temperature:

$$n_i = \sqrt{N_C N_V} \exp\left(-\frac{E_g}{2kT}\right) \quad (1.2)$$

where N_C and N_V are the effective densities of states in the conduction and valence bands, E_g is the bandgap, k is the Boltzmann constant, and T is the absolute temperature. Figure 1.4 depicts the temperature dependence of the intrinsic carrier density for Si and SiC, which is calculated using Eq. (1.2). The wider bandgap of SiC brings an extremely low intrinsic carrier density to SiC at a given temperature. The intrinsic carrier density of SiC at 500°C is still lower than that of Si at the typical maximum operating temperature of 200°C. This is the reason why SiC is suitable for high-temperature electronics.

Figure 1.5 shows the various semiconductor applications from RT to high temperatures up to 600°C [3, 5, 7]. Although SiC devices can operate from the RT to high temperatures of over 300°C, Si devices are mainstream in standard applications with lower temperatures than 150–200°C. Since Si devices cannot operate at high temperatures of over 300°C, SiC devices are promising in such high-temperature applications. As for applications from 200 to 300°C, whether to use Si or SiC devices would depend on applications. For example, the applications using Si devices would be sensing and monitoring where power dealing is low, and those using SiC devices would be highly functional ICs both with sensors and with power management units located close to or on engines.

1.3 SiC Metal-Oxide-semiconductor Field-Effect Transistors (MOSFETs)

1.3.1 Power MOSFETs and Complementary MOS Devices

SiC MOSFETs have been commercially available for next-generation low-loss and high-voltage power devices. Since high carrier mobility is preferable to achieve a low on-resistance, power MOSFETs are n-channel MOSFETs of which carriers are electrons. In fact, commercialized SiC MOSFETs are n-channel devices because the electron mobility (1200 cm²/Vs [17]) is higher than the hole mobility (95 cm²/Vs [15]) in bulk SiC. The on-resistance of power MOSFETs consists not only of the drift layer resistance but also of other resistances such as the channel, substrate, JFET, source/drain contact, and source region resistances. Among these resistances, channel resistance especially causes an undesirable increase in specific on-resistance of 600 V- and 1.2 kV-class SiC power MOSFETs. The ratio of the channel resistance to the specific on-resistance is about 66% for 600 V-class devices and about 48% for 1.2 kV-class devices [35]. On the other hand, the influence of channel resistance is small in Si MOSFETs. The difference in the influence of channel resistance between Si and SiC MOSFETs is caused by the large difference in channel mobility. For

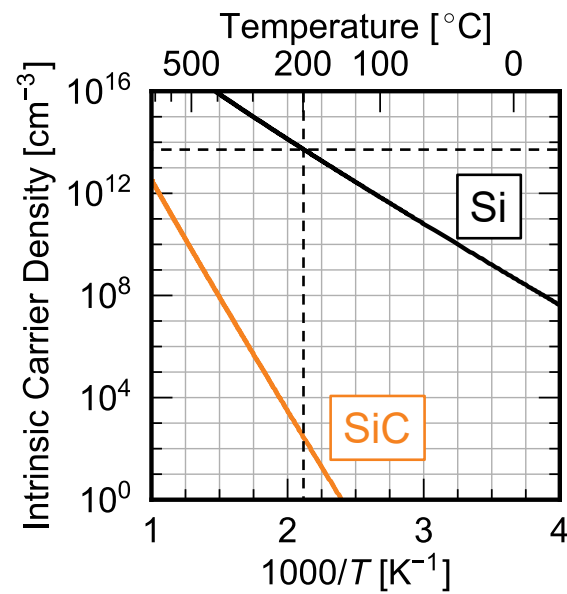


Figure 1.4: Temperature dependence of the intrinsic carrier density for Si and SiC.

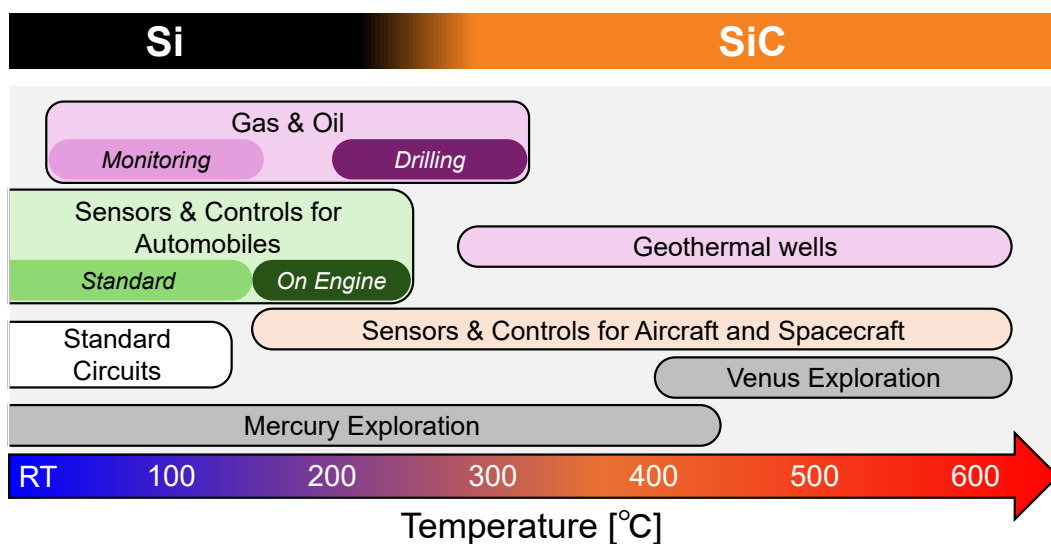


Figure 1.5: Expected major territories of Si and SiC devices for high-temperature applications.

MOSFETs with a lightly-doped body, Si MOSFETs show a channel mobility of over 500 cm^2/Vs [36, 37], which is more than 30% of the bulk mobility. In contrast, SiC MOSFETs show a channel mobility of about 30–50 cm^2/Vs [38, 39], less than 5% of the bulk mobility. The channel mobility lower than bulk mobility in Si MOSFETs is a general behavior because drift mobility in the inversion layer must be lower than bulk mobility due to interface scatterings [40–43]. However, in SiC MOSFETs, the channel mobility as low as 5% of the bulk mobility originates not only from interface scatterings but also from carrier trapping at the interface. Here, channel mobility is effective mobility, assuming all carriers induced by gate voltages contribute to conduction in MOSFETs. In SiC/SiO₂ structures, a large number of interface states exist, of which the density is 2–3 orders of magnitude higher than that in Si/SiO₂ structures [44–47]. The interface states capture most of the carriers induced by gate voltages, causing a decrease in the density of carriers that contribute to conduction. In addition to carrier trapping effects, the carriers trapped at the interface behave as strong Coulombic scattering centers [48, 49], decreasing the drift mobility of carriers. Thus, the channel mobility in SiC MOSFETs is significantly lower than the bulk mobility.

So far, extensive studies have been conducted to reveal the origin of the interface states and to reduce the interface states. Although C-related defects are one of the most promising origins [50–54], the origin of interface states still needs to be clarified. As for reducing the interface states, the reduction methods have been proposed by several groups: Impurity incorporation near the interface such as nitrogen (N) [55, 56], phosphorus (P) [57, 58], boron (B) [59], and hydrogen (H) [60], ultra-high-temperature oxidation [61], and metal-enhanced oxidation (MEO) using sodium (Na) and barium (Ba) [62–64]. Although a high mobility of over 70 cm^2/Vs was achieved by several methods (P incorporation, B incorporation, Na MEO, and Ba MEO), these methods have dielectric reliability problems, such as threshold voltage shifts. As a result, annealing in nitric oxide (NO), one of the N incorporation methods, became the standard annealing process after gate oxide (SiO₂) formation because NO annealing can improve channel mobility to some extent, keeping the oxide reliability. Recently, Tachiki *et al.* have proposed the oxidation-minimizing process [65] based on the idea that oxidation of SiC causes C-related defects near the interface. The oxidation-minimizing process consists of three steps: (i) Si-rich H₂ treatment, (ii) SiO₂ formation without SiC oxidation, and (iii) nitridation such as NO and N₂ annealing [65, 66]. This new technique dramatically improves the channel mobility (25–40 cm^2/Vs) for (0001) MOSFETs with a heavily-doped body ($> 10^{17} \text{ cm}^{-3}$), which is important for practical planar-gate power MOSFETs [67], where typical mobility obtained by the standard process is only 10 cm^2/Vs . Furthermore, this technique also improves the channel mobility (over 100 cm^2/Vs) for the nonpolar-face MOSFETs, which is important for trench-gate power MOSFETs. Energetic research is being conducted to improve the performance of SiC power MOSFETs, and further progress is expected.

Another application of SiC MOSFETs is CMOS ICs operating at high temperatures. Several groups have reported the high-temperature demonstration of SiC CMOS. In 1997,

6H-SiC CMOS successfully operated from RT to 300°C [68]. 4H-SiC CMOS was then demonstrated [69–73], and 532°C operation was confirmed [73]. In addition to CMOS IC application itself, monolithic power ICs with high power density, which is difficult to achieve with Si technology, can be realized by fabricating SiC power MOSFETs and SiC CMOS on the same chip [74, 75]. Since SiC power MOSFETs are currently driven by Si-CMOS-based circuits, cooling systems only for Si devices are usually required. SiC monolithic power ICs can reduce cooling systems for Si devices, contributing to miniaturization, weight reduction, and low loss of the entire power conversion system. Moreover, wiring distance between power MOSFETs and driving circuits can be shortened, suppressing voltage overshoots caused by parasitic inductance during fast switching. Although SiC CMOS devices have also been attractive for advanced SiC-MOSFET-based circuits, such as high-temperature CMOS ICs and monolithic power ICs, SiC CMOS devices have yet to be practical at the present stage.

1.3.2 Key Issues for Advanced SiC-MOSFET-Based Circuits

One of the obstacles to implementing SiC CMOS devices is the lack of knowledge of SiC p-channel MOSFETs. Since CMOS devices consist of both n-channel and p-channel MOSFETs, a fundamental understanding of both devices is important. However, extensive studies have focused on SiC n-channel MOSFETs to implement SiC power MOSFETs and improve their performance. As a result, fundamental knowledge of SiC p-channel MOSFETs is severely lacking, causing difficulties in designing and fabricating SiC CMOS ICs.

As mentioned in the previous section, SiC/SiO₂ interface states capture a large number of electrons in the inversion layer, degrading the n-channel mobility. Similarly, the interface states capture holes in the inversion layer, degrading the p-channel mobility. Here, at SiC/SiO₂ interface, the interface state density exponentially increases as the energy level of the interface states approaches the conduction band edges [7]. These interface states have a significant impact on channel mobility. Taking n-channel MOSFETs as an example, as shown in Fig. 1.6, the electrons in the inversion layer are trapped at the interface states near the conduction band edge because the on-state surface Fermi level is located near the conduction band edge. As for the p-channel MOSFETs, the on-state surface Fermi level is located near the valence band edge, and the holes are trapped at the interface states near the valence band edge. Thus, the interface state density near the band edges should be obtained to discuss the influence on channel mobility and predict the characteristics of both n- and p-channel MOSFETs. Several reports have quantified the energy distribution of interface state density near the conduction band edge [47, 55, 56, 76, 77]. In contrast, since studies near the valence band edge are limited [76, 78], an accurate energy distribution of the interface state density has not been obtained.

Physics-based device model of n- and p-channel MOSFETs is essential when designing CMOS ICs. The most important device parameters are channel mobility and threshold voltage. Here, shortening channel length is a standard technique to improve the performance

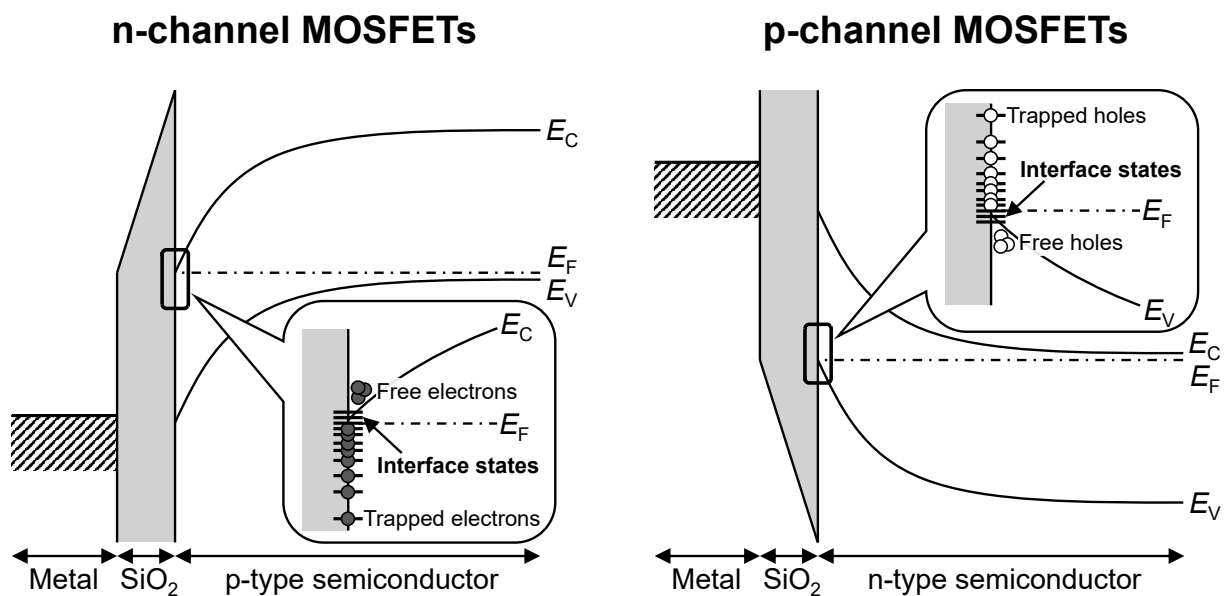


Figure 1.6: Band diagrams of the on-state n- and p-channel MOSFETs. The interface states near the conduction band edge capture electrons in the inversion layer for n-channel MOSFETs, whereas those near the valence band edge capture holes in the inversion layer for p-channel MOSFETs.

of CMOS devices [9] in terms of high speed, low loss, and high integrity. On the other hand, shortening channel length causes short-channel effects, which negatively affect the performance of MOSFETs, such as unintentional lowering of threshold voltage, increase in leakage currents from the source to the drain regions, and degradation of the subthreshold characteristics. The short-channel effects can be effectively suppressed by a higher impurity concentration in the body region of MOSFETs. However, an increase in body doping concentration changes both channel mobility and threshold voltage. Moreover, the body doping is changed not only to suppress the short-channel effects but also to precisely control the threshold voltage. Therefore, the body doping dependence of channel mobility and threshold voltage is one of the most important knowledge for designing CMOS ICs. The n-channel mobility has been investigated with a wide range of body doping concentrations (10^{15} – 10^{18} cm $^{-3}$) [49, 77, 79–83], whereas the p-channel mobility has not been investigated to date. Regarding the threshold voltage, only one report exists for n-channel MOSFETs [79]. In other words, the body doping dependence of threshold voltage is sorely lacking for both n- and p-channel SiC MOSFETs.

1.4 Objectives and Outline of This Thesis

Based on the background, the author investigates (i) the energy distribution of SiC/SiO $_2$ interface state density near the valence band edge, (ii) the body doping dependence of mobility in SiC p-channel MOSFETs, and (iii) the body doping dependence of threshold voltage in both n- and p-channel SiC MOSFETs. These investigations, mainly focusing on SiC p-channel MOSFETs, are essential for implementing SiC-MOSFET-based circuits that possess high power density and can operate at high temperatures, which cannot be inherently achieved by Si technology.

In Chapter 2, the energy distribution of interface state density near the valence band edge is extracted by three different methods, the high-low, C – ψ_s , and conductance methods. The interface state density is accurately determined by the conductance method. The time constant of carrier emissions from the interface states, capture cross section of the interface states, and surface potential fluctuation obtained for the valence band side are compared to those for the conduction band side.

In Chapter 3, SiC (0001) p-channel MOSFETs with various body doping concentrations are fabricated. The p-channel mobility is compared to the n-channel mobility, considering the difference between electron and hole mobility in bulk SiC. In addition, the body doping dependence of n- and p-channel mobility is investigated using the body biasing technique, and the carrier scattering in the inversion layer is discussed, considering the scattering unique to SiC MOSFETs.

In Chapter 4, SiC p-channel MOSFETs on nonpolar faces such as (11 $\bar{2}$ 0) and (1 $\bar{1}$ 00), are fabricated with various body doping concentrations, and the highest mobility ever reported

for SiC p-channel MOSFETs is demonstrated. The body doping and crystal face dependence of nonpolar-face p-channel mobility are discussed using the body biasing technique and subthreshold characteristics, respectively. Furthermore, the origin of anisotropic p-channel mobility is revealed by a numerical calculation of the hole effective mass in the inversion layer considering quantum-confinement effects and three different hole bands in SiC. Based on the highest p-channel mobility obtained in this chapter, a promising structure of SiC FinFETs is proposed to achieve high-performance SiC CMOS ICs.

In Chapter 5, the dependence of threshold voltage on body doping is investigated for both n- and p-channel SiC (0001) MOSFETs. The difference between the experimental and theoretical threshold voltages is discussed considering the fixed charges near SiC/SiO₂ interface. Based on the results of various control experiments, a model of fixed charge generation is proposed, and the validity of the proposed model is also discussed.

Finally, the conclusions and future prospects are provided in Chapter 6.

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Chapter 2

Interface State Density near The Conduction and Valence Band Edges at SiC/SiO₂ Interface

2.1 Introduction

The interface states, whose energy levels are near the conduction and valence band edges, strongly affect the characteristics of n- and p-channel MOSFETs, respectively. So far, the interface state density (D_{it}) near the conduction band edge (E_C) at the nitrided SiC/SiO₂ interface has been investigated in detail by various methods such as the high-low, $C-\psi_S$, and conductance methods [1–5]. In addition, MOS-Hall effect measurements combined with Split capacitance–voltage ($C-V$) measurements have been developed to obtain D_{it} vicinity of the band edge [6]. As a result, it was found that the D_{it} exponentially increases as the surface Fermi level approaches E_C , with the density reaching as high as 10^{12} – 10^{13} cm⁻²eV⁻¹. On the other hand, the D_{it} near the valence band edge (E_V) at the nitrided interface was investigated only by the high-low and $C-\psi_S$ methods [3, 7]. The high-low and $C-\psi_S$ methods usually underestimate or overestimate D_{it} due to their principles, thereby unreliable D_{it} near E_V at the present stage. The conductance method is one of the most powerful techniques for obtaining D_{it} because of its high sensitivity in D_{it} detection ($\sim 10^9$ cm⁻²eV⁻¹) and reliable data in the probe frequency range. Furthermore, the conductance method provides not only D_{it} but also important information about the interface states.

2.2 Device Fabrication

The starting materials for n- and p-type MOS capacitors were an n-type epilayer grown on a SiC (0001) n-type substrate and a p-type epilayer grown on a p-type substrate, respectively. The donor concentration of the n-type epilayer was 5×10^{15} cm⁻³, while the acceptor concentration of the p-type epilayer was 1×10^{15} cm⁻³. The gate oxide was formed by dry

oxidation at 1300°C for 20 min, followed by NO annealing [1, 2, 8] at 1250°C for 70 min, resulting in an oxide thickness of about 30 nm. After forming the backside electrode, both samples were annealed at 1000°C for 2 min to obtain good ohmic contacts. The gate metal was formed by Al evaporation.

2.3 Characterization Method of Interface State Density

2.3.1 High-Low Method

The high-low method uses two different C - V curves measured with a “high” frequency and a “low” frequency. The most important assumption in this method is that all interface states can respond to the low frequency but cannot respond to the high frequency. Under this assumption, the interface state density can be extracted by [9, 10]:

$$D_{it} = \frac{(C_D + C_{it})_{LF} - (C_D + C_{it})_{HF}}{q^2 S} \quad (2.1)$$

where C_D is the depletion layer capacitance in a semiconductor, C_{it} is the interface-state capacitance, q is the elementary charge, and S is the gate electrode area. $(C_D + C_{it})_{LF}$ and $(C_D + C_{it})_{HF}$ are the semiconductor capacitances measured with low and high frequencies, respectively. If the assumption is satisfied, the high-frequency semiconductor capacitance corresponds to the depletion layer capacitance, $(C_D + C_{it})_{HF} = C_D$. In this situation, the high-low method provides an accurate D_{it} . In general, a frequency of 100 kHz or 1 MHz is adopted for a high frequency in this method. However, the high-low method typically underestimates D_{it} in SiC/SiO₂ structures because very fast states, which can respond to frequencies over 1 MHz, exist after interface nitridation [4]. Additionally, the interface states have a large dispersion of time constants near the conduction band edge [11–14].

2.3.2 C - ψ_S Method

The C - ψ_S method is a similar technique to the high-low method, but this method uses a calculated depletion capacitance instead of a high-frequency capacitance. Thus, the limitation of D_{it} characterization in the high-low method can be overcome by using the C - ψ_S method. In other words, the C - ψ_S method can characterize all interface states, including the very fast states underestimated by the conventional high-low method. In this method, the interface state density can be extracted by [4]:

$$D_{it} = \frac{(C_D + C_{it})_{LF} - C_{D,calc}}{q^2 S} \quad (2.2)$$

where $C_{D,\text{calc}}$ is the calculated depletion capacitance. The $C_{D,\text{calc}}$ for p-type MOS capacitors is given by the following equation [4, 10]:

$$C_{D,\text{calc}}(\psi_S) = \frac{SqN_A \left| \exp\left(-\frac{q\psi_S}{kT}\right) - 1 \right|}{\sqrt{\frac{2kTN_A}{\varepsilon_S} \left\{ \exp\left(-\frac{q\psi_S}{kT}\right) + \frac{q\psi_S}{kT} - 1 \right\}}} \quad (2.3)$$

Here, N_A is the acceptor concentration, ψ_S is the surface potential, k is the Boltzmann constant, T is the absolute temperature, and ε_S is the permittivity of the semiconductor. The surface potential can be obtained by the Berglund's technique [15]:

$$\psi_S(V_G) = \int (1 - C_{QS}/C_{ox}) dV_G + A \quad (2.4)$$

where C_{QS} is the quasi-static capacitance, C_{ox} is the gate oxide capacitance, V_G is the gate voltage, and A is the integration constant. It has been reported that small errors in the integration constant of A cause large errors in D_{it} extracted by the C - ψ_S method [16].

2.3.3 Conductance Method

The high-low and C - ψ_S methods characterize D_{it} using the interface-state capacitance, whereas the conductance method characterizes it using the interface-state conductance. The interface-state conductance has a peak value when plotted against frequency. The interface state density is extracted by fitting Eq. 2.5 [9, 10] to the experimental conductance-frequency curves.

$$\frac{G_{\text{pit}}}{\omega} = q^2 S D_{it} \int_{-\infty}^{+\infty} \frac{\ln(1 + (\omega\tau_{it} \exp(\eta))^2)}{2\omega\tau_{it} \exp(\eta)} \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{\eta^2}{2\sigma^2}\right) d\eta \quad (2.5)$$

where G_{pit} is the interface-state conductance, ω is the angular frequency, τ_{it} is the time constant of carrier emissions from the interface states, and σ is the standard deviation of the surface potential fluctuations. Here, D_{it} , τ_{it} , and σ are the fitting parameters. Since the conductance method needs numerous fittings to obtain the energy distribution of D_{it} (one fitting provides a single data point of the energy distribution), it takes significantly more time when using this method compared to the C - V -based methods. On the other hand, the conductance method can extract not only the interface state density but also the time constant and surface potential fluctuations. The capture cross section of the interface states (σ_{it}) can be obtained by using the time constant:

$$\sigma_{it} = \frac{1}{v_{th} N_V \tau_{it}} \exp\left(\frac{E_T - E_V}{kT}\right) \quad (2.6)$$

where v_{th} is the thermal velocity of holes, N_V is the effective density of states in the valence band, and E_T is the energy levels of interface states.

When electrons/holes are captured at the traps inside the oxide via tunneling, the conductance is modeled using the following equation [17]:

$$\frac{G_{\text{pit}}}{\omega} = \frac{q^2 S N_{\text{ot}}}{2K_0} \int_{-\infty}^{+\infty} \left[\frac{\pi}{2} + \frac{\ln(1 + (\omega\tau_{\text{ot}})^2)}{2\omega\tau_{\text{ot}}} - \arctan(\omega\tau_{\text{ot}}) \right] \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{\eta^2}{2\sigma^2}\right) d\eta \quad (2.7)$$

where N_{ot} is the density of oxide traps and τ_{ot} is the time constant of carrier emissions from the oxide traps. K_0 is the tunneling probability from the semiconductor to the oxide, given by [18]:

$$K_0 = \frac{\sqrt{2m^*(E - E_V^{\text{ox}})}}{\hbar} \quad (2.8)$$

Here, m^* is the effective mass of holes ($0.58m_0$ [19], m_0 : free electron mass), $E - E_V^{\text{ox}}$ is the barrier height for hole tunneling (2.9 eV), and $\hbar$ is the reduced Planck constant.

2.4 Experimental Results

2.4.1 Capacitance–Voltage Characteristics

Figure 2.1 shows the C – V characteristics of the fabricated n- and p-type SiC (0001) MOS capacitors. The experimental C – V curves for both samples show a negative shift from the ideal curves. The flatband voltage shift was -2.3 V for the p-type sample and -1.2 V for the n-type sample. Compared to the n-type samples, a larger frequency dispersion was observed for the p-type sample in the gate-voltage range from -5 to -4 V. This frequency dispersion corresponds to a relatively high interface state density near the valence band edge, where the energy levels are deeper than approximately 0.4 eV.

2.4.2 Conductance–Frequency Characteristics

Figure 2.2 depicts the conductance–frequency (G_{pit}/ω – f) characteristics at $E_T - E_V = 0.25$ eV of the fabricated p-type MOS capacitor. The G_{pit}/ω – f curve shows a peak conductance at 300 kHz and an asymptotic behavior approaching 6.7×10^{-5} F/m² in the low-frequency range (<10 kHz). This experimental G_{pit}/ω – f curve (symbols) was fitted well with the calculated curve (black line), assuming one type of interface state (red line) and one type of oxide trap (blue line). Similarly, the G_{pit}/ω – f curves at different energy levels were fitted well, as shown in Fig. 2.3. When the energy levels approach E_V (from 0.47 to 0.25 eV), the peak conductance in the high-frequency range (100 k–1 MHz) increases from 1.9×10^{-4} to 1.4×10^{-3} F/m², and the peak-conductance frequency decreases from 1 M to 300 kHz. In the low-frequency range (<10 kHz), the asymptotic conductance increases from 2.4×10^{-5} to 6.7×10^{-5} F/m². The conductance increase in the high- and low-frequency ranges corresponds to the increase in interface state density and oxide traps, respectively. The decrease in the peak-conductance frequency corresponds to a slower response of the interface states.

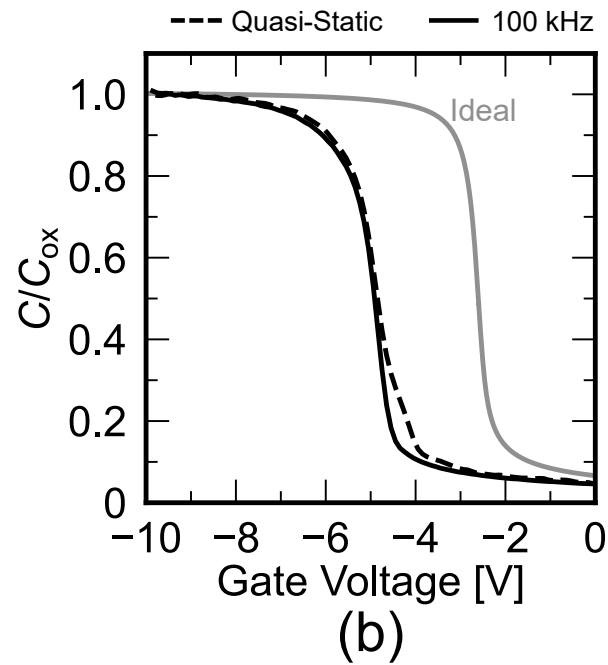
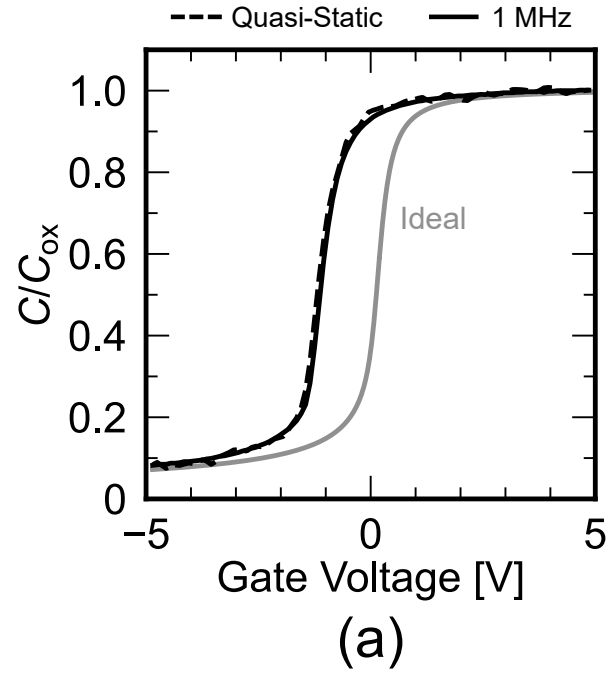


Figure 2.1: Capacitance–voltage characteristics for the (a) n-type and (b) p-type MOS capacitors fabricated on (0001).

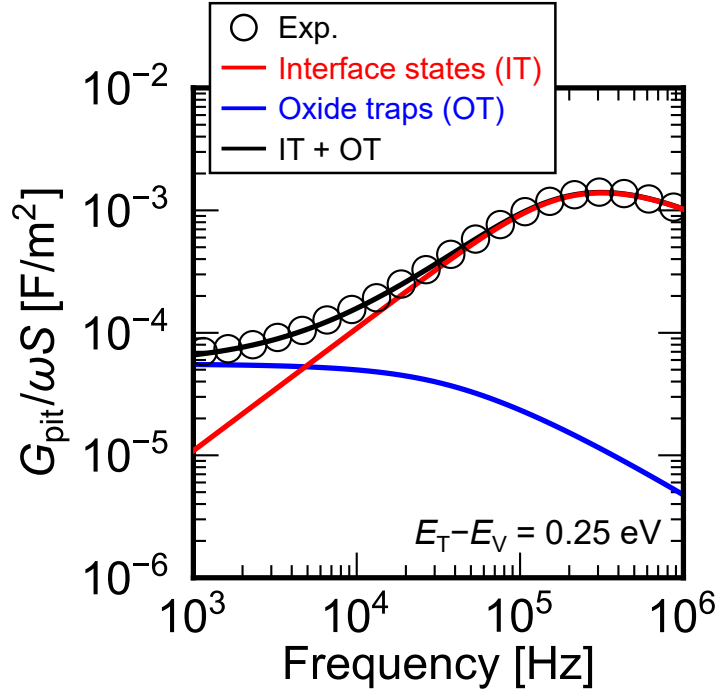


Figure 2.2: Experimental interface-state conductance (G_{pit}) and fitting results of G_{pit} considering oxide traps and interface states as a function of the frequency. The vertical axis is G_{pit} normalized by angular frequency (ω) and the gate area (S). The energy level of interface states (E_{T}) is $E_{\text{T}} - E_{\text{V}} = 0.25$ eV, where E_{V} is the valence band edge.

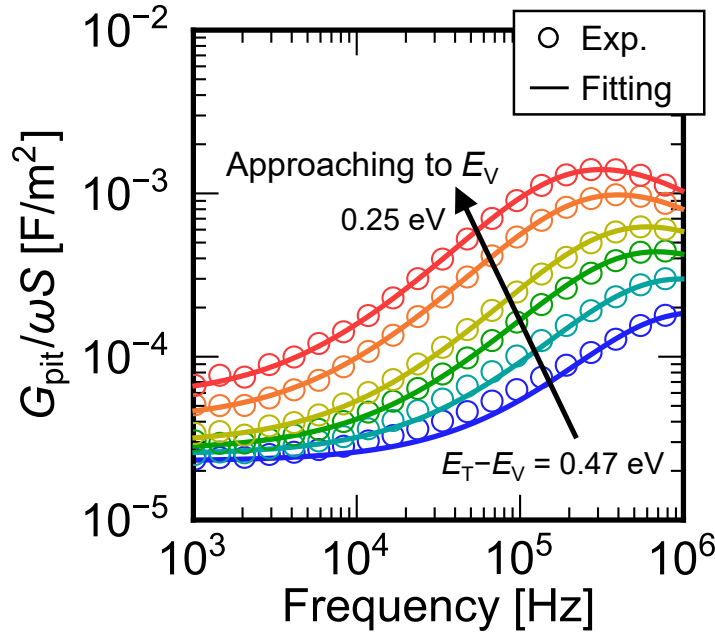


Figure 2.3: Interface-state conductance–frequency ($G_{\text{pit}}-f$) characteristics at different energy levels for the p-type MOS capacitors fabricated on (0001). The vertical axis is G_{pit} normalized by angular frequency (ω) and the gate area (S).

2.4.3 Interface State Density

Figure 2.4 illustrates the D_{it} near E_V extracted by the high-low, $C-\psi_S$, and conductance methods. The interface state density near the conduction band edge is also shown in Fig. 2.4 for comparison. The D_{it} near E_V extracted by the high-low method is lower than that extracted by the other two methods, indicating that the high-low method underestimates the D_{it} near E_V . On the other hand, the D_{it} near E_V extracted by the conductance methods is comparable to that extracted by the $C-\psi_S$ method, indicating that an accurate energy distribution of interface state density could be obtained for the nitrided SiC/SiO₂ interface. It was found that the D_{it} near E_V exponentially increases from 2.8×10^{11} to 3.9×10^{12} cm⁻²eV⁻¹ when the energy levels approach E_V (from 0.5 to 0.2 eV). The slight difference between the D_{it} extracted by the conductance method and the D_{it} extracted by the $C-\psi_S$ method originates from the oxide traps corresponding to the asymptotic conductance in Fig. 2.3, which is discussed in the next paragraph. Comparing D_{it} around 0.2 eV from the band edges (E_C or E_V), the D_{it} near E_V is almost the same as that near E_C . In addition to the results close to the band edges, the D_{it} near E_V is higher than that near E_C in the energy level region deeper than 0.2 eV from the band edge.

The density of oxide traps extracted by the conductance method is shown in Fig. 2.5. The obtained N_{ot} increases from 1.2×10^{18} to 2.9×10^{18} cm⁻³ when the energy levels approach E_V (from 0.47 to 0.25 eV). Assuming the tunneling distance from the SiC/SiO₂ interface to the oxide layer is only a few nanometers, the areal density of oxide traps can be estimated to be approximately 10^{11} cm⁻², corresponding to the slight difference between the D_{it} values extracted by the conductance method and those extracted by the $C-\psi_S$ method.

2.4.4 Time Constants, Capture Cross Sections, and Surface Potential Fluctuations

Figure 2.6 illustrates the time constants of hole emissions from the interface states and the capture cross sections of the interface states as a function of the energy level from the valence band edge. When the energy levels approach E_V (from 0.47 to 0.25 eV), the time constants increase from 2.4×10^{-7} to 1.0×10^{-6} s, and the capture cross section decreases from 8.9×10^{-13} to 4.5×10^{-17} cm⁻². It is noteworthy that the time constants usually decrease approaching the band edge because the capture and emission processes typically occur more readily for the interface states closer to the band edge. However, when the capture cross sections strongly depend on the energy levels from the band edge, the observed decrease in the capture cross section is plausible. Figure 2.7 depicts the capture cross sections near the conduction and valence band edges. Here, “OX” and “NI” denote the interface states near the conduction band edge generated by oxidation and nitridation processes, respectively [4]. The exponential relationship between the capture cross sections and the energy levels significantly differs between the interface states near the conduction

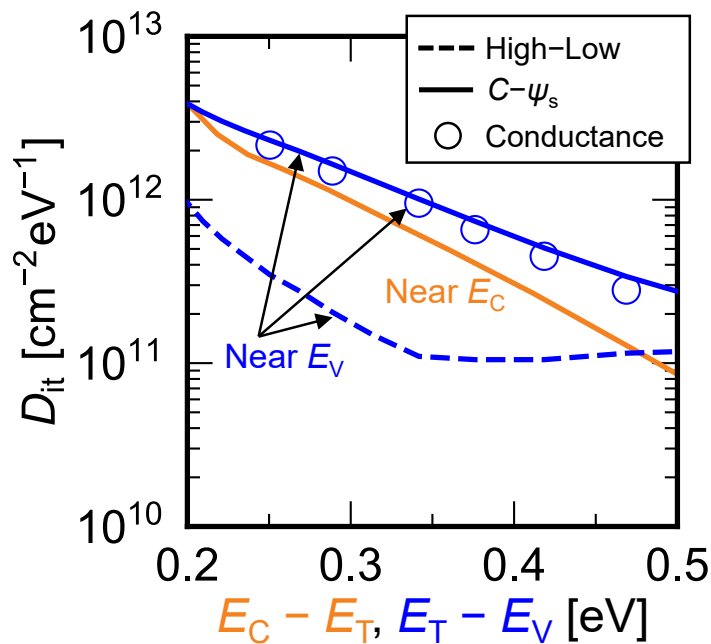


Figure 2.4: Energy distribution of the density of interface states (D_{it}) near the valence band edge (E_V) extracted by the high(100 kHz)-low, $C-\psi_s$, and conductance method. The energy distribution of D_{it} near the conduction band edge (E_C) is also shown for comparison.

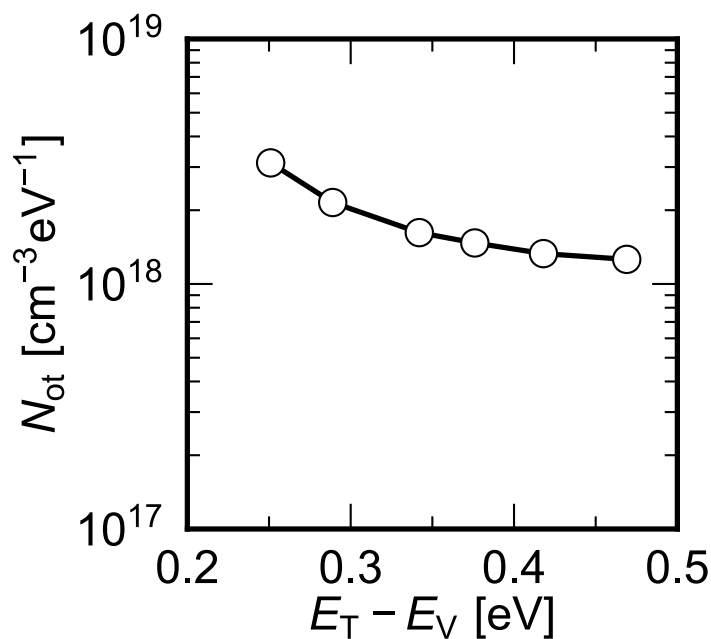


Figure 2.5: Energy distribution of the density of oxide traps (N_{ot}) near the valence band edge (E_V) extracted by the conductance method.

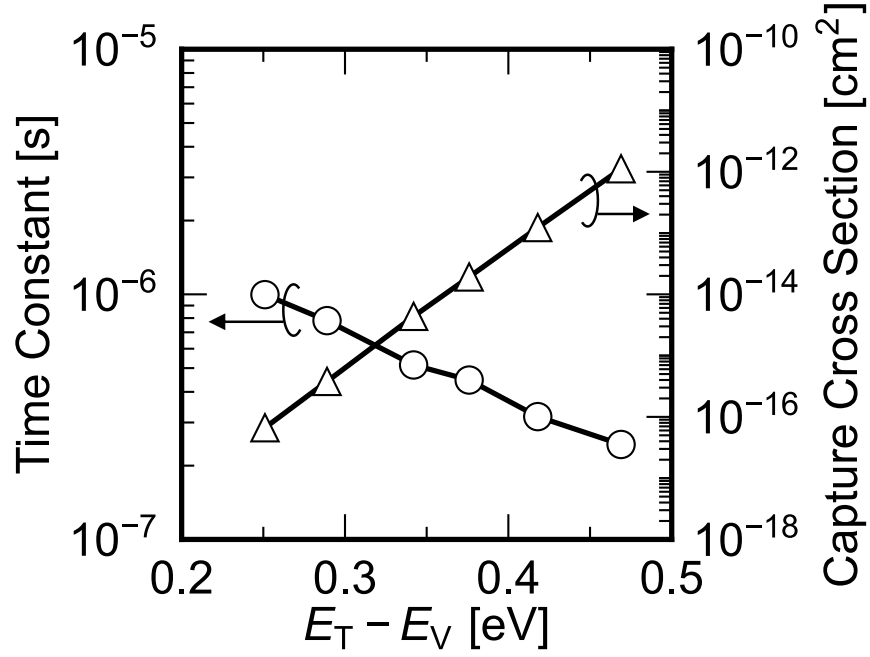


Figure 2.6: Time constant of hole emission from the interface states and capture cross section of the interface states as a function of the energy level from the valence band edge ($E_T - E_V$).

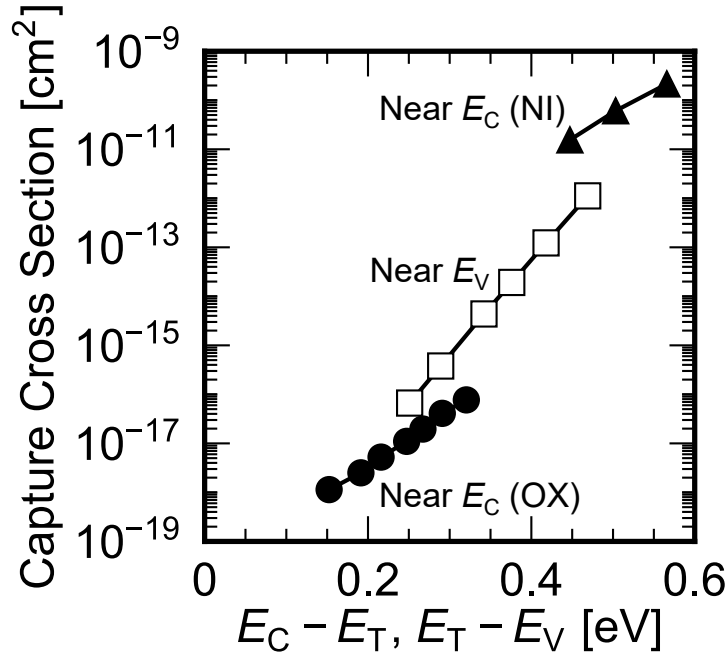


Figure 2.7: Capture cross section of the interface states near the conduction and valence band edges as a function of the energy level from the conduction or valence band edge ($E_C - E_T$ or $E_T - E_V$). "OX" and "NI" denote the interface state near E_C generated by oxidation and nitridation, respectively [4].

and those near the valence band edges. The exponential dependence can be characterized by a slope factor γ [20]:

$$\sigma_{it}(E) = \sigma_{it,0} \exp(\gamma \Delta E) \quad (2.9)$$

where $\sigma_{it,0}$ is a constant. ΔE is $E_C - E_T$ for the interface states near E_C and $E_T - E_V$ for those near E_V . Fitting each dataset with the exponential function yields a γ value of 1.0 for the interface states OX near E_C , 0.9 for the interface states NI near E_C , and 1.8 for the interface state near E_V . Thus, the capture cross sections of interface states near E_V is more strongly dependent on the energy level compared to those near E_C . Capture cross sections generally give information about the charge state of interface states such as acceptor- and donor-type states. In the case of electron traps, acceptor-type states change from neutral (0) to negative (-1) by capturing electrons, while donor-type states change from positive ($+1$) to neutral (0). Due to the attractive force between positively charged donor-type states and electrons, the capture cross sections for donor-type states are larger than those for acceptor-type states. Typically, the capture cross sections for electron traps range from 10^{-18} to 10^{-14} cm^{-2} for acceptor-type states and from 10^{-14} to 10^{-12} cm^{-2} for donor-type states [21–25]. For hole traps, the situation is reversed: acceptor-type states transition from negative (-1) to neutral (0) upon capturing holes, while donor-type states transition from neutral (0) to positive ($+1$). Similarly, since negatively-charged acceptor-type states attract holes, the capture cross sections of acceptor-type states are larger than those of donor-type states. According to the literature [4], the interface states OX possessing smaller capture cross sections and NI possessing larger capture cross sections would be acceptor-type and donor-type states, respectively. Since the capture cross sections near E_V have a wide-range value from 8.9×10^{-13} to 4.5×10^{-17} cm^{-2} , it is difficult to determine the charge states of the interface states.

Figure 2.8 shows the fitting results of G_{pit}/ω - f characteristics when the standard deviation of the surface potential fluctuations was varied as 0.1, 0.5, and 1.0. The experimental G_{pit}/ω - f curve was fitted well when $\sigma = 0.1$ and 0.5. This standard deviation corresponds to a standard deviation of 3–13 meV by multiplying the obtained standard deviation by $kT/q = 25.6$ meV. Note that the standard deviation near the conduction band edge is 4 (about 100 meV), which is significantly larger than that near the valence band edge. Two possible phenomena may explain this discrepancy. The first phenomenon is the literally smaller fluctuation of the surface potential near the valence band edge. In the SiC (0001)/SiO₂ interface, the difference in the sequence of atomic bilayers in SiC at the interface would cause a large fluctuation of the conduction band edge [26], while such fluctuation is much smaller near the valence band edge. The second phenomenon is that, although the actual fluctuations of the surface potential near E_V might be similar to that near E_C , the effective surface potential fluctuations, which carriers feel the fluctuations from the true one, could be weak for holes due to their large effective mass.

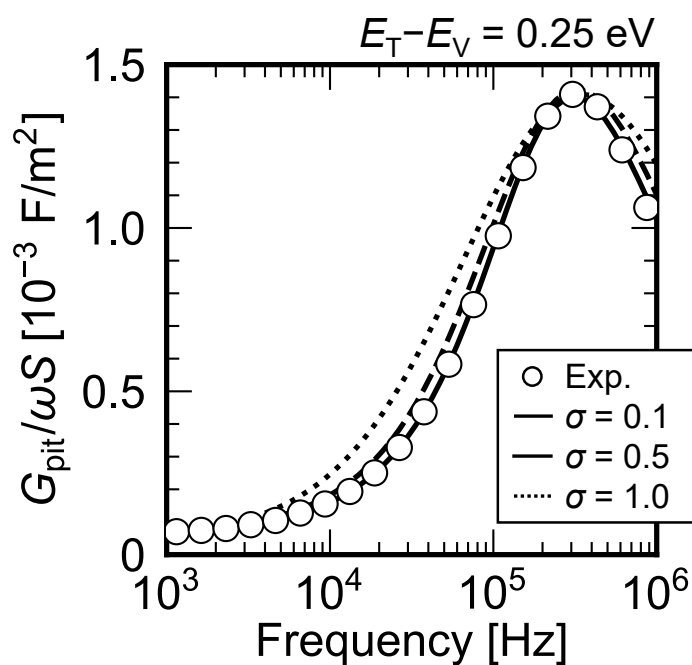


Figure 2.8: Fitting results of interface-state conductance–frequency ($G_{\text{pit}}-f$) characteristics with various surface potential fluctuations ($\sigma = 0.1, 0.5$, and 1.0). The vertical axis is G_{pit} normalized by angular frequency (ω) and the gate area (S).

2.5 Summary

In this chapter, the interface states near the valence band edge for nitrided SiC/SiO₂ interfaces have been investigated using three methods: the high-low, $C-\psi_s$, and conductance methods. The combination of the $C-\psi_s$ and conductance methods revealed that the interface state near the valence band edge exponentially increases near the band edge. The density at $E_T - E_V = 0.2$ eV is $3.9 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$, which is comparable to that near the conduction band edge. The capture cross sections of the interface states near the valence band edge strongly depends on the energy levels from the band edge. The standard deviation of the surface potential fluctuations is 0.1–0.5 (3–13 meV) near the valence band edge, whereas the reported value near the conduction band edge is 4 (about 100 meV), indicating that the surface potential fluctuations for holes (or near E_V) is much smaller and likely flatter compared to those for electrons (or near E_C).

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Chapter 3

Channel Mobility in 4H-SiC (0001) N- and P-Channel MOSFETs

3.1 Introduction

Channel mobility is one of the most important parameters in designing CMOS devices. The ratio of n- and p-channel mobilities determines the channel width of n- and p-channel MOSFETs so that the mutual conductance of both MOSFETs has the same absolute value. At a given channel length, a desirable ratio of channel width is given by [1]:

$$\frac{W_p}{W_n} = \frac{\beta_n}{\beta_p} = \frac{\mu_n}{\mu_p} \quad (3.1)$$

where W_n and W_p are the channel width, β_n and β_p are the mutual conductance, and μ_n and μ_p are the channel mobility. The “n” and “p” subscripts correspond to n- and p-channel MOSFETs, respectively. In general, the channel width of p-channel MOSFETs is larger than that of n-channel MOSFETs because the p-channel mobility is lower than the n-channel mobility.

So far, the mobility in SiC p-channel MOSFETs has been reported in devices with lightly-doped bodies ($< 1 \times 10^{16} \text{ cm}^{-3}$) [2–8]. However, since the lightly-doped body inherently causes short-channel effects, which are accompanied by high integration, a heavily-doped body ($\sim 10^{17} \text{ cm}^{-3}$) is preferable for practical applications. In this chapter, the author fabricated SiC (0001) p-channel MOSFETs with various body doping concentrations and investigated the p-channel mobility, comparing it to the n-channel mobility. Since the gate oxides of both n- and p-channel MOSFETs are formed simultaneously in the actual CMOS process, the gate oxide of both fabricated MOSFETs was formed by the standard process with the same conditions: oxidation of SiC followed by NO annealing.

3.2 Device Fabrication

The process flow and device structure of the fabricated n- and p-channel SiC (0001) MOSFETs are shown in Fig. 3.1. The starting materials were a lightly-doped n-type epilayer with a donor concentration of $5 \times 10^{15} \text{ cm}^{-3}$ on a SiC (0001) n-type substrate for p-channel MOSFETs and a lightly-doped p-type epilayer with an acceptor concentration of $1 \times 10^{15} \text{ cm}^{-3}$ on a SiC (0001) p-type substrate for n-channel MOSFETs. To control impurity concentrations in the body region (body doping concentrations: N_{Body}) with a box profile of 600 nm, multiple-energy ion implantation of Al^+ for the n-channel MOSFETs and N^+ for the p-channel MOSFETs was conducted at room temperature. The body doping concentrations were experimentally determined by capacitance-voltage (C - V) measurements of MOS capacitors fabricated on the same chip as the MOSFETs. The obtained N_{Body} was 4.5×10^{15} , 1.5×10^{16} , 1.2×10^{17} , 5.3×10^{17} , and $2.2 \times 10^{18} \text{ cm}^{-3}$ for the p-channel MOSFETs, while the N_{Body} for the n-channel MOSFETs was 1.5×10^{15} , 2.3×10^{16} , 7.1×10^{16} , $4.2 \times 10^{17} \text{ cm}^{-3}$. The source and drain regions were formed by Al^+ implantation for p^+ regions and P^+ implantation for n^+ regions at 300°C . The designed doping profile was a box profile of 200 nm with a doping density of $2 \times 10^{20} \text{ cm}^{-3}$. Post-implantation annealing was performed in Ar ambient at 1750°C for 20 min with a carbon cap to suppress surface roughening during the high-temperature annealing [9]. After the post-implantation annealing, the carbon cap was removed by O_2 annealing at 900°C for 30 min. Since the implanted impurities are absent in a 10–20 nm-thick SiC from its surface due to the limitation of ion implantation energy, the surface layer was removed by sacrificial oxidation followed by using HF solution. After RCA cleaning, the gate oxide of SiO_2 was formed by dry oxidation at 1300°C for 20 min, followed by NO annealing [10–12] at 1250°C , resulting in an oxide thickness of 32–35 nm. The source and drain contacts were formed by Ti/Al evaporation followed by annealing at 1000°C for the p^+ regions and Al evaporation followed by annealing at 400°C for the n^+ regions. The gate and backside metal were deposited by Al evaporation for both n- and p-channel MOSFETs. The channel length (L) and width (W) were $100 \mu\text{m}$ and 50 – $170 \mu\text{m}$, respectively.

3.3 Characteristics of Fabricated N- and P-Channel MOSFETs

3.3.1 Gate Characteristics

Figure 3.2 shows the gate characteristics for the fabricated n- and p-channel SiC (0001) MOSFETs with various body doping concentrations. The vertical axis is the drain current (I_{D}) normalized by channel length and width ($I_{\text{DN}} = I_{\text{D}} \times L/W$). The applied drain voltage was 0.1 V for the n-channel devices and -0.1 V for the p-channel devices, where the MOSFETs operate in the linear region. The on/off ratio was higher than 10^4 for all

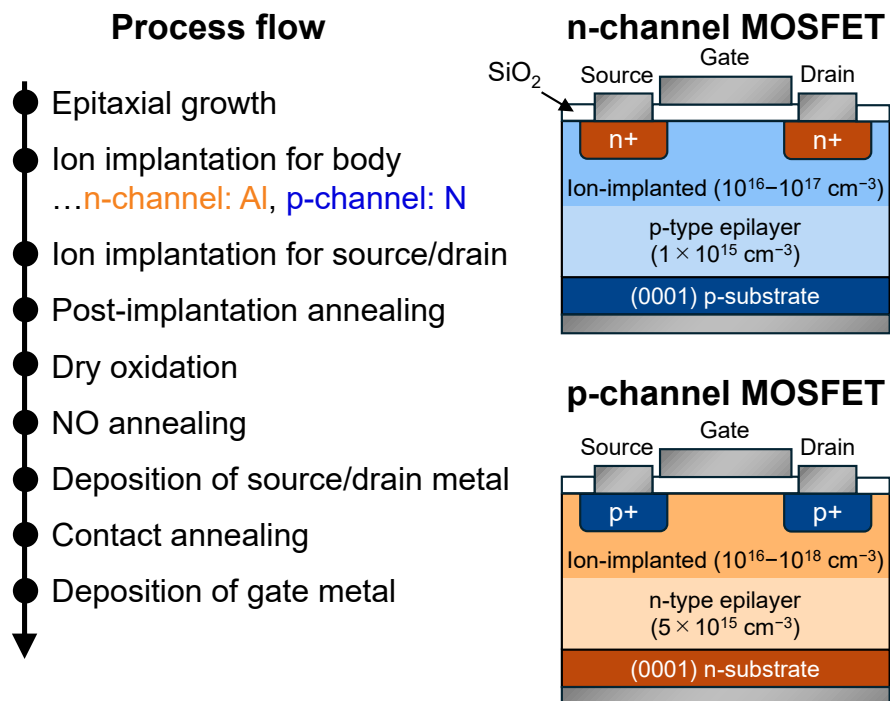


Figure 3.1: Process flow and device structure of the fabricated n- and p-channel SiC(0001) MOSFETs.

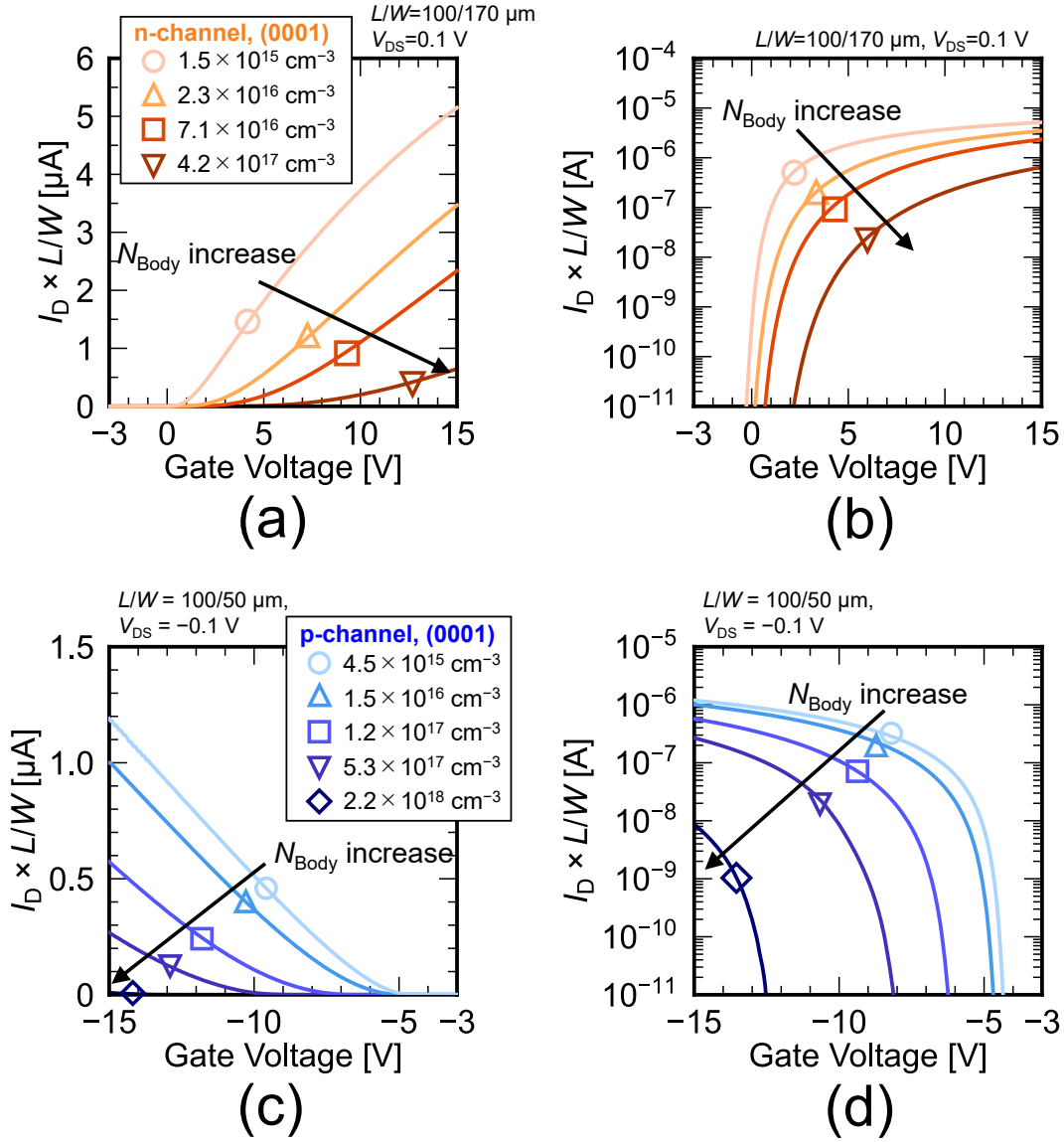


Figure 3.2: Gate characteristics of the fabricated n- and p-channel SiC MOSFETs. Figures (a) and (b) are the linear and semilog plots for the n-channel devices, respectively. Figures (c) and (d) are those for the p-channel devices. The drain current (I_D) was normalized by the channel length (L) and width (W). (©IOP Publishing. Partially reproduced with permission from K. Mikami *et. al.*, *Appl. Phys. Express* **15**, 036503 (2022). All rights reserved.)

devices except for the p-channel MOSFET with $N_{\text{Body}}=2.2 \times 10^{18} \text{ cm}^{-3}$ because this device has a small overdrive voltage of less than 3 V in the measured range. The source-drain leakage current in the OFF-state was less than $1 \times 10^{-11} \text{ A}$, indicating good transistor characteristics. When N_{Body} increases from 10^{15} to 10^{18} cm^{-3} , the threshold voltage of the p-channel MOSFETs negatively increases, whereas that of the n-channel MOSFETs positively increases. A detailed discussion of the threshold voltage will be described in Chapter 5.

3.3.2 Field-Effect Mobility

Field-effect mobility (μ_{FE}) was utilized to characterize channel mobility in this study, given by the following equation [13]:

$$\mu_{\text{FE}} = \frac{L}{WC_{\text{ox}}V_{\text{DS}}} \frac{dI_{\text{D}}}{dV_{\text{GS}}} \quad (3.2)$$

where C_{ox} is the gate oxide capacitance per unit area, V_{DS} is the drain-source voltage, and V_{GS} is the gate-source voltage. The μ_{FE} as a function of the gate voltage is depicted in Fig. 3.3. The maximum μ_{FE} for the p-channel devices decreases from 13.0 to 7.8 cm^2/Vs when N_{Body} increases from 4.5×10^{15} to $5.3 \times 10^{17} \text{ cm}^{-3}$. As for the n-channel devices, the maximum μ_{FE} decreases from 48.8 to 10.3 cm^2/Vs when N_{Body} increases from 1.5×10^{15} to $4.2 \times 10^{17} \text{ cm}^{-3}$. The gate voltage dependence of μ_{FE} for the lightly-doped devices ($N_{\text{Body}} \sim 10^{15} \text{ cm}^{-3}$) is quite different between the n- and p-channel MOSFETs. The p-channel device with $N_{\text{Body}}=4.5 \times 10^{15} \text{ cm}^{-3}$ exhibited a nearly constant mobility of 12–13 cm^2/Vs over the V_{GS} range of -10 to -15 V , while the n-channel device with $N_{\text{Body}}=1.5 \times 10^{15} \text{ cm}^{-3}$ showed a peak mobility of 48.8 cm^2/Vs at $V_{\text{GS}} = 3.0 \text{ V}$ and a decrease in μ_{FE} in the higher V_{GS} region.

3.3.3 Subthreshold Swing

Figure 3.4 illustrates the body doping dependence of subthreshold swing (SS). The SS was taken from a normalized drain-current range of $1 \times 10^{-10} \text{ A} < I_{\text{DN}} < 1 \times 10^{-9} \text{ A}$. The theoretical SS is also shown in Fig. 3.4, where the oxide thickness was 32 nm. The experimental SS for both devices is significantly higher than the theoretical one at a given N_{Body} , which could arise from a high interface state density at the SiC/SiO₂ interface. When a high interface state density is present, SS is expressed by the following equation [14]:

$$SS = \frac{dV_{\text{GS}}}{d \log_{10} I_{\text{D}}} = \frac{kT}{q} \ln 10 \left(1 + \frac{C_{\text{depl}} + q^2 D_{\text{it}}}{C_{\text{ox}}} \right) \quad (3.3)$$

Here, k is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, C_{depl} is the depletion layer capacitance in a semiconductor, and D_{it} is the interface state density. Figure 3.5 shows the D_{it} near E_{C} and E_{V} extracted from SS of the n- and p-channel MOSFETs with various body doping concentrations, assuming the surface potential

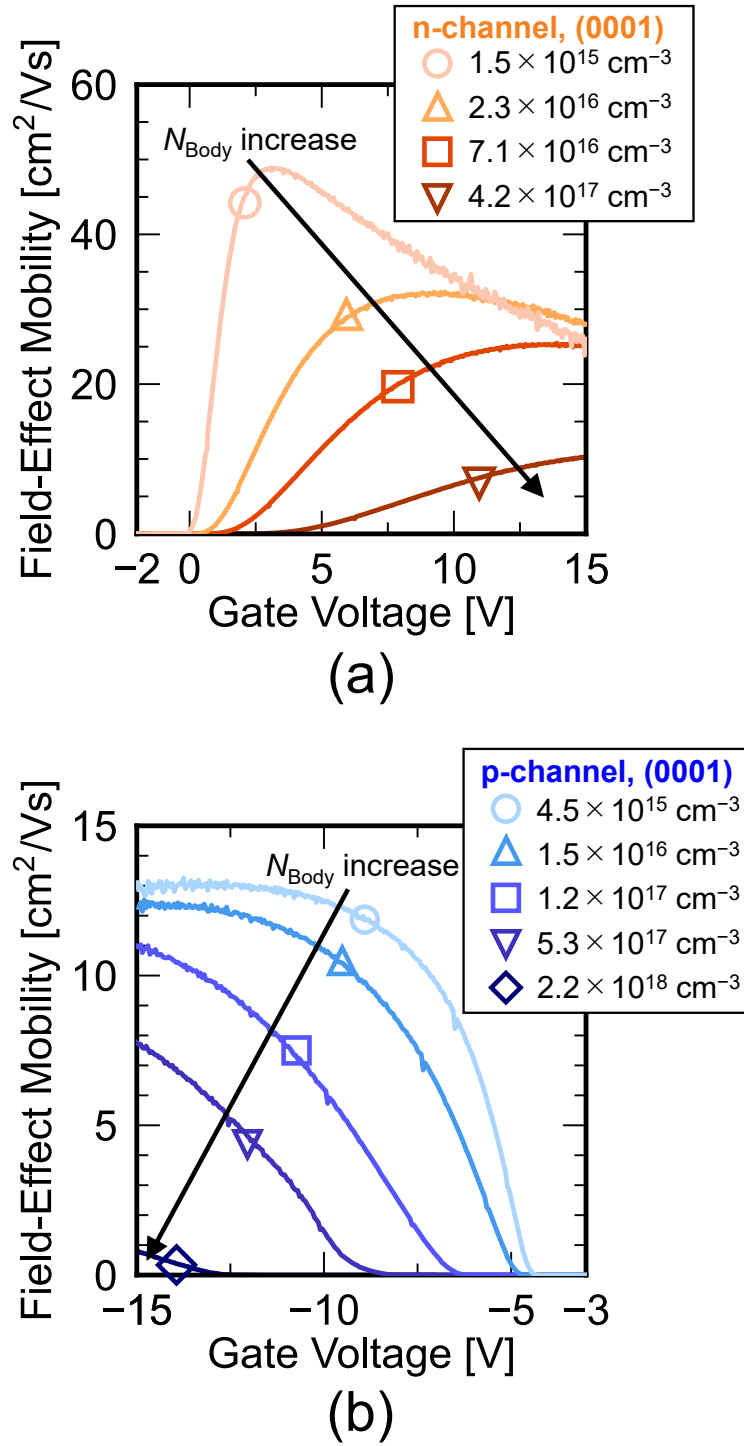


Figure 3.3: Field-effect mobility as a function of the gate voltage for both (a) n-channel and (b) p-channel SiC MOSFETs. (©IOP Publishing. Partially reproduced with permission from K. Mikami *et. al.*, *Appl. Phys. Express* **15**, 036503 (2022). All rights reserved.)

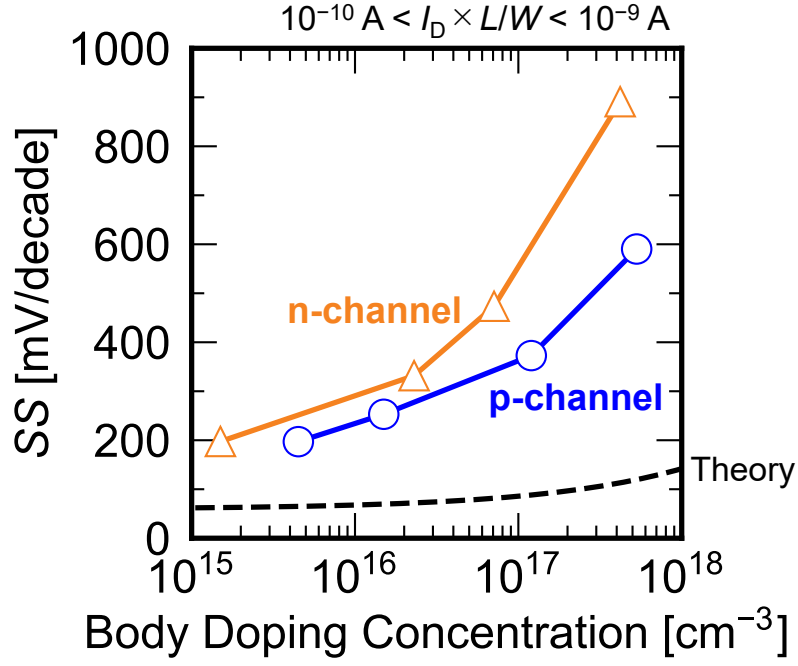


Figure 3.4: Body doping dependence of subthreshold slope (SS) for both n-channel and p-channel SiC MOSFETs.

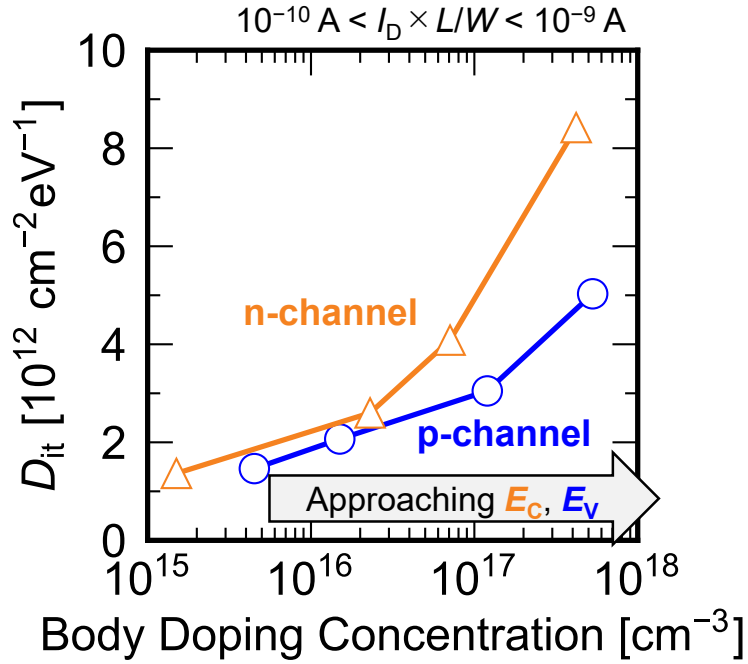


Figure 3.5: Interface state density extracted from the subthreshold slope of the n-channel and p-channel SiC MOSFETs. The D_{it} increase with increasing body doping concentration corresponds to a higher D_{it} closer to the band edges.

is $2\psi_B$ (ψ_B : bulk potential). Here, the D_{it} extracted from SS corresponds to the effective D_{it} which captures electrons/holes when the MOSFETs turn on. At first glance, the increase in N_{Body} appears to cause an increase in D_{it} . However, the horizontal axis (body doping concentration) requires careful interpretation because the surface Fermi level at a given I_{DN} depends on N_{Body} . The N_{Body} dependence of surface Fermi level can be interpreted as follows. Since a higher N_{Body} causes lower drift mobility in the inversion layer due to strong Coulomb scattering in the subthreshold regions, the carrier density needs to be higher in heavily-doped devices than in lightly-doped devices to maintain the same I_{DN} . In other words, the surface Fermi level (the energy level of D_{it}) for heavily-doped devices is closer to the band edges. Therefore, a monotonical D_{it} increase with increasing N_{Body} indicates that D_{it} increases close to both E_C and E_V . It will be discussed that the D_{it} does not depend on N_{Body} in Section 3.5.

Comparing the D_{it} extracted from SS between the n- and p-channel devices, it can be observed that the D_{it} near E_V is lower than that near E_C , especially in the high body doping region (close to the band edges). However, in Chapter 2, it was confirmed that the D_{it} near E_V of 10^{12} – 10^{13} $\text{cm}^{-2}\text{eV}^{-1}$ is comparable to that near E_C . This contradiction can be resolved by taking into account the quantum confinement effects in MOSFETs. The carrier density of MOSFETs (N_{free}) is given by [15]:

$$N_{free} = \sum D_{2D} kT \ln \left[1 + \exp \left(\frac{E_{FS} - \varepsilon}{kT} \right) \right] \quad (3.4)$$

where D_{2D} is the two-dimensional density of states, E_{FS} is the surface Fermi level, and ε is the energy level of subbands. D_{2D} is given by [15]:

$$D_{2D} = \frac{m_d^*}{\pi \hbar^2} \quad (3.5)$$

Here, m_d^* is the density of effective mass and $\hbar$ is the reduced Planck constant. The subband shift from the band edge ($\Delta\varepsilon$) can be calculated by [15]:

$$\Delta\varepsilon = c_1 \left[\frac{(qF\hbar)^2}{2m_z^*} \right]^{1/3} \quad (3.6)$$

where c_1 is a constant (≈ 2.388), F is the surface electric field, and m_z^* is the confinement-direction effective mass. Since the effective mass of holes is larger than that of electrons in SiC, both m_d^* and m_z^* of holes are larger than those of electrons. Thus, compared to n-channel MOSFETs, p-channel MOSFETs have a higher density of states and lower energy levels of subbands. As a result, the surface Fermi level for p-channel MOSFETs is located at a deeper from the band edge than that for n-channel MOSFETs at a given carrier density (drain current), resulting in less carrier trapping in the p-channel MOSFETs. This discussion is schematically illustrated in Figure 3.6, which depicts the band diagrams of n- and p-channel MOSFETs considering the quantum confinement effects. In other words, the D_{it} extracted from SS of the p-channel MOSFETs may be lower than that of the n-channel MOSFETs even though the D_{it} near E_V is almost the same as that near E_C , as obtained in Chapter 2.

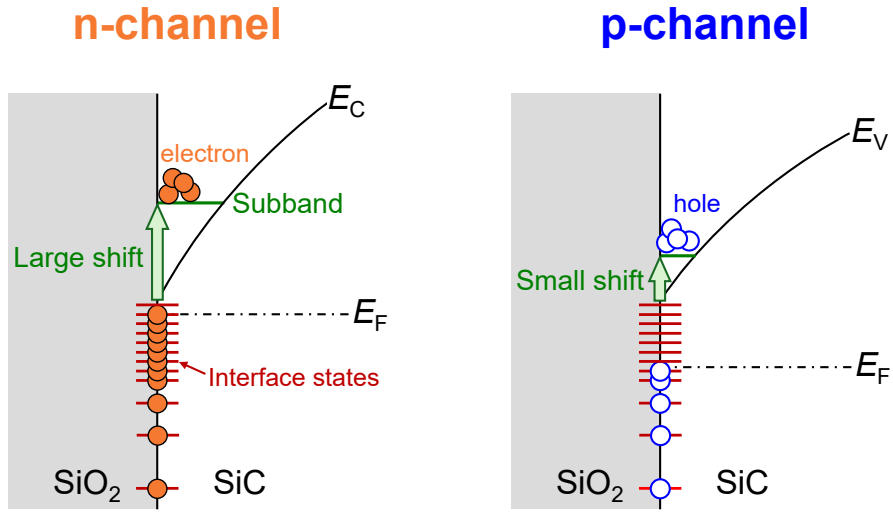


Figure 3.6: Band diagrams of n- and p-channel MOSFETs considering the quantum confinement effects. The surface Fermi level for the p-channel MOSFETs is located at deeper energy from the band edge compared to the n-channel MOSFETs at a given carrier density because of a larger density of states and smaller subband shift originating from the large effective mass of holes.

3.4 Comparison of Field-Effect Mobility Between N- and P-Channel MOSFETs

In order to understand p-channel mobility in SiC MOSFETs, the p-channel mobility was compared to the n-channel mobility, considering the body doping concentration, gate voltage, and difference in bulk mobility between electrons and holes. Figure 3.7 depicts the field-effect mobility normalized by the bulk mobility (μ_{FE}/μ_{bulk}) as a function of the effective normal field for the fabricated n- and p-channel MOSFETs. In this study, the μ_{bulk} was taken as $1020 \text{ cm}^2/\text{Vs}$ [13] for electrons (n-channel) and $95 \text{ cm}^2/\text{Vs}$ [16] for holes (p-channel). The effective normal field (E_{eff}) represents the average electric field perpendicular to the oxide/semiconductor interface experienced by the channel carriers, defined by the following equation [17, 18]:

$$E_{eff} = \sqrt{\frac{2qN_{Body}(2\psi_B + |V_{BS}|)}{\epsilon_s}} + \frac{\eta q N_S}{\epsilon_s} \quad (3.7)$$

where V_{BS} is a body bias (usually 0 V unless intentionally applied), ϵ_s is the permittivity of the semiconductor, and N_S is the total carrier density obtained by quasi-static Split C - V measurement. η is the ratio of carrier density contributing to the electric field in the inversion layer, which was assumed to be $1/3$ [19, 20] for both devices. In general, trapped carriers do not contribute to E_{eff} because trapped carriers are located just at the oxide/semiconductor interface. In SiC MOSFETs, however, it has been reported that carbon-related defects would be formed in the SiC side during oxidation of SiC [21]. In addition, the energy distribution of D_{it} plotted with respect to the band edge of the two-dimensional density of states is almost uniquely determined by the oxide formation condition [22]. These results suggest that a significant portion of the “interface states” could be present in SiC very close to the interface. Thus, the trapped carriers near the SiC/SiO₂ interface could contribute to E_{eff} , and the total carrier density was used for E_{eff} calculation.

Two phenomena can be observed in Fig. 3.7. The first phenomenon is that the μ_{FE}/μ_{bulk} ratio of the p-channel MOSFETs is approximately twice that of the n-channel devices. For the lightly-doped MOSFETs, the p-channel mobility represents 13% of the bulk mobility, and the n-channel mobility represents 5% of the bulk mobility. This phenomenon might originate from less carrier trapping in the p-channel MOSFETs due to the larger effective mass of holes, as mentioned in the previous section. The second phenomenon is that the decrease in μ_{FE}/μ_{bulk} ratio as E_{eff} increases is less pronounced for the p-channel devices but more significant for the n-channel devices, especially in the high E_{eff} region. For example, the maximum μ_{FE}/μ_{bulk} ratio for the p-channel devices slightly decreases from 0.13 for $N_{Body}=1.5 \times 10^{16} \text{ cm}^{-3}$ to 0.08 for $N_{Body}=5.3 \times 10^{17} \text{ cm}^{-3}$, whereas the μ_{FE}/μ_{bulk} ratio for the n-channel devices decreases from 0.03 for $N_{Body}=2.3 \times 10^{16} \text{ cm}^{-3}$ to 0.01 for $N_{Body}=4.2 \times 10^{17} \text{ cm}^{-3}$. This difference might arise from the difference in carrier scattering in the inversion layer between the n- and p-channel MOSFETs. The possible origin is discussed in the next

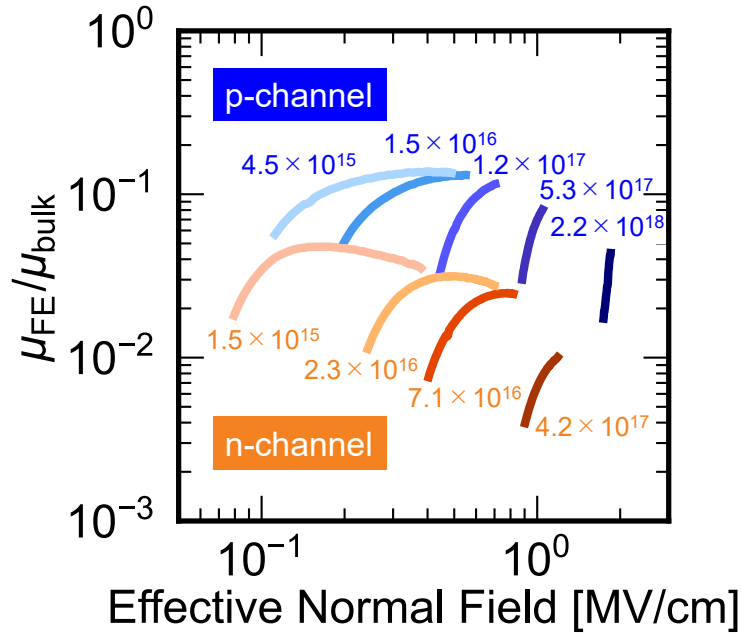


Figure 3.7: Field-effect mobility normalized by the bulk mobility (μ_{FE}/μ_{bulk}) as a function of the effective normal field for the n- and p-channel SiC(0001) MOSFETs. The μ_{bulk} used in this study was $1020 \text{ cm}^2/\text{Vs}$ for electrons (n-channel) and $95 \text{ cm}^2/\text{Vs}$ (p-channel) for holes. The numbers in the figure indicate the body doping concentration with a unit of cm^{-3} . (©IOP Publishing. Partially reproduced with permission from K. Mikami *et. al.*, *Appl. Phys. Express* **15**, 036503 (2022). All rights reserved.)

section.

3.5 Insight into Carrier Scattering in Inversion Layer by Using Body Biasing Technique

3.5.1 Basis of Carrier Scattering in Inversion Layer

In this subsection, a general understanding of carrier scattering in the inversion layer is described. Figure 3.8 shows a schematic illustration of the expected carrier scattering in SiC MOSFETs. Ionized-impurity, phonon, and surface-roughness scatterings are well-known types of scatterings in Si MOSFETs [19]. In SiC MOSFETs, in addition to the scatterings in Si MOSFETs, Coulomb scattering due to interface charges (trapped electrons/holes and fixed charges) [23–25] would strongly affect the drift mobility. Drift mobility (μ_{drift}) limited by these scatterings is expressed by using Matthiessen's rule:

$$\frac{1}{\mu_{\text{drift}}} = \frac{1}{\mu_{\text{ii}}} + \frac{1}{\mu_{\text{ph}}} + \frac{1}{\mu_{\text{sr}}} + \frac{1}{\mu_{\text{it}}} \quad (3.8)$$

where μ_{ii} , μ_{ph} , μ_{sr} , and μ_{it} are the mobility limited by ionized-impurity, phonon, surface-roughness, and interface-charge scattering, respectively. Strictly speaking, the mobility limited by Coulomb scattering due to interface charges can be divided into two components: one due to trapped electrons/holes and one due to fixed charges. This is because the density (scattering centers) of trapped electrons/holes depends on gate voltages and temperatures, while fixed charges maintain their density. The characteristics of each scattering mechanism are explained as follows.

- ***Ionized-impurity scattering***

Mobility limited by ionized-impurity scattering strongly depends not only on the body doping concentration ($\mu_{\text{ii}} \propto N_{\text{Body}}^{-1}$) but also on the sheet carrier density in the inversion layer ($\mu_{\text{ii}} \propto N_{\text{S}}$) because of screening effects [19]. Since an increase in the sheet carrier density causes an increase in the effective normal field, the mobility limited by ionized impurities increases when it is plotted against E_{eff} , as shown in Fig. 3.8. In Si MOSFETs, ionized-impurity scattering limits carrier mobility at low temperatures due to strong Coulomb scattering and in a low N_{S} region because of weak screening effects.

- ***Phonon scattering***

Phonon scattering has a strong temperature dependence ($\mu_{\text{ph}} \propto T^{-\alpha}$), where a constant α is 1.75 for Si MOSFETs [26], while the reported α in SiC MOSFETs is 1.67 [27] and is being discussed at the present stage. In addition, in the inversion layer, the phonon-limited mobility weakly depends on the effective normal field ($\mu_{\text{ph}} \propto E_{\text{eff}}^{-\beta}$) due

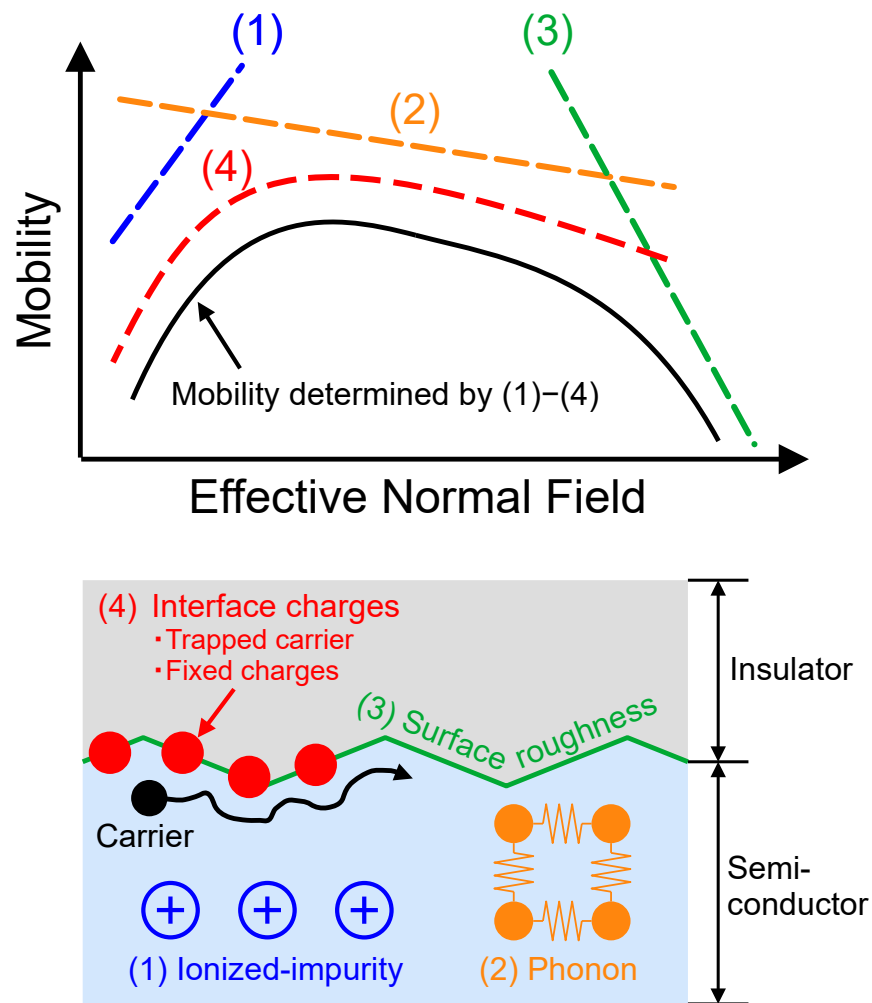


Figure 3.8: Schematic illustration of the expected carrier scattering in SiC MOSFETs.

to the quantum-confinement effects. In Si MOSFETs, phonon scattering dominates carrier mobility at high temperatures and in the intermediate E_{eff} range near RT.

- ***Surface-roughness scattering***

Surface-roughness scattering degrades carrier mobility in high E_{eff} regions because carriers are located close to the semiconductor surface by a high E_{eff} . The mobility limited by surface roughness is expressed as $\mu_{\text{sr}} \propto E_{\text{eff}}^{-\gamma}$, where γ is a parameter depending on surface roughness caused by crystal orientation and device processes.

- ***Interface-charge scattering***

Interface charges, such as electrons/holes trapped at interface states and fixed charges near the interface, are one of the Coulomb scattering centers. The mobility limited by these charges shows a complex behavior with respect to the effective normal field. It is important to note that the mobility is affected by their density, measurement temperature, and sheet carrier density due to the screening effects in the same manner as ionized-impurity scattering. A high E_{eff} causes a carrier distribution close to the scattering centers, thereby strongly affecting carrier mobility in the high E_{eff} region. Furthermore, since the density of trapped carriers is highly dependent on the surface Fermi level (gate voltage) and temperature, the mobility limited by trapped electrons and holes is likely to exhibit even more complex behavior. The influence of interface-charge scattering on mobility is small in Si MOSFETs unless interface charges are intentionally incorporated during device processes or carrier injections by a high gate voltage [19]. On the other hand, interface-charge scattering should be considered in SiC MOSFETs because a high interface state density and fixed charges (see Chap. 5) exist in SiC/SiO₂ structures.

3.5.2 Body Biasing Technique

Applying a bias to the body electrode of MOSFETs can control the effective normal field independently from the body doping concentration. A negative and a positive body biasing enhances the effective normal field in n- and p-channel MOSFET, respectively. Figure 3.9 depicts the schematic MOS band diagrams without and with body biasing in n-channel MOSFETs. When an appropriate body bias is applied to MOSFETs with a lightly-doped body, the E_{eff} for the lightly-doped MOSFETs becomes the same as that for the heavily-doped MOSFETs. The appropriate body bias can be calculated based on Eq. (3.7) so that $\sqrt{2qN_{\text{Body}}(2\psi_{\text{B}} + |V_{\text{BS}}|)}$ for the lightly-doped MOSFETs with body biasing becomes $\sqrt{4qN_{\text{Body}}\psi_{\text{B}}}$ for the heavily-doped MOSFETs without body biasing. Under appropriate body bias conditions, the lightly- and heavily-doped MOSFETs have the same E_{eff} but a different N_{Body} . Thus, the impact of ionized-impurity scattering can be discussed by this body biasing technique.

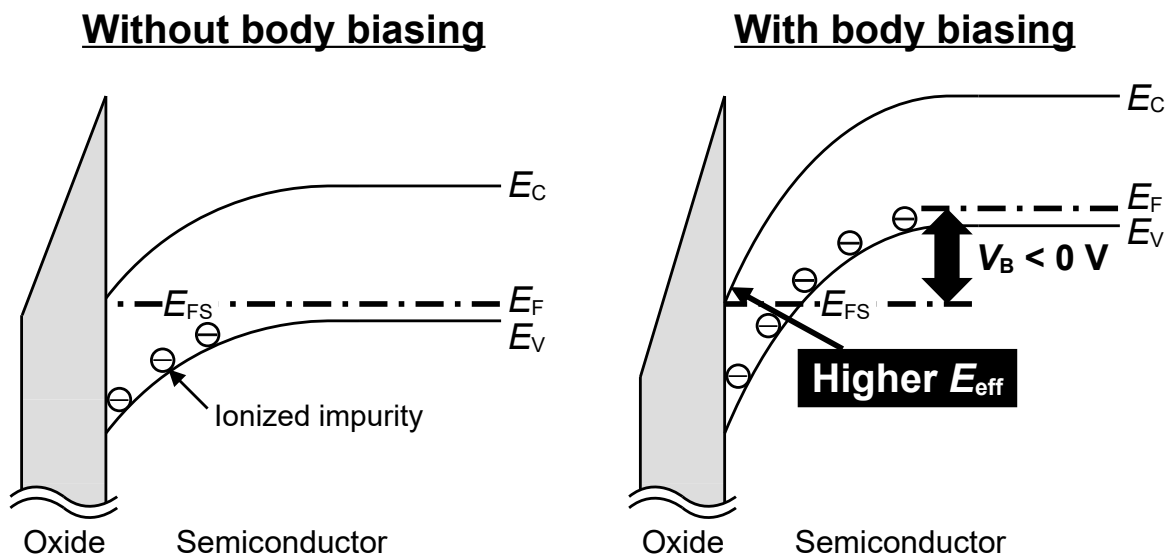


Figure 3.9: Schematic MOS band diagrams without and with body biasing in n-channel MOSFETs.

3.5.3 Experimental Results and Discussion

Figure 3.10 illustrates the field-effect mobility as a function of the effective normal field for both n- and p-channel MOSFETs. The solid lines and symbols represent the field-effect mobility without body biasing and with the appropriate body biasing, respectively. As E_{eff} of lightly-doped MOSFETs increases by applying V_{BS} , the μ_{FE} noticeably decreases, and the μ_{FE} for lightly-doped MOSFETs with body biasing takes the same values as that for the heavily-doped MOSFETs without body biasing at a given E_{eff} . For example, the square symbols of the n-channel MOSFETs, representing the μ_{FE} for the $N_{\text{Body}} = 7.1 \times 10^{16} \text{ cm}^{-3}$ device with $V_{\text{BS}} = -14 \text{ V}$, exactly follow the μ_{FE} for the $N_{\text{Body}} = 4.2 \times 10^{17} \text{ cm}^{-3}$ device without body biasing. Consequently, the μ_{FE} for both n- and p-channel MOSFETs depends on the effective normal field rather than the body doping concentration, suggesting that the ionized impurities are not one of the dominant scattering centers in both n- and p-channel SiC MOSFETs. Previous studies on SiC n-channel MOSFETs have also reported that ionized impurities do not primarily influence channel mobility [23]. The present study revealed that the mobility decrease with increasing N_{Body} is linked to the high E_{eff} for both n- and p-channel MOSFETs.

As mentioned in Subsection 3.5.1, the scattering mechanisms with a function of E_{eff} are phonon, surface-roughness, and interface-charge scattering. Among these scatterings, phonon scattering could not become the origin of the different mobility degradation between the n- and p-channel devices for two reasons. The first reason is that phonon scattering does not dominate carrier mobility in the high E_{eff} range ($\sim 1 \text{ MV/cm}$) at room temperature, as confirmed by the theoretical calculation of carrier scattering in SiC MOSFETs [24]. The second reason is that in Si MOSFETs, the parameter of α for phonon scattering takes the same value for electrons and holes [26]. Thus, the possible origins are surface-roughness and interface-charge scatterings. Based on the result that trapped hole density is lower than trapped electron density in SiC MOSFETs, interface-charge scattering caused by trapped carriers in the p-channel MOSFETs should be weaker than that in the n-channel MOSFETs. Regarding surface-roughness scattering, the γ parameter for surface-roughness scattering is 2.6 for electrons (n-channel) and 1.5 for holes in Si MOSFETs [26], meaning that surface-roughness scattering has a large influence on the electron mobility degradation. Furthermore, scattering caused by surface potential fluctuations must be considered in SiC MOSFETs because the large potential fluctuations of the conduction band may strongly affect the electron mobility, while such scattering is weak in the p-channel MOSFETs due to nearly flat surface potential. Therefore, surface-roughness scattering, Coulomb scattering due to trapped carriers, and scattering caused by surface potential fluctuations are the possible origins for the difference in mobility degradation in the high E_{eff} region between the n- and p-channel MOSFETs.

In addition to the above discussion on the scattering mechanisms, the results presented in Fig. 3.10 provide insights into the influence of the body doping concentration on SiC/SiO₂

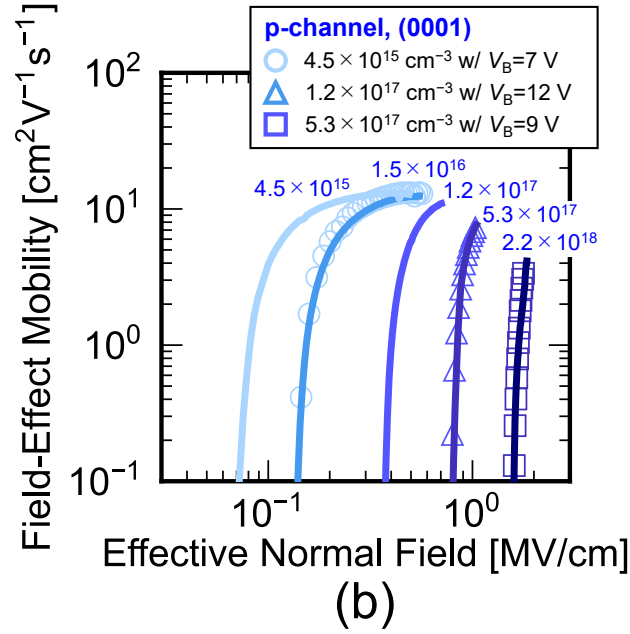
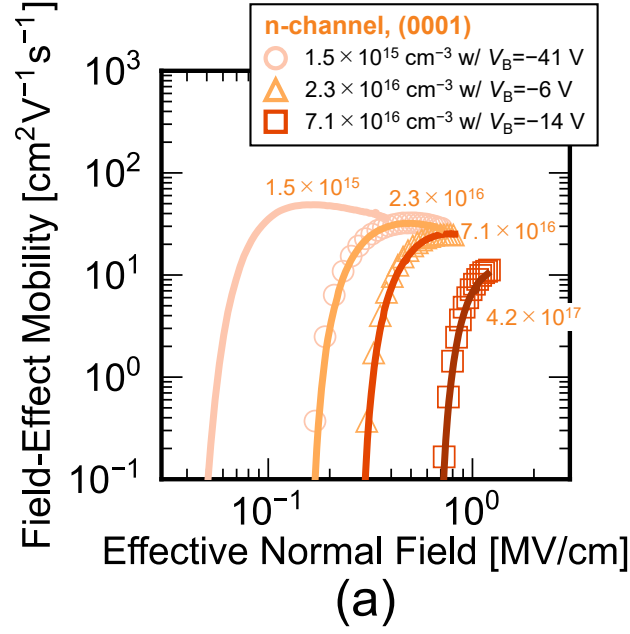


Figure 3.10: Field-effect mobility as a function of the effective normal field for the (a) n-channel and (b) p-channel SiC(0001) MOSFETs with (symbol) and without (line) applied body bias (V_{BS}).

interface states. As mentioned in Section 3.3.3, while the higher D_{it} for heavily-doped MOSFETs would indicate a high D_{it} near the band edges, the possibility of a dependence of the interface trap density (D_{it}) on N_{Body} cannot be ruled out. If D_{it} indeed depends on N_{Body} , the μ_{FE} for high- D_{it} devices should have a lower μ_{FE} than low- D_{it} devices at a given E_{eff} . However, the μ_{FE} for low N_{Body} devices with the appropriate body bias exactly follows that for high N_{Body} devices at a given E_{eff} . This result suggests that the interface state density does not depend on the body doping concentration. Thus, the D_{it} both near E_C and E_V are independent of the body doping concentration, and it is certain that in Fig. 3.5, the D_{it} for devices with a higher N_{Body} is the interface state density located closer to the band edges, compared to the D_{it} for the lightly-doped devices.

3.6 Summary

In this chapter, SiC (0001) p-channel MOSFETs with various body doping concentrations (4.5×10^{15} – 2.2×10^{18} cm $^{-3}$) were fabricated, and the p-channel mobility was investigated by comparing it to the n-channel mobility. Considering the difference in the bulk mobility between electrons and holes, the p-channel mobility is higher than the n-channel mobility. This is attributed to trapped hole density is lower than trapped electron density due to the larger effective mass of holes, even though the D_{it} distribution is almost the same near E_C and E_V . Moreover, by using the body biasing technique, it was found that ionized-impurity scattering has a limited influence on the field-effect mobility and the mobility degradation in heavily-doped MOSFETs originates from scattering caused by high E_{eff} for both n- and p-channel MOSFETs. The possible scatterings are surface-roughness scattering, Coulomb scattering due to trapped electrons/holes, and scattering caused by surface potential fluctuations.

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Chapter 4

Channel Mobility in 4H-SiC (11 $\bar{2}$ 0) and (1 $\bar{1}$ 00) P-Channel MOSFETs

4.1 Introduction

In Chapter 3, the author investigated the mobility in SiC (0001) p-channel MOSFETs for the application to SiC planar CMOS technology. Towards high-performance SiC CMOS, FinFETs present a promising alternative to conventional planar devices because of their low power consumption, fast switching, and high integrity [1, 2]. Given that 4H-SiC (0001) wafers are commercially available, the MOS channels are mainly formed on the nonpolar faces, such as (11 $\bar{2}$ 0) and (1 $\bar{1}$ 00). Thus, it is essential to investigate the MOS channel properties on the nonpolar faces for designing SiC-FinFET-based CMOS. So far, channel mobility in the nonpolar-face n-channel MOSFETs and its interface properties have been investigated [3–13]. In comparison to the typical mobility of 40 cm²/Vs in the (0001) n-channel MOSFETs, a higher mobility of approximately 100 cm²/Vs was demonstrated in the nonpolar-face MOSFETs. These crystal faces are already in practical use for the trench-type power MOSFETs. However, the study on the nonpolar-face p-channel MOSFETs does not exist except for one study investigating only the (11 $\bar{2}$ 0) devices with a lightly-doped n-body ($\sim 10^{15}$ cm⁻³) [14]. As mentioned in Chapter 1, the heavily-doped MOSFETs are essential for practical CMOS applications. Therefore, in this chapter, the author fabricated SiC (11 $\bar{2}$ 0) and (1 $\bar{1}$ 00) p-channel MOSFETs with various body doping concentrations (N_{Body}) up to approximately 10^{18} cm⁻³ to investigate p-channel mobility on the nonpolar faces comprehensively.

4.2 Device Fabrication

Lateral nonpolar-face p-channel MOSFETs were fabricated on n-type epilayers grown on n-type SiC (11 $\bar{2}$ 0) and (1 $\bar{1}$ 00) substrates. The (11 $\bar{2}$ 0) and (1 $\bar{1}$ 00) substrates were prepared by vertically slicing SiC ingots grown on (000 $\bar{1}$). The donor concentration of the epilayers

was 4.5×10^{15} , 8.4×10^{16} , and $8.3 \times 10^{17} \text{ cm}^{-3}$ for the ($11\bar{2}0$) samples and 1.5×10^{16} , 5.0×10^{16} , and $4.4 \times 10^{17} \text{ cm}^{-3}$ for the ($1\bar{1}00$) samples. N^+ ion implantation to the most lightly-doped samples was conducted to prepare devices with heavily-doped n-body ($\sim 10^{18} \text{ cm}^{-3}$), resulting in $2.1 \times 10^{18} \text{ cm}^{-3}$ for the ($11\bar{2}0$) sample and $1.4 \times 10^{18} \text{ cm}^{-3}$ for the ($1\bar{1}00$) sample. The source and drain regions were formed by Al^+ implantation at 300°C . The designed doping profile was a box profile of 200 nm with a doping density of $2 \times 10^{20} \text{ cm}^{-3}$. Post-implantation annealing was performed in Ar ambient at 1750°C for 20 min with a carbon cap to suppress surface roughening during the high-temperature annealing [15]. After the post-implantation annealing, the carbon cap was removed by O_2 annealing at 900°C for 30 min. Then, sacrificial oxidation was performed at 1300°C for 3 min, and the oxidized layer was removed by wet etching. The gate oxide was formed by thermal oxidation at 1300°C for 3 min, followed by NO annealing [16–18] at 1250°C for 70 min, resulting in an oxide thickness of about 40 nm. Note that the oxidation time of 3 min was shorter than that of the (0001) MOSFETs in Chapter 3 because of the faster oxidation rate on the nonpolar faces [19]. The source, drain, gate, and backside electrodes were the same as the (0001) devices. The channel length (L) and width (W) were 100 μm and 50 μm , respectively. MOSFETs with two different channel directions, perpendicular and parallel to the c -axis, were fabricated side by side.

4.3 Characteristics of Fabricated MOSFETs

4.3.1 Gate Characteristics

Figure 4.1 shows the gate characteristics for the fabricated nonpolar-face p-channel MOSFETs. The vertical axis represents the drain current (I_D) normalized by channel length and width ($I_{\text{DN}} = I_D \times L/W$). The applied drain voltage was -0.1 V . As N_{Body} increases, the threshold voltage for both devices decreases. At a given crystal face and N_{Body} , the drain current in the strong inversion regions clearly depends on the channel direction perpendicular and parallel to the c -axis, whereas the drain current in the subthreshold regions perpendicular to the c -axis is comparable to that parallel to the c -axis. Taking the ($1\bar{1}00$) device with $N_{\text{Body}} = 1.5 \times 10^{16} \text{ cm}^{-3}$ as an example, the perpendicular and parallel drain currents show different values within the gate voltage range of -12 to -17 V (strong inversion region), while they are almost equal near the gate voltage of -7.5 V (subthreshold region).

4.3.2 Field-Effect Mobility

Figure 4.2 depicts the field-effect mobility (μ_{FE}) as a function of the gate voltage for the ($11\bar{2}0$) and ($1\bar{1}00$) p-channel MOSFETs. The μ_{FE} depends on the crystal faces and channel directions, which will be described in the following sections. The ($11\bar{2}0$) devices with the most lightly-doped body exhibited mobilities of 25.3 and 20.2 cm^2/Vs in the channel

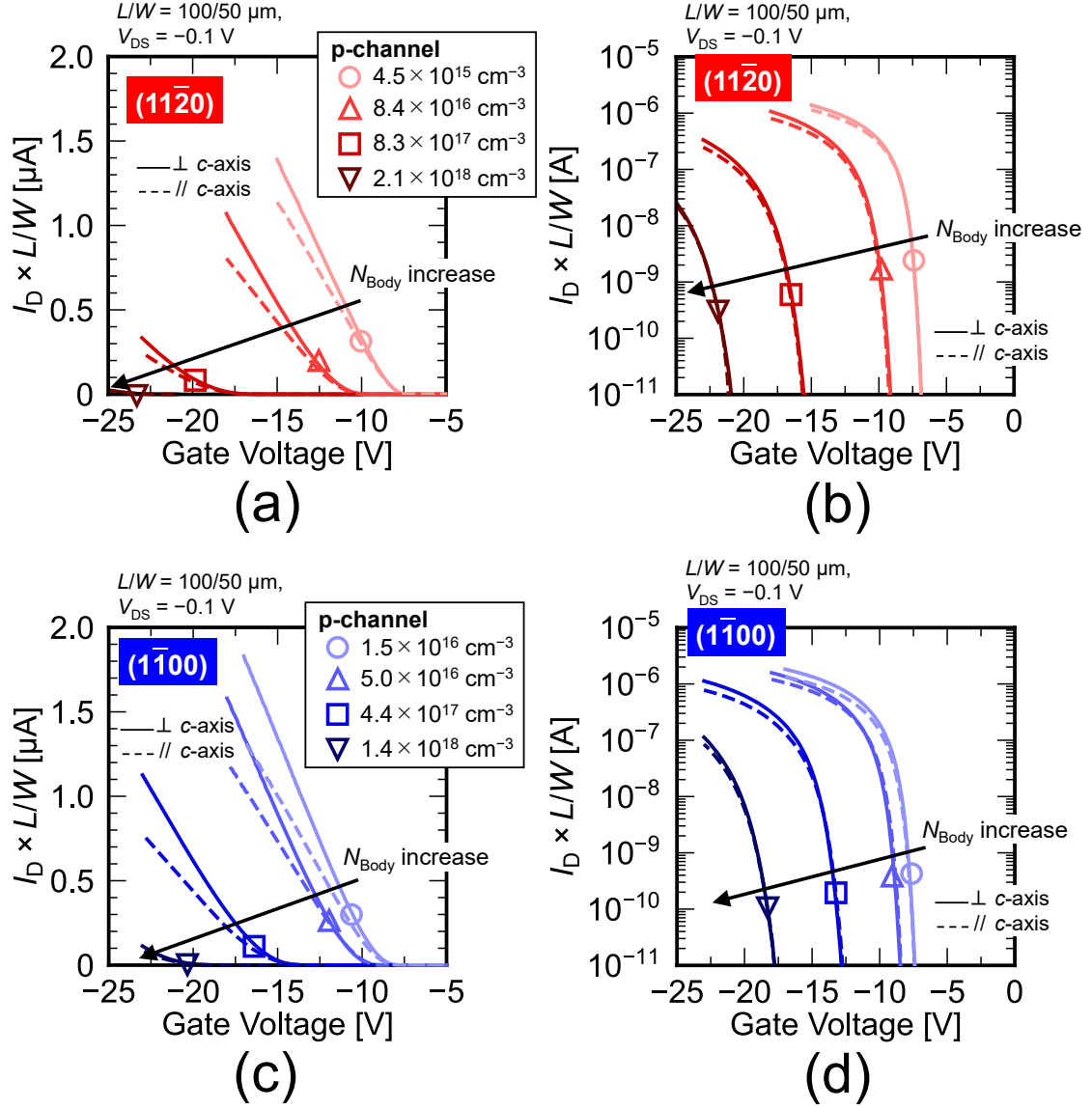


Figure 4.1: Gate characteristics of the SiC p-channel MOSFETs fabricated on (11 $\bar{2}0$) and (1 $\bar{1}00$). Figures (a) and (b) are the linear and semilog plots for the (11 $\bar{2}0$) devices, respectively. Figures (c) and (d) are those for the (1 $\bar{1}00$) devices. The drain current (I_D) was normalized by the channel length (L) and width (W). ((©IEEE. Partially reproduced with permission from K. Mikami *et. al.*, *IEEE Electron Device Lett.* **45**, 1113 (2024). All rights reserved.)

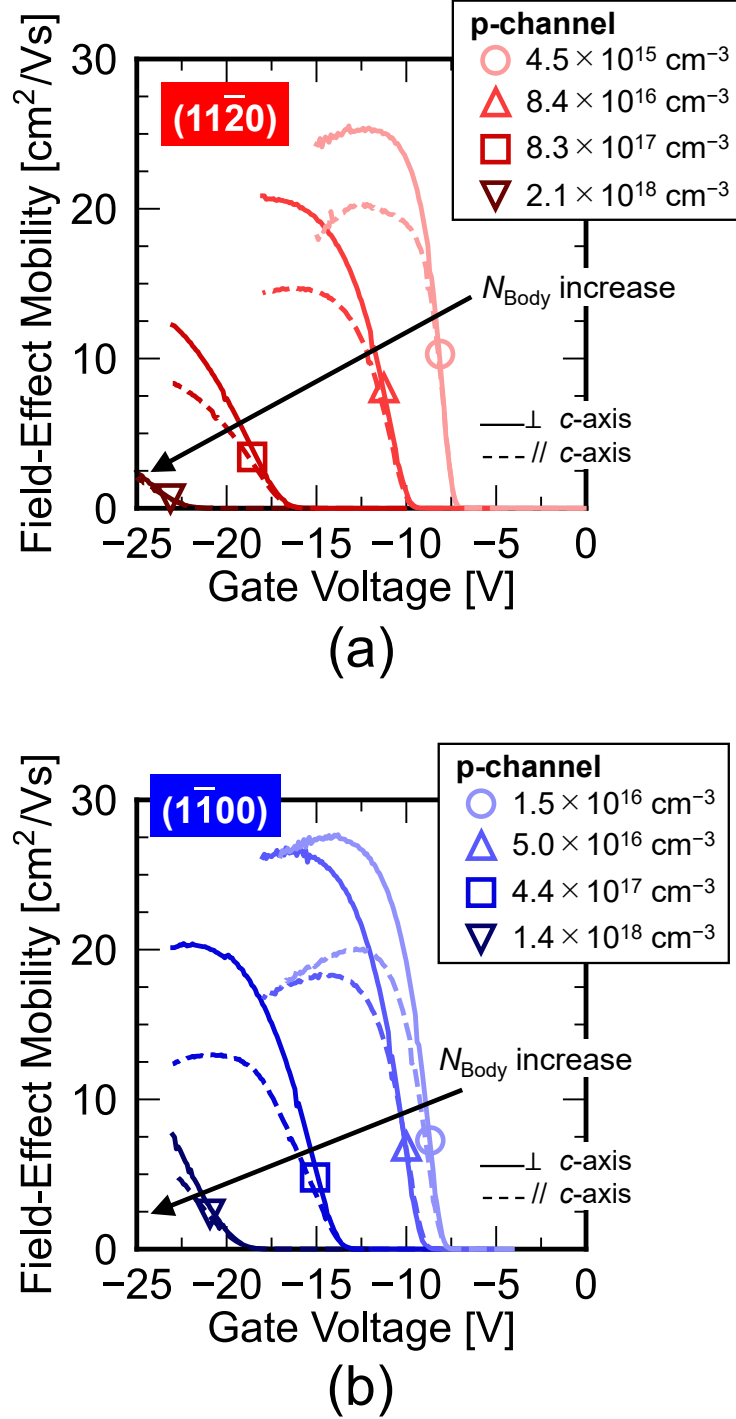


Figure 4.2: Field-effect mobility as a function of the gate voltage for the SiC p-channel MOSFETs fabricated on $(11\bar{2}0)$ and $(1\bar{1}00)$. The highest mobility ever reported for SiC p-channel MOSFETs was achieved on $(1\bar{1}00)$ with the channel direction perpendicular to the c -axis. (©IEEE. Partially reproduced with permission from K. Mikami *et. al.*, *IEEE Electron Device Lett.* **45**, 1113 (2024). All rights reserved.)

directions perpendicular and parallel to the c -axis, respectively, while the $(1\bar{1}00)$ devices exhibited mobilities of 27.5 and 20.0 cm^2/Vs in the channel directions perpendicular and parallel to the c -axis, respectively. The highest mobility of 27.5 cm^2/Vs ever reported for SiC p-channel MOSFETs [14, 20–27] was achieved on the $(1\bar{1}00)$ in the channel direction perpendicular to the c -axis. Note that this mobility was underestimated due to the source and drain parasitic resistances. Thus, the actual channel mobility was extracted by using two MOSFETs with different channel lengths (50 and 100 μm). As a result, the actual mobility was found to be 31.5 cm^2/Vs for the $(1\bar{1}00)$ device with $N_{\text{Body}}=1.5 \times 10^{16} \text{ cm}^{-3}$. Although a negative shift of threshold voltage and a decrease in maximum μ_{FE} ($\mu_{\text{FE,max}}$) were observed with increasing N_{Body} , a high mobility of 20.3 cm^2/Vs was still obtained for the $(1\bar{1}00)$ device with a high N_{Body} of $4.4 \times 10^{17} \text{ cm}^{-3}$.

4.4 P-Channel Mobility on $(11\bar{2}0)$ and $(1\bar{1}00)$

The $\mu_{\text{FE,max}}$ in p-channel MOSFETs on (0001) , $(11\bar{2}0)$, and $(1\bar{1}00)$ is shown in Fig. 4.3. The solid and broken lines represent the $\mu_{\text{FE,max}}$ in the channel direction perpendicular and parallel to the c -axis, respectively. The following three phenomena can be observed.

- (1) $\mu_{\text{FE,max}}$ depends on the crystal face. At a given N_{Body} , the highest mobility was observed in the $(1\bar{1}00)$ devices, followed in order by the $(11\bar{2}0)$ and (0001) devices.
- (2) For the nonpolar-face devices, the $\mu_{\text{FE,max}}$ in the channel direction perpendicular to the c -axis is higher than that parallel to the c -axis. Note that the channel mobility on (0001) was independent of the channel direction: $\langle 11\bar{2}0 \rangle$ and $\langle 1\bar{1}00 \rangle$.
- (3) The $\mu_{\text{FE,max}}$ on the $(11\bar{2}0)$ and $(1\bar{1}00)$ monotonically decreases as N_{Body} increases, similar to that on the (0001) devices.

4.4.1 Crystal Face Dependence

The phenomenon (1), the crystal-face dependence of $\mu_{\text{FE,max}}$, may arise from differences in interface state density (D_{it}) between crystal faces. It is known that the D_{it} near the conduction band edge (E_C) strongly depends on the crystal faces. The high n-channel mobility on the nonpolar faces mainly originates from the lower D_{it} near E_C on the nonpolar faces [3, 9, 12]. Thus, the D_{it} near the valence band edge (E_V) was extracted from the subthreshold swing [28] taken from a normalized drain-current range of $1 \times 10^{-9} \text{ A} < I_{\text{DN}} < 1 \times 10^{-8} \text{ A}$, and the extracted D_{it} is depicted in Fig. 4.4. As mentioned in Subsection 3.3.3, the D_{it} for MOSFETs with a higher N_{Body} corresponds to D_{it} closer to E_V . In the case of heavily-doped devices, the extracted D_{it} is $1.0 \times 10^{13} \text{ cm}^{-2}\text{eV}^{-1}$ for the (0001) device with $N_{\text{Body}}=5.3 \times 10^{17} \text{ cm}^{-3}$, $8.1 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ for the $(11\bar{2}0)$ device with $N_{\text{Body}}=8.3 \times 10^{17} \text{ cm}^{-3}$, and $5.7 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ for the $(1\bar{1}00)$ device with $N_{\text{Body}}=4.4 \times 10^{17} \text{ cm}^{-3}$. The

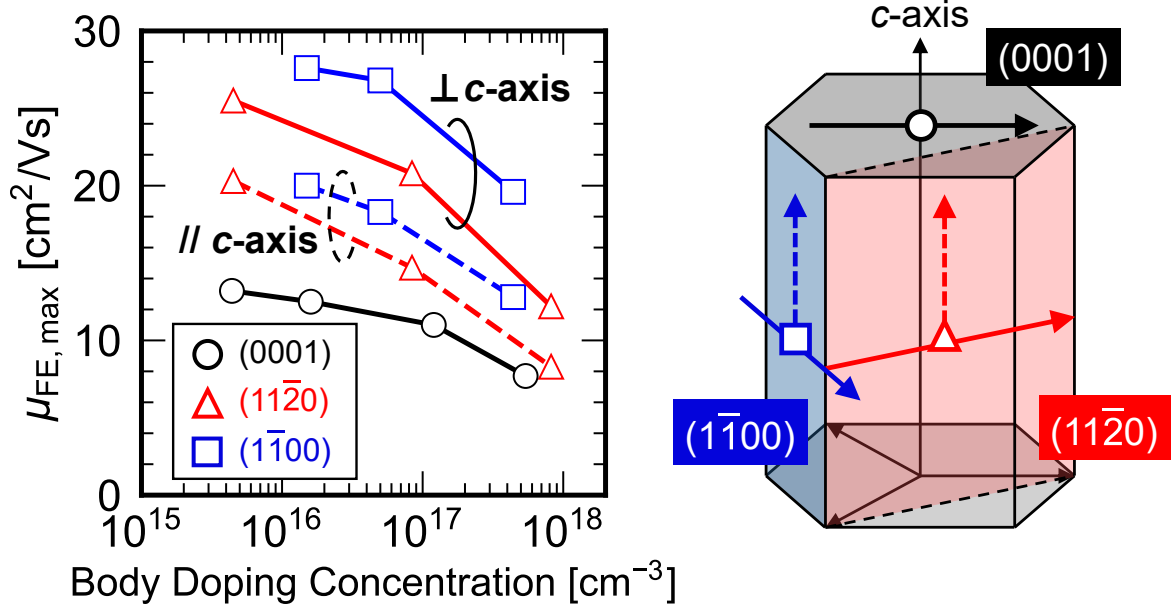


Figure 4.3: Dependence of maximum field-effect mobility ($\mu_{FE,max}$) on donor concentration of n-body for the SiC p-channel MOSFETs fabricated on ($1\bar{1}00$) and ($11\bar{2}0$) with the channel directions perpendicular and parallel to the c -axis. (©IEEE. Partially reproduced with permission from K. Mikami *et. al.*, *IEEE Electron Device Lett.* **45**, 1113 (2024). All rights reserved.)

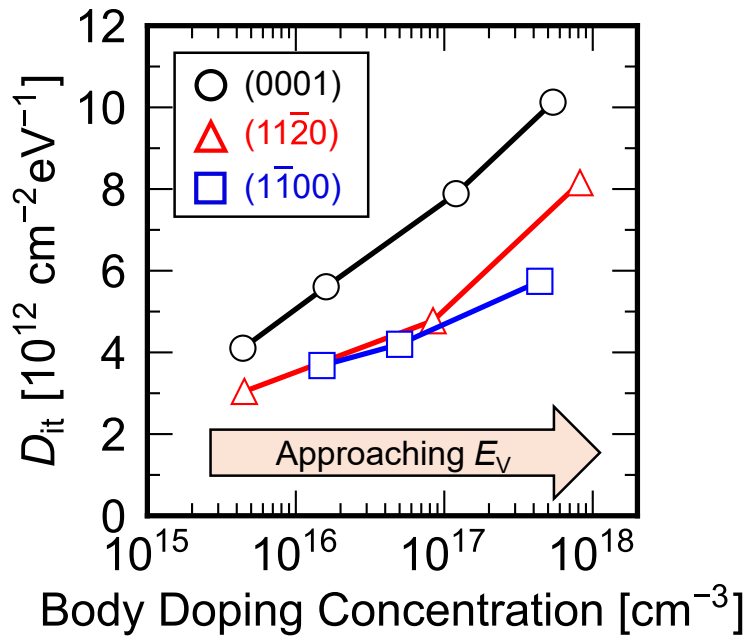


Figure 4.4: Interface state density (D_{it}) near the valence band edge extracted from the subthreshold swing of the SiC p-channel MOSFETs fabricated on (0001), ($11\bar{2}0$), and ($1\bar{1}00$). A higher body doping concentration corresponds to an energy level of D_{it} closer to the valence band edge. (©IEEE. Partially reproduced with permission from K. Mikami *et. al.*, *IEEE Electron Device Lett.* **45**, 1113 (2024). All rights reserved.)

lowest D_{it} was observed in the $(1\bar{1}00)$ device, followed in order by the $(11\bar{2}0)$ and (0001) devices. Therefore, the origin of the crystal-face dependence of $\mu_{FE,max}$ can primarily be attributed to the crystal-face dependence of the interface state density near the valence band edge.

4.4.2 Channel Direction Dependence

This subsection discusses the phenomenon (2), the anisotropy of p-channel mobility on $(11\bar{2}0)$ and $(1\bar{1}00)$, is discussed. The observed anisotropy in field-effect mobility, measured in two MOSFETs with different channel directions on the same chip, is likely attributed to the anisotropy of drift mobility in the inversion layer. In general, the drift mobility (μ_{drift}) is expressed by:

$$\mu_{drift} = \frac{q\langle\tau\rangle}{m^*} \quad (4.1)$$

Here, q is the elementary charge, $\langle\tau\rangle$ is the averaged momentum relaxation time, and m^* is the effective mass of carriers. Although both $\langle\tau\rangle$ and m^* could have the anisotropy, the m^* anisotropy is considered in this study because the anisotropy of hole mobility in bulk SiC can mainly explained by the m^* anisotropy [29]. Note that the effective mass calculated by the second derivatives of the E - k dispersion is the effective mass in the bulk (not in the inversion layer).

The effective mass in the inversion layer (m_{inv}^*) is calculated by a weighted average of the conductive effective mass where weighted values are the hole concentrations in heavy hole (HH), light hole (LH), and crystal-field split-off hole (CH) bands, which is given by:

$$m_{inv,x}^* = \frac{\sum_j p_j}{\sum_j p_j / m_{x,j}^*} \quad (4.2)$$

Here, x is the channel direction perpendicular ($\perp$) or parallel ($//$) to the c -axis, and j corresponds to the HH, LH, and CH bands. p is the hole concentration taking into account of quantum confinement effects in the inversion layer. $m_{x,j}^*$ is the effective mass of holes along the x direction (conductive effective mass) in the j band, summarized in Table 4.1, which was obtained by the second derivatives of the E - k dispersion in Ref. [30]. The hole concentrations in the HH, LH, and CH bands were calculated by the following equation [31]:

$$p_j = \sum_i \int_{-\infty}^{\varepsilon_{i,j}} D_{2D,j} \{1 - f_{FD}(E)\} dE \quad (4.3)$$

Here, $D_{2D,j}$ is the two-dimensional density of states in the j band and $f_{FD}(E)$ is the Fermi-Dirac function. $\varepsilon_{i,j}$ is the energy level of the i -th subband in the j band obtained. In this study, the first, second, and third subbands are considered for the calculation. The $D_{2D,j}$ is expressed as follows [31]:

$$D_{2D,j} = \frac{m_{xy,j}^*}{\pi \hbar^2} \quad (4.4)$$

Table 4.1: Effective mass of heavy hole (HH), light hole (LH), and crystal-field split-off hole (CH) perpendicular and parallel to the c -axis, which were obtained by the second derivatives of the E - k dispersion in Ref. [30].

Direction	Effective mass [m_0]		
	HH	LH	CH
Parallel to the c -axis ($//$)	1.7	1.5	0.21
Perpendicular to the c -axis ($\perp$)	1.5	0.37	1.5

Here $\hbar$ is the reduced Planck constant and $m_{xy,j}^*$ is the density-of-states effective mass in the j band, where y is the direction perpendicular to x in the channel planes. On the nonpolar faces, the $m_{xy,j}^*$ can be calculated by $\sqrt{m_{\perp,j}^* m_{\parallel,j}^*}$. The subband shift from the band edge ($\Delta\varepsilon_{i,j}$) is given by the following equation [31]:

$$\Delta\varepsilon_{i,j} = c_i \left[\frac{(qF\hbar)^2}{2m_{z,j}^*} \right]^{1/3} \quad (4.5)$$

$$c_i = \left[\frac{3}{2}\pi \left(i - \frac{1}{4} \right) \right]^{2/3} \quad (4.6)$$

Here, F is the surface electric field and $m_{z,j}^*$ is the confinement-direction (z) effective mass in the j band. The surface electric field was calculated assuming a triangular-shaped potential in the inversion layer. For the device with $N_D = 1.5 \times 10^{16} \text{ cm}^{-3}$ ($F = 0.13 \text{ MV/cm}$), the ratio of hole concentration is $\sim 90\%$ in the HH band, $\sim 10\%$ in the LH band, and less than 1% in the CH band, indicating that the influence of the CH band is almost negligible. The smallest hole concentration in the CH band can be explained by the split-off band located at 60 meV higher energy level from the valence band maxima [32]. The significant difference in the hole concentration between the HH and LH bands is due to the smaller confinement-direction effective mass of the LH band ($0.37m_0$, m_0 : free electron mass), which causes the energy level of the LH subband higher than that of the HH subband. For example, the energy level of the first subband is 0.037 eV from E_V for the HH band and 0.059 eV from E_V for the LH band. The calculated m_{inv}^* perpendicular ($m_{\text{inv},\perp}^*$) and parallel ($m_{\text{inv},\parallel}^*$) to the c -axis are $1.0m_0$ and $1.3m_0$, respectively.

Figure 4.5 depicts the μ_{FE} perpendicular ($\mu_{\text{FE},\perp}$) and parallel ($\mu_{\text{FE},\parallel}$) to the c -axis for the $(11\bar{2}0)$ device with $N_{\text{Body}} = 4.5 \times 10^{15} \text{ cm}^{-3}$ and $(1\bar{1}00)$ device with $N_{\text{Body}} = 1.5 \times 10^{16} \text{ cm}^{-3}$. The mobility ratio of $\mu_{\text{FE},\perp}/\mu_{\text{FE},\parallel}$ is also shown in Fig. 4.5, with values ranging from 1.1 to 1.3 for the $(11\bar{2}0)$ device and 1.3 to 1.5 for the $(1\bar{1}00)$ device. Here, if the momentum relaxation time is the same in two different channel directions, the field-effect mobility and effective mass in the inversion layer have the following relation because mobility is inversely proportional to effective mass:

$$\frac{\mu_{\text{FE},\perp}}{\mu_{\text{FE},\parallel}} = \frac{m_{\text{inv},\parallel}^*}{m_{\text{inv},\perp}^*} \quad (4.7)$$

Thus, the $\mu_{\text{FE},\perp}/\mu_{\text{FE},\parallel}$ ratio for both devices is almost comparable to the $m_{\text{inv},\parallel}^*/m_{\text{inv},\perp}^*$ ratio of 1.3, indicating that the anisotropy of channel mobility is mainly caused by the m_{inv}^* anisotropy. Note that the assumption of a triangular-shaped potential is valid in subthreshold regions. The slight discrepancy between the $\mu_{\text{FE},\perp}/\mu_{\text{FE},\parallel}$ ratio and $m_{\text{inv},\parallel}^*/m_{\text{inv},\perp}^*$ ratio may originate from the fact that the assumption is not valid in the strong inversion region. Therefore, the surface electric field should be obtained by the self-consistent calculation of the Poisson and Schrödinger equations [33] to reproduce the mobility anisotropy accurately. In addition, the momentum relaxation time could be anisotropic, which should be considered in the future.

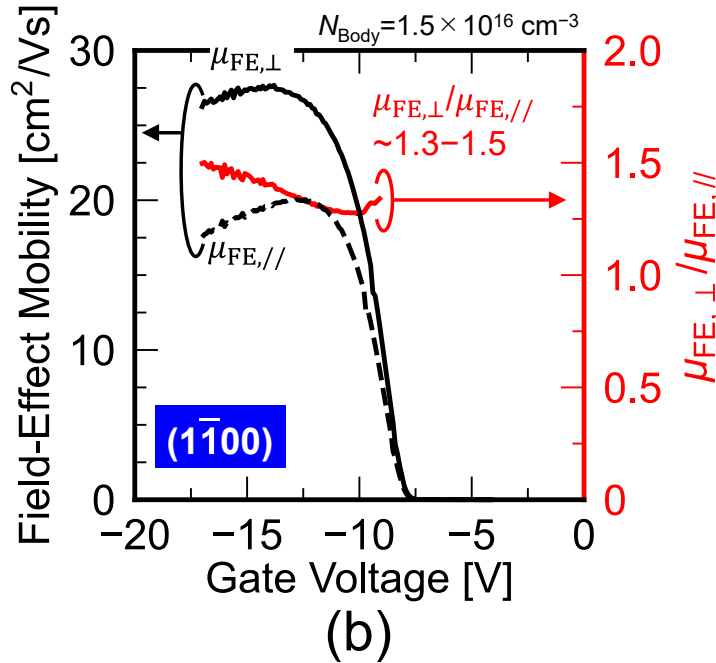
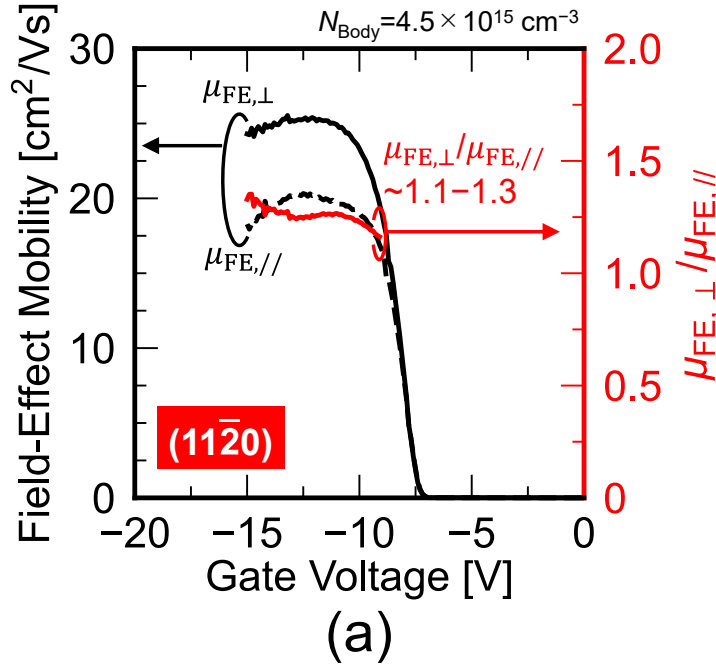


Figure 4.5: Field-effect mobility perpendicular ($\mu_{\text{FE},\perp}$) and parallel ($\mu_{\text{FE},\parallel}$) to the c -axis and mobility ratio ($\mu_{\text{FE},\perp}/\mu_{\text{FE},\parallel}$) as a function of the gate voltage for the (a) ($11\bar{2}0$) and (b) ($1\bar{1}00$) p-channel MOSFETs. (©IEEE. Partially reproduced with permission from K. Mikami *et. al.*, *IEEE Electron Device Lett.* **45**, 1113 (2024). All rights reserved.)

4.4.3 Body Doping Dependence

Regarding the phenomenon (3), the body doping dependence of $\mu_{\text{FE,max}}$ on the nonpolar-face devices is examined using the body biasing technique in the same manner as the (0001) MOSFETs in Section 3.5. Figure 4.6 shows the field-effect mobility as a function of the effective normal field (E_{eff}) for the nonpolar-face p-channel MOSFETs. The solid lines and symbols represent the field-effect mobility without body biasing and with the appropriate body biasing, respectively. The μ_{FE} for lightly-doped MOSFETs with body biasing is comparable to that for heavily-doped MOSFETs without body biasing applied at a given E_{eff} . Thus, the mobility drop with increasing N_{Body} originates from scattering due to E_{eff} , which is the same result as the (0001) devices. To discuss the difference in the mobility drop (scattering mechanisms) between (0001), (11 $\bar{2}$ 0), and (1 $\bar{1}$ 00) p-channel MOSFETs, further investigation through MOS-Hall effect measurements is required. In addition to the scattering mechanisms, it can be suggested that the D_{it} near E_{V} is independent of the body doping concentration not only for the (0001) but also for the (11 $\bar{2}$ 0) and (1 $\bar{1}$ 00) devices.

4.5 Comparison Between N- and P-Channel Mobility on (0001), (11 $\bar{2}$ 0), and (1 $\bar{1}$ 00)

Figure 4.7 shows the comparison of channel mobility perpendicular to the c -axis normalized by the bulk mobility ($\mu_{\text{FE},\perp,\text{max}}/\mu_{\text{bulk},\perp}$) between n- and p-channel SiC MOSFETs on (0001), (11 $\bar{2}$ 0), and (1 $\bar{1}$ 00). The gate oxide of n-channel MOSFETs was formed by the same process (oxidation and NO annealing) as that of the p-channel MOSFETs. The $\mu_{\text{bulk},\perp}$ values used in this study were 1020 cm²/Vs [34] for electrons (n-channel) and 95 cm²/Vs [32] for holes (p-channel). The $\mu_{\text{FE},\perp,\text{max}}/\mu_{\text{bulk},\perp}$ ratio for the p-channel devices is significantly higher than that for the n-channel devices on a given crystal face. In particular, the (1 $\bar{1}$ 00) and (11 $\bar{2}$ 0) p-channel devices exhibited $\mu_{\text{FE},\perp,\text{max}}/\mu_{\text{bulk},\perp}$ ratios of 29% and 26%, respectively. Note that the ratio of channel mobility to bulk mobility is about 40% in Si MOSFETs [35]. Thus, the $\mu_{\text{FE},\perp,\text{max}}/\mu_{\text{bulk},\perp}$ ratio of nearly 30% for the p-channel devices on the nonpolar faces is exceptionally high as SiC MOSFETs, but the p-channel mobility must be still affected by the interface states.

4.6 Summary

In this chapter, the author investigated the p-channel mobility in SiC (11 $\bar{2}$ 0) and (1 $\bar{1}$ 00) MOSFETs. The highest p-channel mobility of 31.5 cm²/Vs was achieved by utilizing the (1 $\bar{1}$ 00) with the channel direction perpendicular to the c -axis. Both (11 $\bar{2}$ 0) and (1 $\bar{1}$ 00) MOSFETs exhibited that the mobility perpendicular to the c -axis is 20–50% higher than that parallel to the c -axis, which originates from the anisotropy of the effective mass of

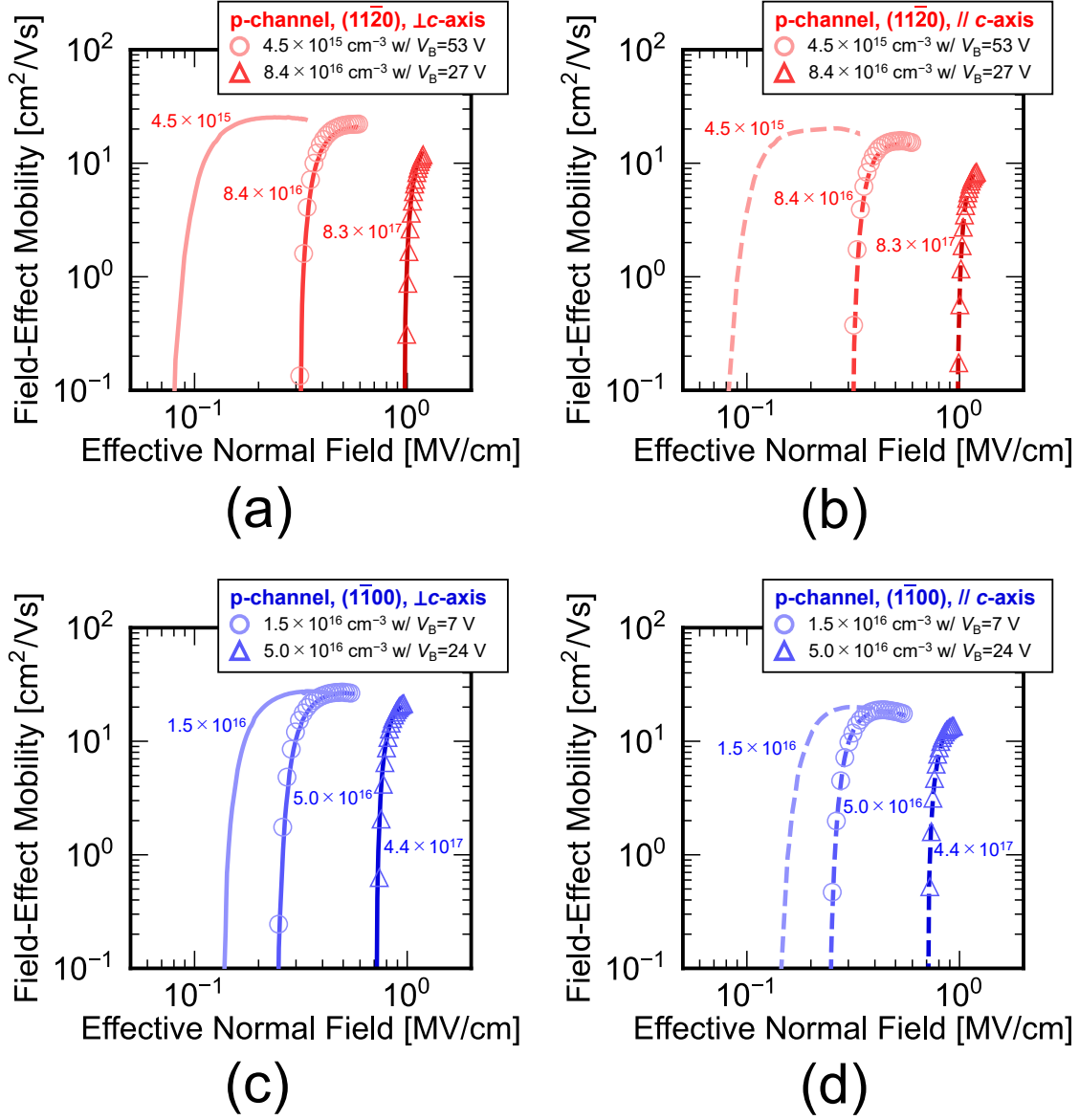


Figure 4.6: Field-effect mobility as a function of the effective normal field for the SiC nonpolar-face MOSFETs with (symbol) and without (line) applied body bias (V_{BS}). Figures (a) and (b) show the ($11\bar{2}0$) p-channel mobility perpendicular and parallel to the c -axis, respectively. Figures (c) and (d) show the ($1\bar{1}00$) p-channel mobility perpendicular and parallel to the c -axis, respectively.

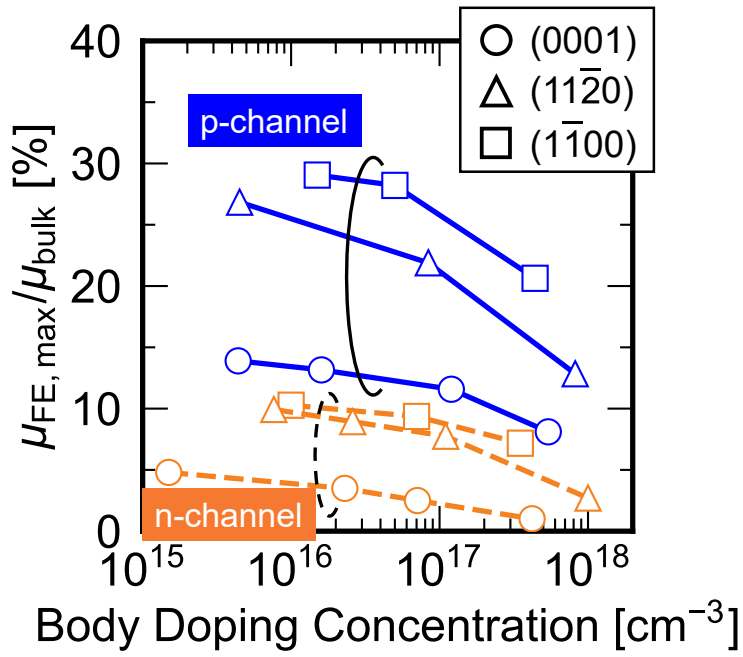


Figure 4.7: Comparison of field-effect mobility perpendicular to the c -axis normalized by bulk mobility ($\mu_{FE, \perp, \max} / \mu_{\text{bulk}, \perp}$) between n- and p-channel SiC MOSFETs on (0001), (11 $\bar{2}$ 0), and (11 $\bar{1}$ 00). The $\mu_{\text{bulk}, \perp}$ used in this study was 1020 cm²/Vs for electrons (n-channel) and 95 cm²/Vs for holes (p-channel). (©IEEE. Partially reproduced with permission from K. Mikami *et. al.*, *IEEE Electron Device Lett.* **45**, 1113 (2024). All rights reserved.)

holes in the inversion layer. Considering the highest mobility achieved in this study, it is preferable to form the sidewalls of FinFETs to be the ($1\bar{1}00$) face and the channel direction to be perpendicular to the c -axis for high-performance SiC CMOS. Such FinFETs can be fabricated using commercially available (0001) wafers.

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Chapter 5

Threshold Voltage and Doping-Dependent Fixed Charges in 4H-SiC MOSFETs

5.1 Introduction

In Chapters 3 and 4, the p-channel mobility in SiC MOSFETs on (0001), (11 $\bar{2}$ 0), and (1 $\bar{1}$ 00) faces with various body doping concentrations was mainly discussed by comparing it with the n-channel mobility. As mentioned in Chapter 1, threshold voltage is as crucial as channel mobility for device modeling and practical applications. Since CMOS devices for high-temperature applications require a large noise margin to prevent operational errors due to thermal noise, the logic threshold voltage must be controlled to be half of the supply voltage ($V_{DD}/2$) whenever possible. This logic threshold voltage can be achieved through drain current balancing and threshold voltage balancing between n- and p-channel MOSFETs. Since the threshold voltage of MOSFETs has a strong impact on the logic threshold voltage, precise control of the threshold voltage is essential for CMOS applications.

The textbook threshold voltage of MOSFETs is given by [1]:

$$V_{th} = \phi_g - \phi_s \pm 2\psi_B \pm \frac{\sqrt{4\varepsilon_s q N_{Body} \psi_B}}{C_{ox}} \quad (5.1)$$

Here, V_{th} is the threshold voltage, ϕ_g is the gate work function, ϕ_s is the semiconductor work function, ψ_B is the bulk potential, ε_s is the permittivity of the semiconductor, q is the elementary charge, N_{Body} is the body doping concentration, and C_{ox} is the gate oxide capacitance per unit area. The plus and minus signs in this equation correspond to the threshold voltage of n- and p-channel MOSFETs, respectively. Since ϕ_s and ϕ_B are almost uniquely determined by the semiconductor material, the threshold voltage is mainly changed by the gate work function, oxide capacitance, and body doping concentration. The threshold voltage of n- and p-channel MOSFETs must be controlled independently and over a wide range for flexible device design.

The gate work function can independently control the threshold voltage by using different materials for n- and p-channel MOSFETs. However, the typical work functions of 4.1 eV for n⁺ poly-Si and 5.2 eV for p⁺ poly-Si [2] allow the gate work function to control the threshold voltage only within a 1 V range. Although the oxide capacitance can widely change the threshold voltage, individual control of threshold voltage is difficult because the gate oxide of n- and p-channel MOSFETs is formed at the same time. In addition to the difficulty in individual control of threshold voltage, a change in the oxide capacitance directly affects device performance such as the mutual conductance and the endurance against short-channel effects. Therefore, threshold voltage control is not performed through the oxide capacitance. On the other hand, the body doping concentration can control the threshold voltage widely and independently because of the wide-range controllability of doping density, where the typical density is 10^{16} – 10^{18} cm⁻³. Furthermore, ion implantation technology allows precise control of threshold voltage. This technique is used in Si CMOS technology, and the body doping dependence of threshold voltage has been investigated [3, 4]. However, the investigation is very limited in SiC MOSFETs. A study of SiC n-channel MOSFETs reported by Ortiz et al. revealed that the threshold voltage for lightly-doped devices is nearly the theoretical value, whereas that for heavily-doped devices is negatively shifted from the theoretical one [5]. They concluded that the threshold voltage shift is caused by the positive oxide fixed charges, of which the density depends on the acceptor concentration of p-body. Since the density of fixed charges is independent of the body doping concentration in Si MOSFETs [6, 7], the fixed charges depending on the body doping concentration could be a unique phenomenon in SiC MOSFETs, and it should be systematically investigated in detail. Moreover, the body doping dependence of threshold voltage and fixed charges has not been studied in SiC p-channel MOSFETs. Therefore, in this chapter, the author investigated the relationship between body doping concentration and threshold voltage in both n- and p-channel SiC MOSFETs.

5.2 Body Doping Dependence of Threshold Voltage

5.2.1 Comparison Between Experimental and Theoretical Threshold Voltages

SiC (0001) n- and p-channel MOSFETs in Chapter 3 were used to investigate the body doping dependence of threshold voltage. The experimental threshold voltage is usually determined by the extrapolated intercept of the linear portion of gate characteristics at low drain voltages [1]. However, in SiC MOSFETs, since the linear portion is hardly observed due to the high density of interface states, it is difficult to obtain an accurate threshold voltage by such determination. Thus, in this study, the experimental threshold voltage was defined as the gate voltage where the total carrier density in the channel region (N_{channel}) is 1×10^{11} cm⁻². The N_{channel} can be obtained by integrating the gate oxide capacitance on

the channel region (C_{GC}) with respect to the gate-source voltage (V_{GS}):

$$N_{\text{channel}} = \frac{1}{qS} \int C_{GC} dV_{GS} \quad (5.2)$$

Here, S is the channel area. The C_{GC} can be obtained through Split C - V measurements, but the capacitance directly obtained by Split C - V measurements (C_{Split}) includes the parasitic capacitances such as the direct overlap (C_{do}), outer fringe (C_{of}), and inner fringe (C_{if}) capacitances [1]. The relationship between C_{Split} and C_{GC} is expressed as follows:

$$C_{\text{Split}} = \begin{cases} C_{\text{do}} + C_{\text{of}} + C_{\text{if}} & (\text{off-state}) \\ C_{GC} + C_{\text{do}} + C_{\text{of}} & (\text{on-state}) \end{cases} \quad (5.3)$$

Since the overlap length was about $5 \mu\text{m}$ for the fabricated MOSFETs, the C_{do} dominates the total overlap capacitance ($C_{\text{do}} + C_{\text{of}} + C_{\text{if}}$), with C_{if} being nearly negligible. Thus, C_{Split} in the off-state can be approximately $C_{\text{do}} + C_{\text{of}}$, and the C_{GC} can be obtained by subtracting $C_{\text{do}} + C_{\text{of}}$ from C_{Split} at the on-state. Figure 5.1 shows the N_{channel} as a function of the gate voltage for the n- and p-channel SiC (0001) MOSFETs. Note that the slope of each data corresponds to the oxide capacitance. The experimental threshold voltage ($V_{\text{th,exp}}$) was defined as the gate voltage where N_{channel} is $1 \times 10^{11} \text{ cm}^{-2}$ indicated by the green broken line in the figure. As the body doping concentration (N_{Body}) increases, the threshold voltage negatively increases in the n-channel MOSFETs and positively increases in the p-channel MOSFETs.

Figure 5.2 depicts the body doping dependence of threshold voltage in the n- and p-channel MOSFETs. The theoretical threshold voltage ($V_{\text{th,theory}}$) was calculated by the following equation:

$$V_{\text{th,theory}} = \phi_{\text{ms}} + \psi_{\text{S,th}} \pm \frac{\sqrt{\pm 2\varepsilon_s q N_{\text{Body}} |\psi_{\text{S,th}} - V_{\text{BS}}|}}{C_{\text{ox}}} \quad (5.4)$$

where ϕ_{ms} is the difference in work function between the gate electrode (Al: 4.1 eV) and semiconductor, $\psi_{\text{S,th}}$ is the surface potential at the threshold voltage, and V_{BS} is a body bias (usually 0 V unless intentionally applied). The plus and minus signs in the equation correspond to the threshold voltage in n- and p-channel MOSFETs. The $\psi_{\text{S,th}}$ can be obtained by solving the following equation self-consistently:

$$N_{\text{free}} = \begin{cases} \frac{1}{q} \int_0^{\psi_{\text{S,th}}} \frac{n_i^2}{p_0} e^{q\psi/kT} \frac{dx}{d\psi} d\psi & (\text{n-channel}) \\ \frac{1}{q} \int_0^{\psi_{\text{S,th}}} \frac{n_i^2}{n_0} e^{-q\psi/kT} \frac{dx}{d\psi} d\psi & (\text{p-channel}) \end{cases} \quad (5.5)$$

Here, N_{free} is the free carrier density in the inversion layer, n_i is the intrinsic carrier density, p_0 is the hole density in the bulk region, n_0 is the electron density in the bulk region, ψ is the surface potential, k is the Boltzmann constant, T is the absolute temperature, and x is

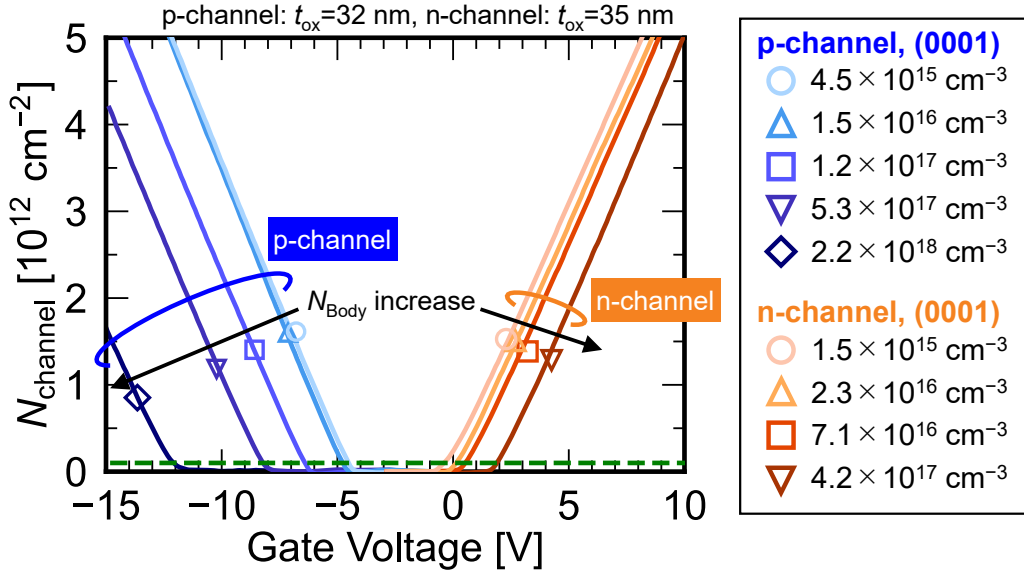


Figure 5.1: Total carrier density in the channel region (N_{channel}) as a function of the gate voltage for the n- and p-channel SiC(0001) MOSFETs. The experimental threshold voltage was defined as the gate voltage where N_{channel} is $1 \times 10^{11} \text{ cm}^{-2}$ (the green broken line in the figure).

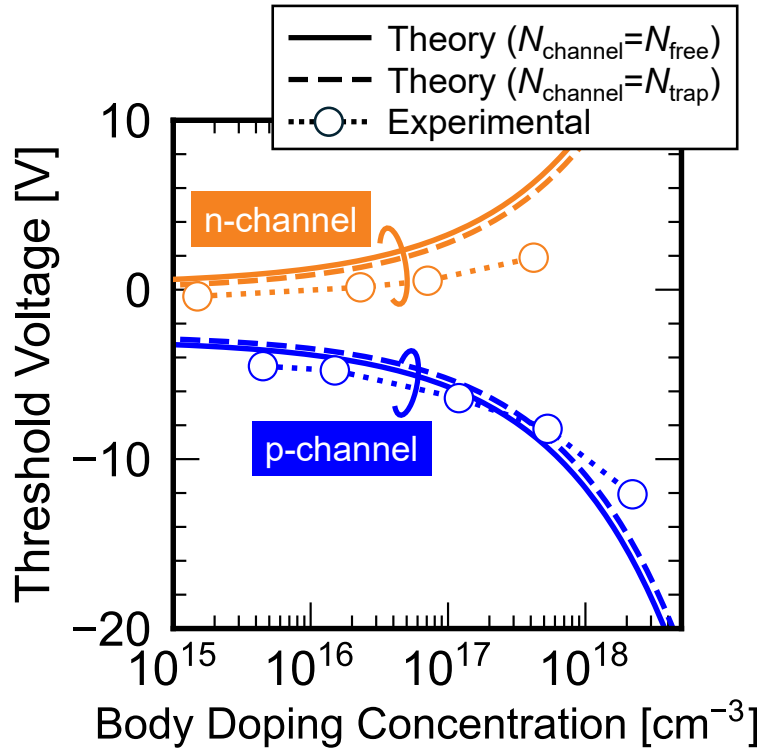


Figure 5.2: Body doping dependence of threshold voltage in the n- and p-channel SiC(0001) MOSFETs.

the distance from the interface ($x = 0$ nm) toward the bulk region. The $V_{\text{th,theory}}$, indicated with the solid line in Fig. 5.2, was calculated by the above equations assuming that the total carrier density of $1 \times 10^{11} \text{ cm}^{-2}$ is the free carrier density ($N_{\text{channel}} = N_{\text{free}}$). Note that the high interface state density (D_{it}) in SiC/SiO₂ structures would fail the assumption. Thus, another $V_{\text{th,theory}}$ was calculated assuming that the total carrier density is the trapped carrier density ($N_{\text{channel}} = N_{\text{trap}}$), as shown with the broken line. In this calculation, $\psi_{\text{S,th}}$ is the surface potential (energy level) at which the trapped carrier density corresponds to $1 \times 10^{11} \text{ cm}^{-2}$. Such surface potential can be obtained by integrating the energy distribution of D_{it} extracted by the C - ψ_{S} method [8–10]. The $V_{\text{th,theory}}$ obtained with the assumption of $N_{\text{channel}} = N_{\text{trap}}$ is almost the same as that obtained with the assumption of $N_{\text{channel}} = N_{\text{free}}$, suggesting that the assumptions in the $V_{\text{th,theory}}$ calculation have a limited influence on the following discussion. Note that the smaller $|V_{\text{th}}|$ obtained with the assumption of $N_{\text{channel}} = N_{\text{trap}}$ originates from the interface states located at deep energy levels (~ 0.3 eV), which can respond to the quasi-static split C - V measurements. From Fig. 5.2, a slightly negative V_{th} shift from the theoretical value was observed in the low N_{Body} region for both devices. In the high N_{Body} region, the n-channel device with $N_{\text{Body}} = 4.4 \times 10^{17} \text{ cm}^{-3}$ showed a positive V_{th} shift of 4.3 V, whereas the p-channel device with $N_{\text{Body}} = 2.2 \times 10^{18} \text{ cm}^{-3}$ showed a negative V_{th} shift of 3.9 V.

5.2.2 Origin of Discrepancy Between Experimental and Theoretical Threshold Voltages

The discrepancy between the experimental and theoretical threshold voltages is caused by the non-ideal charges in MOS structures, such as fixed charges in the gate oxide and electrons/holes trapped at the interface states and in the gate oxide [7, 11], as shown in Fig. 5.3. The density of trapped electrons/holes depends on bias conditions such as gate voltages and measurement temperatures, while the density of the fixed charges does not depend on bias conditions and measurement temperatures, except in cases where additional fixed charges are generated by applying high gate voltages or under high temperature conditions. The total density of these charges (effective fixed charges) can be extracted from the difference between $V_{\text{th,exp}}$ and $V_{\text{th,theory}}$:

$$Q_{\text{eff}} = Q_{\text{fix}} + Q_{\text{trap}} = C_{\text{ox}}(V_{\text{th,theory}} - V_{\text{th,exp}}) \quad (5.6)$$

Here, Q_{eff} is the areal density of effective fixed charges, Q_{fix} is the areal density of fixed charges, and Q_{trap} is the areal density of trapped electrons and holes. Figure 5.4 illustrates the Q_{eff} as a function of the body doping concentration. The Q_{eff} indicated with the solid line was extracted from the threshold voltage shift with the assumption of $N_{\text{channel}} = N_{\text{free}}$, denoted by $Q_{\text{eff}}(V_{\text{th}})$. In the n-channel MOSFETs, $Q_{\text{eff}}(V_{\text{th}})$ positively increases from 6.6×10^{11} to $2.8 \times 10^{12} \text{ cm}^{-2}$ when N_{Body} increases from 1.5×10^{15} to $4.2 \times 10^{17} \text{ cm}^{-3}$. As for the p-channel MOSFETs, $Q_{\text{eff}}(V_{\text{th}})$ negatively increases from 6.6×10^{11} to -2.6×10^{12}

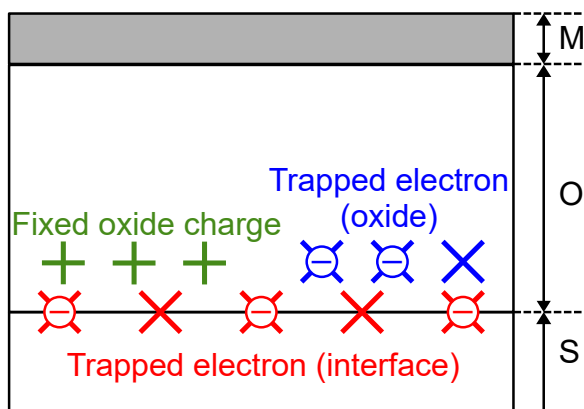


Figure 5.3: Schematic illustration of the non-ideal charges in MOS structures.

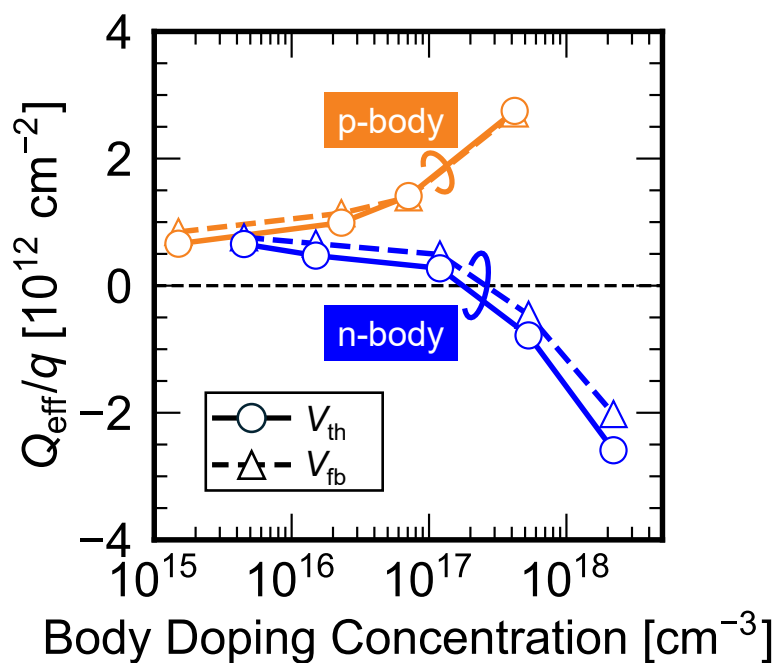


Figure 5.4: Density of effective fixed charges (Q_{eff}) as a function of the body doping concentration. The Q_{eff} with the solid and broken lines were extracted at the threshold voltage (V_{th}) of the MOSFETs and the flatband voltage (V_{fb}) of the MOS capacitors, respectively.

cm^{-2} when N_{Body} increases from 4.5×10^{15} to $2.2 \times 10^{18} \text{ cm}^{-3}$. In order to clarify whether the fixed charges or trapped electrons/holes are dominant in the $Q_{\text{eff}}(V_{\text{th}})$ depending on N_{Body} , Q_{eff} was also extracted from the flatband voltage shift of MOS capacitors on the same chip as the MOSFETs, which is shown with the broken line in Fig. 5.4, denoted by $Q_{\text{eff}}(V_{\text{fb}})$. The $Q_{\text{eff}}(V_{\text{fb}})$ showed a quite similar $Q_{\text{eff}}-N_{\text{Body}}$ relation as $Q_{\text{eff}}(V_{\text{th}})$, suggesting that Q_{fix} dominates Q_{eff} . The reason for this conclusion is as follows. Taking the p-body (n-channel) devices as an example, the surface Fermi levels at the threshold and flatband voltages are located near the conduction and valence band edges, respectively. $Q_{\text{eff}}(V_{\text{th}})$ is the total density of fixed charges and trapped electrons at the interface states, and $Q_{\text{eff}}(V_{\text{fb}})$ is that of fixed charges and trapped holes at the interface states. Thus, the similar values of $Q_{\text{eff}}(V_{\text{th}})$ and $Q_{\text{eff}}(V_{\text{fb}})$ indicate that the Q_{eff} change with increasing N_{Body} is mainly caused by the fixed charges. In other words, the Q_{fix} depends on the body doping (n-/p-type and its density) in SiC/SiO₂ structures. A previous study has also reported a similar Q_{fix} in n-channel SiC MOSFETs: The positive Q_{fix} increases as the p-type body doping increases [5]. It should be noted that Q_{fix} in Si/SiO₂ structures is positive and independent of the body doping concentration [6]. In addition, the origin of fixed charges in Si/SiO₂ structures is the structural defects (ionized silicon) in the oxide layer less than 2.5 nm from Si/SiO₂ interface [7]. Thus, the origin of doping-dependent fixed charges in SiC/SiO₂ structures could be quite different from that in Si/SiO₂ structures.

5.3 Insight into Doping-Dependent Fixed Charges

In this section, the origin of doping-dependent fixed charges is investigated based on the device processes in this study. Epitaxial growth cannot be the origin because the devices with various N_{Body} were formed on the epitaxial layer grown in the same batch. In addition, since source/drain formation and gate electrode formation do not affect the interface, the possible device processes are ion implantation to control the body doping concentration, post-implantation annealing, sacrificial oxidation, oxidation to form gate oxide, NO annealing, and contact annealing.

5.3.1 Influence of Oxidation

It is known that the oxidation of monocrystalline beta-SiC causes dopant redistribution in SiC/SiO₂ structures, thereby incorporating them inside SiO₂ [12]. Figure 5.5 shows the depth profiles of nitrogen, phosphorus, and aluminum densities for SiC samples after dry oxidation at 1300°C for 20 min obtained by secondary ion mass spectrometry (SIMS). The impurity concentrations in the epilayer were $2 \times 10^{19} \text{ cm}^{-3}$ for nitrogen, $2 \times 10^{19} \text{ cm}^{-3}$ for phosphorus, and $4 \times 10^{18} \text{ cm}^{-3}$ for aluminum. Note that the nitrogen and aluminum concentration was controlled during epitaxial growth, while the phosphorus concentration was controlled by ion implantation. Thus, post-implantation annealing and sacrificial oxidation

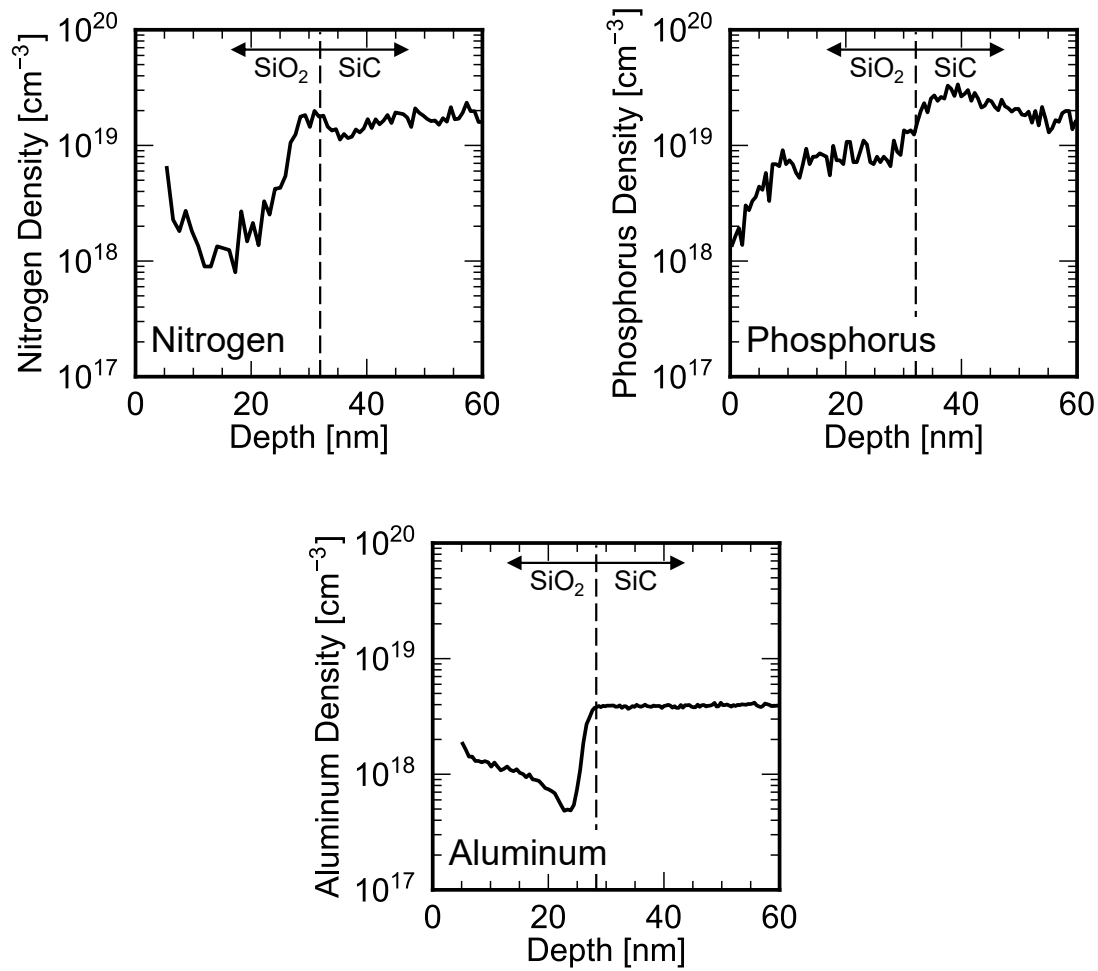


Figure 5.5: Depth profiles of nitrogen, phosphorus, and aluminum densities for the samples after oxidation at 1300°C for 20 min.

were performed for the phosphorus-doped samples. The horizontal axis of depth was obtained by applying the sputtering rate in SiO_2 to the SIMS crater, which does not provide an accurate depth for the SiC region. For the nitrogen-doped sample, the nitrogen density is 1×10^{18} – $2 \times 10^{19} \text{ cm}^{-3}$ in SiO_2 , while it remains almost constant in SiC ($\sim 2 \times 10^{19} \text{ cm}^{-3}$). As for the phosphorus-doped sample, the phosphorus density is about $8 \times 10^{18} \text{ cm}^{-3}$ in SiO_2 , while it remains nearly constant in SiC ($\sim 2 \times 10^{19} \text{ cm}^{-3}$). In the case of the aluminum-doped sample, the aluminum density is 5×10^{17} – $4 \times 10^{18} \text{ cm}^{-3}$ in SiO_2 , while it remains almost constant in SiC ($\sim 4 \times 10^{18} \text{ cm}^{-3}$). Thus, dopant incorporation inside SiO_2 occurs by oxidation of 4H-SiC.

Figure 5.6 shows the Q_{eff} extracted from the flatband voltage shift of the nitrogen-doped MOS capacitors. The gate oxide was formed by dry oxidation at 1300°C for 2, 20, or 30 min, followed by NO annealing at 1250°C for 70 min. The Q_{eff} remains almost constant in the oxide-thickness range of 10 to 40 nm. The obtained Q_{eff} is about $+5 \times 10^{12} \text{ cm}^{-2}$ for the sample with $N_{\text{Body}}=1 \times 10^{16} \text{ cm}^{-3}$ and $-3 \times 10^{12} \text{ cm}^{-2}$ for the sample with $N_{\text{Body}}=2 \times 10^{18} \text{ cm}^{-3}$, respectively. Thus, the incorporated dopants located more than 10 nm away from the interface do not generate doping-dependent fixed charges. In this experiment, it is difficult to determine Q_{eff} accurately for MOS capacitors with a gate oxide thickness of less than 10 nm, particularly for the heavily-doped samples.

To clarify the influence of the incorporated dopants located close to the interface, two kinds of n-type MOS capacitors with different gate oxides were fabricated. The gate oxide was formed by dry oxidation denoted by “Ox-NO” or plasma-enhanced chemical vapor deposition (PECVD) denoted by “CVD-NO”. The oxide thickness was about 30 nm. Note that all processes except for gate oxide formation were the same between both devices and the same condition as mentioned in Section 3.2. Figure 5.7 depicts the Q_{eff} extracted from the flatband voltage shift for the Ox-NO and CVD-NO MOS capacitors. The N_{Body} dependence of Q_{eff} for the CVD-NO samples is similar to that for the Ox-NO samples, suggesting that oxidation itself is not the origin of doping-dependent fixed charges, even though the dopants are incorporated inside SiO_2 by oxidation. The difference in Q_{eff} between the Ox-NO and CVD-NO samples was about $3 \times 10^{11} \text{ cm}^{-2}$ and did not depend on N_{Body} , which may be process-dependent fixed charges.

5.3.2 Influence of Ion Implantation and Post-Implantation Annealing

Ion implantation introduces both extended and point defects in SiC [13–16], and these defects would become doping-dependent fixed charges. To investigate the influence of ion implantation on the fixed charges, n-type MOS capacitors with N_{Body} controlled by ion implantation or epitaxial growth were fabricated. The former samples are denoted by “Impl-CVD-NO” and the latter samples are denoted by “Epi-CVD-NO”. The gate oxide for both samples was formed by PECVD followed by NO annealing at 1250°C for 70 min,

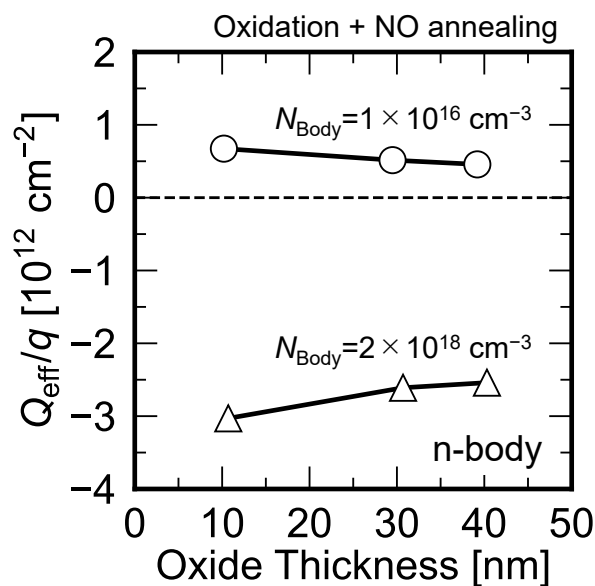


Figure 5.6: Density of effective fixed charges (Q_{eff}) as a function of the equivalent oxide thickness for the n-type MOS capacitors.

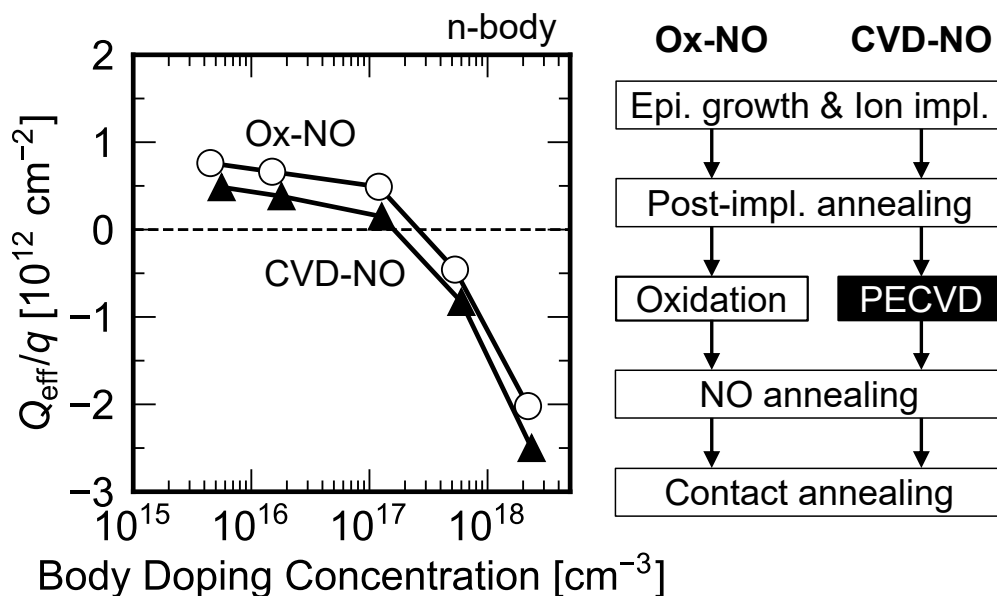


Figure 5.7: Body doping dependence of the density of effective fixed charges (Q_{eff}) for the fabricated n-type MOS capacitors of which gate oxide was formed by oxidation or plasma-enhanced chemical vapor deposition (PECVD).

resulting in an oxide thickness of approximately 30 nm. Here, post-implantation annealing and sacrificial oxidation were not performed for the Epi-CVD-NO sample. The conditions of the other processes were the same as those mentioned in Section 3.2. Figure 5.8 illustrates the Q_{eff} extracted at the flatband voltage for the Impl-CVD-NO and Epi-CVD-NO MOS capacitors. The Q_{eff} for the Epi-CVD-NO samples exactly follows the $Q_{\text{eff}}-N_{\text{Body}}$ relation for the Impl-CVD-NO samples. Thus, ion implantation, post-implantation annealing, and sacrificial oxidation do not contribute doping-dependent fixed charges.

5.3.3 Influence of Post-Oxidation Annealing

To investigate the influence of NO annealing, three kinds of n-type MOS capacitors were fabricated with different conditions of post-oxidation annealing. These include samples without post-oxidation annealing (As-Ox), the samples annealed in NO at 1250°C for 70 min (NO1250), and the samples annealed in NO at 1350°C for 70 min (NO1350). Note that all processes except for the annealing conditions were the same as those mentioned in Section 3.2.

Figure 5.9 shows the Q_{eff} for the fabricated n-type MOS capacitors with different conditions of post-oxidation annealing. The Q_{eff} shift with increasing N_{Body} from $\sim 10^{15}$ to $2 \times 10^{18} \text{ cm}^{-3}$ is $-2.8 \times 10^{12} \text{ cm}^{-2}$ for the NO1250 samples, $-2.7 \times 10^{12} \text{ cm}^{-2}$ for the NO1350 samples, and $-2.6 \times 10^{12} \text{ cm}^{-2}$ for the As-Ox samples. Nearly the same negative Q_{fix} was obtained in the NO-annealed and as-oxidized samples, suggesting that NO annealing temperature and itself do not affect doping-dependent fixed charges. Note that the Q_{eff} for the As-Ox samples shows a positive shift of about $5 \times 10^{11} \text{ cm}^{-2}$ from the NO1250 samples, which may be process-dependent fixed charges.

5.3.4 Influence of Contact Annealing

The Q_{eff} for the fabricated n-type MOS capacitors with and without contact annealing is depicted in Fig. 5.10. The annealing temperature and time were 1000°C and 2 min, respectively. Note that the conditions of other processes were the same as those mentioned in Section 3.2. The Q_{eff} shift with increasing N_{Body} from 5×10^{15} to $2 \times 10^{18} \text{ cm}^{-3}$ is $-2.8 \times 10^{12} \text{ cm}^{-2}$ for the samples with the contact annealing and $-2.6 \times 10^{12} \text{ cm}^{-2}$ for the samples without the contact annealing. Therefore, contact annealing does not appear to be the source of doping-dependent fixed charges. Note that the difference in Q_{eff} between the two devices, of which the density is approximately $7 \times 10^{11} \text{ cm}^{-2}$, may be process-dependent fixed charges.

5.3.5 Discussion

The systematic investigation has revealed that ion implantation, post-implantation annealing, sacrificial oxidation, gate oxide formation, post-oxidation annealing, and contact an-

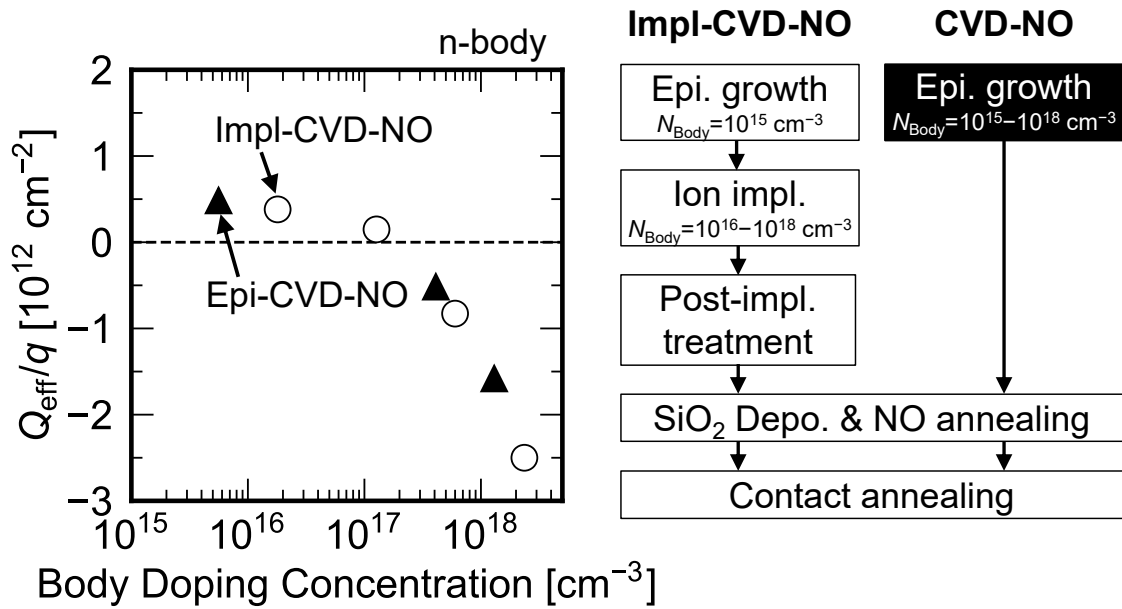


Figure 5.8: Body doping dependence of the density of effective fixed charges (Q_{eff}) for the fabricated n-type MOS capacitors of which body doping concentration was controlled by epitaxial growth or ion implantation.

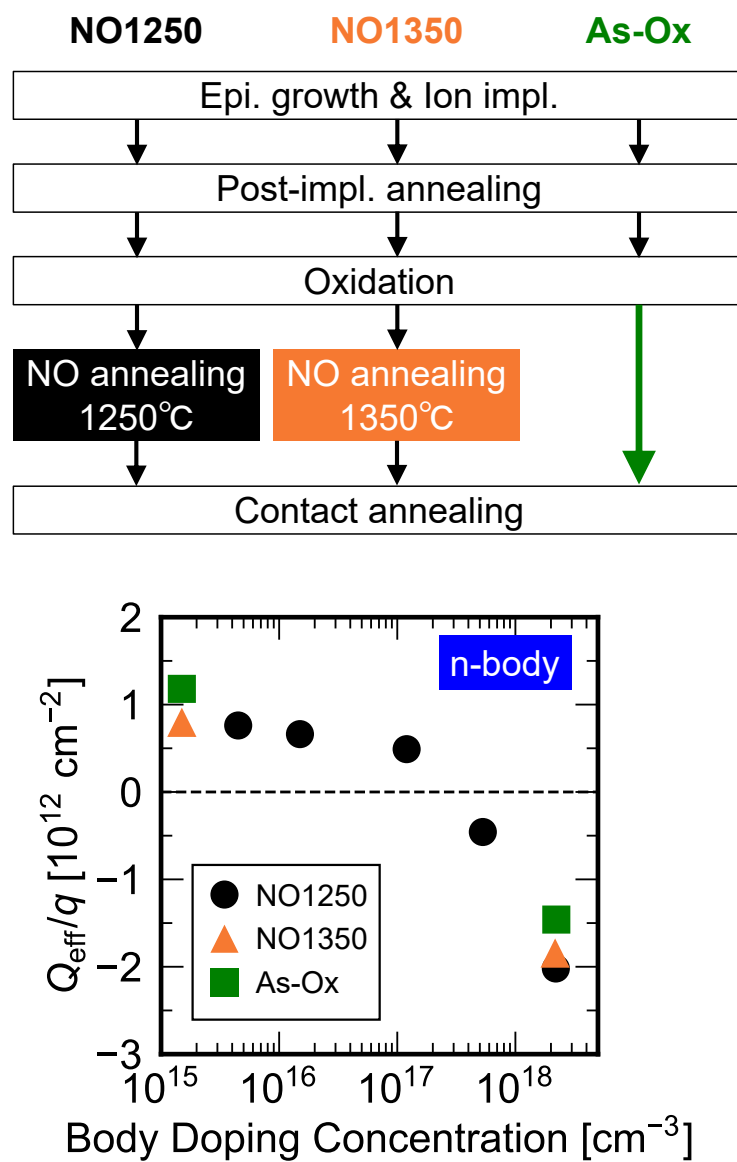


Figure 5.9: Body doping dependence of the density of effective fixed charges (Q_{eff}) for the fabricated n-type MOS capacitors of which gate oxide was formed by oxidation only or oxidation followed by NO annealing.

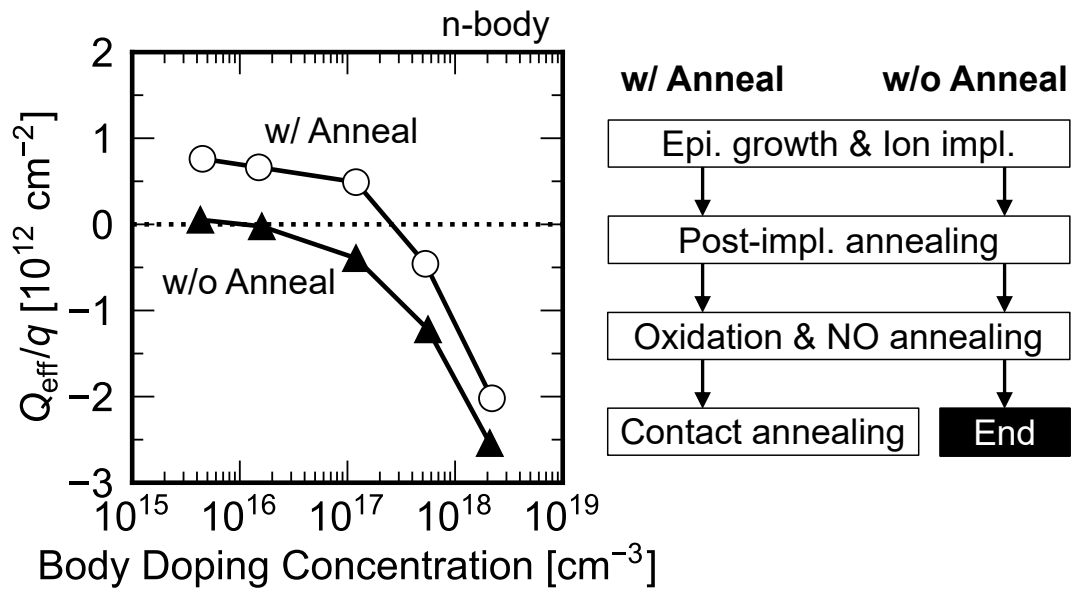


Figure 5.10: Body doping dependence of the density of effective fixed charges (Q_{eff}) for the fabricated n-type MOS capacitors with or without contact annealing.

nealing are not the origin of doping-dependent fixed charges, indicating that other processes not mentioned at the beginning of this section cause the fixed charges. One of the possible process conditions is the cooling down after high-temperature annealing or oxidation. In this study, all samples were cooled down from the annealing/oxidation temperature to 800°C with a cooling rate of 5°C/min in N₂ ambients. This slow cooling may affect the interface properties through unintentional nitridation and thermal reactions. Note that unintentional nitridation is not the origin because similar doping-dependent fixed charges were also observed for the n-type MOS capacitors cooled down in Ar ambients with the same cooling rate. Thus, only thermal reactions during cooling may affect the fixed charges.

In order to investigate the influence of cooling rates, fast cooling was performed after post-oxidation annealing. Due to the cooling rate limitation in our furnace for NO annealing and dry oxidation, the author conducted high-temperature N₂ annealing followed by fast cooling down using a cold-wall furnace. The experimental procedures are as follows. The starting materials were epi-grown ($N_{\text{Body}} \sim 5 \times 10^{15} \text{ cm}^{-3}$) or ion-implanted ($N_{\text{Body}} \sim 2 \times 10^{18} \text{ cm}^{-3}$) n-type epilayers on a SiC (0001) n-type substrate. Post-implantation and sacrificial oxidation were performed only for the ion-implanted samples. The gate oxide was formed by dry oxidation at 1300°C for 20 min, followed by 5°C/min cooling from 1300 to 800°C. Then, the samples were pulled from the oxidation furnace for about 10 min. Next, the samples were loaded into the cold-wall furnace at room temperature and annealed in N₂. Figure 5.11 depicts the N₂ annealing flow for fast and slow cooling. The N₂ flow rate was 0.4 slm from loading to unloading. First, the temperature was elevated from RT to 1400°C in about 3 min. The samples were annealed at 1400°C for 45 min in N₂ ambients, followed by fast or slow cooling. The fast cooling corresponds to a temperature drop from 1400 to 800°C within 1 min (denoted by N₂-600°C/min), while the slow cooling corresponds to a temperature lowering for 120 min with a rate of 5°C/min (denoted by N₂-5°C/min). The temperature lowering from 800°C to RT was performed for 20 min without any heat treatment. Finally, the temperature was lowered from 800°C to RT for 20 min without heating. Contact annealing and electrode formation were the same process described in Chapter 3. Figure 5.12 shows the Q_{eff} for the n-type MOS capacitors with different cooling rates. The Q_{eff} for the NO-annealed samples (NO-5°C/min) is also shown in Fig. 5.14. The vertical axis is the Q_{eff} variation from the Q_{eff} for the lightly-doped samples (ΔQ_{eff}). As for the samples with $N_{\text{Body}} \sim 2 \times 10^{18} \text{ cm}^{-3}$, the N₂-5°C/min cooling sample showed almost the same ΔQ_{eff} as the NO-5°C/min cooling sample, while the N₂-600°C/min cooling sample showed a smaller ΔQ_{eff} than the 5°C/min cooling samples. These results can be interpreted as follows. The 600°C/min cooling samples maintain the final interface formed at 1400°C (annealing temperature) due to the fast cooling. In contrast, the 5°C/min cooling samples have the interface re-formed below 1250°C due to the slow cooling. It should be noted that in Si/SiO₂ structures, the density of fixed charges after oxidation depends on the pulling rate from the oxidation furnace in O₂ ambients [7]. A slower pulling rate allows the samples to be oxidized at temperatures lower than intentional oxidation temperatures, whereas a

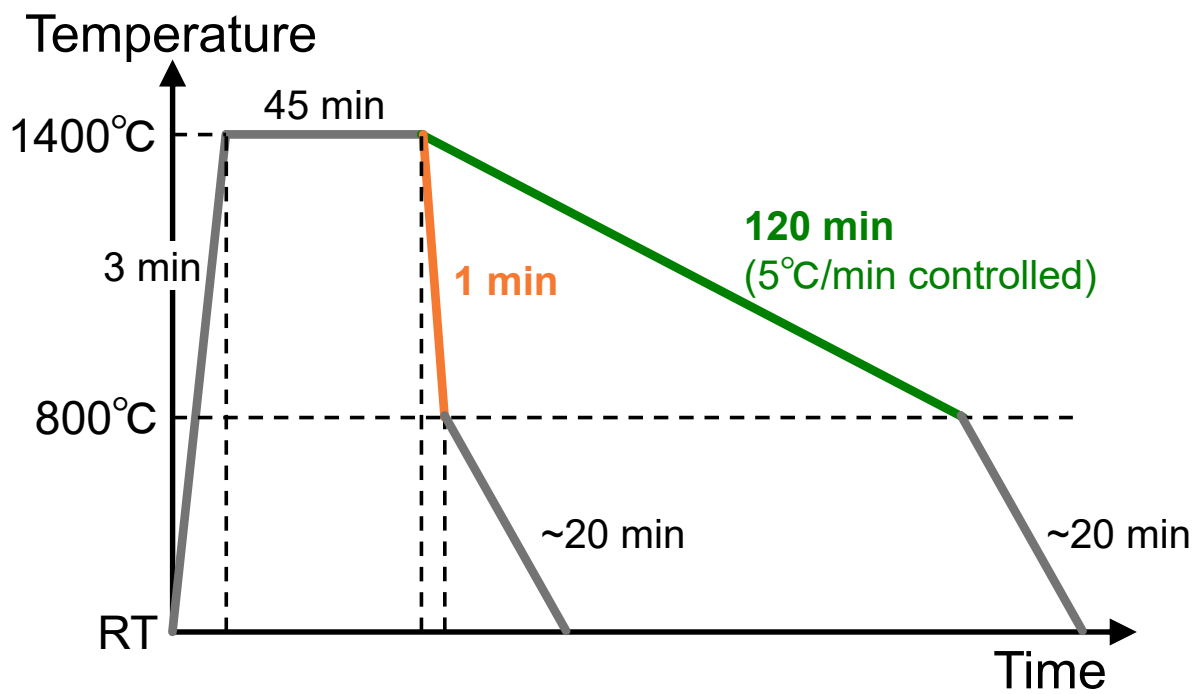


Figure 5.11: N₂ annealing process-flow for fast (orange) and slow (green) cooling. The flow rate of N₂ was 0.4 slm from loading to unloading.

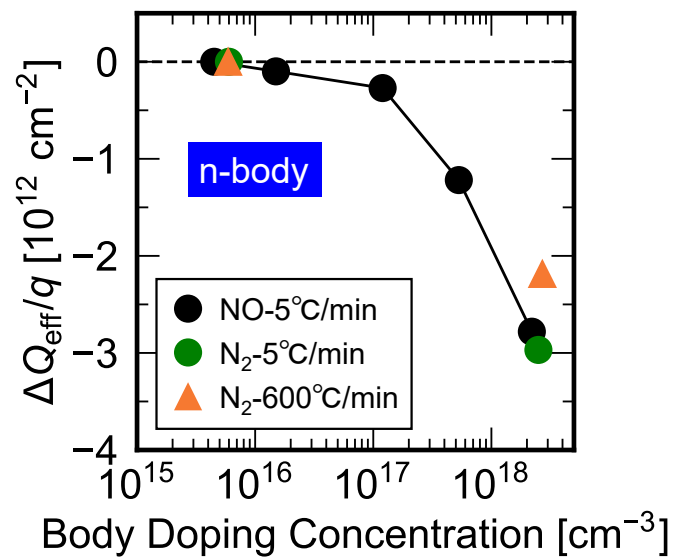
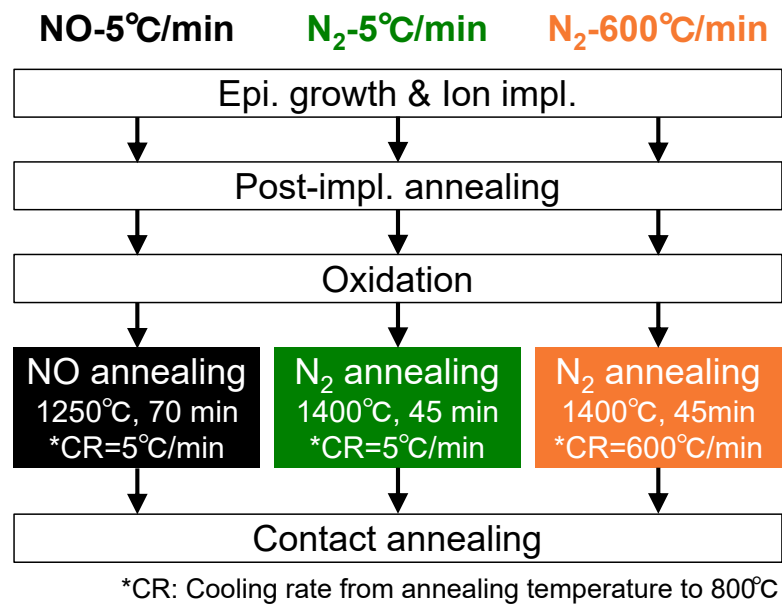


Figure 5.12: Body doping dependence of the density of effective fixed charges (Q_{eff}) for the n-type MOS capacitors with different cooling processes. The vertical axis is the Q_{eff} variation based on Q_{eff} for the lightly-doped samples.

rapid pulling rate results in the samples being oxidized at oxidation temperatures. Although there is a large difference in kinetics between cooling in O_2 (oxidation) and cooling in inert gases, the cooling rate dependence of Q_{eff} suggests that the density of doping-dependent fixed charges also depends on the final annealing temperature. The dependence of Q_{eff} on a final annealing temperature is discussed in the next section.

5.4 Generation Mechanism of Doping-Dependent Fixed Charges

5.4.1 Proposed Model

Based on the various control experiments in the previous section, it is expected that the density of fixed charges depends not only on the body doping concentration but also on the final annealing temperature. Thus, a generation mechanism of doping-dependent fixed charges is proposed based on the Fermi level at a final annealing temperature. Figure 5.13 illustrates the proposed model of fixed charge generation in SiC/SiO₂ structures. Here, the Fermi level (E_F) is a function of the doping concentration and temperature [1]:

$$E_F - E_i = kT \log \left(\frac{N_D}{n_i} \right) \quad (\text{n-type}) \quad (5.7)$$

$$E_i - E_F = kT \log \left(\frac{N_A}{n_i} \right) \quad (\text{p-type}) \quad (5.8)$$

where E_i is the midgap, N_D is the donor density, and N_A is the acceptor density. The intrinsic carrier density strongly depends on the bandgap (E_g) and temperature [1]:

$$n_i = \sqrt{N_C N_V} \exp \left(-\frac{E_g}{2kT} \right) \quad (5.9)$$

Here, N_C and N_V are the effective densities of states in the conduction and valence bands, respectively. Considering the E_g decrease due to the thermal expansion of SiC at high annealing temperatures, E_g is calculated by the semi-empirical equation [17]:

$$E_g = E_{g0} - \frac{\alpha T^2}{T + \beta} \quad (5.10)$$

where E_{g0} is the bandgap at 0 K and α and β are fitting parameters. The E_{g0} , α , and β in 4H-SiC are 3.295 eV, 8.2×10^{-4} eV/K, and 1.8×10^{-3} K, respectively [18]. From the relationship between the Fermi level and body doping concentration in Fig. 5.13, the Fermi level in SiC is located near the midgap for lightly-doped bodies and away from the midgap for heavily-doped bodies due to the wide bandgap of SiC. This may cause a difference in defect formation energy between SiC/SiO₂ structures with different body doping. For example, the Fermi level for heavily-doped n-type SiC is located in the conduction band side, resulting in a smaller formation energy of negatively-charged defects, which can explain

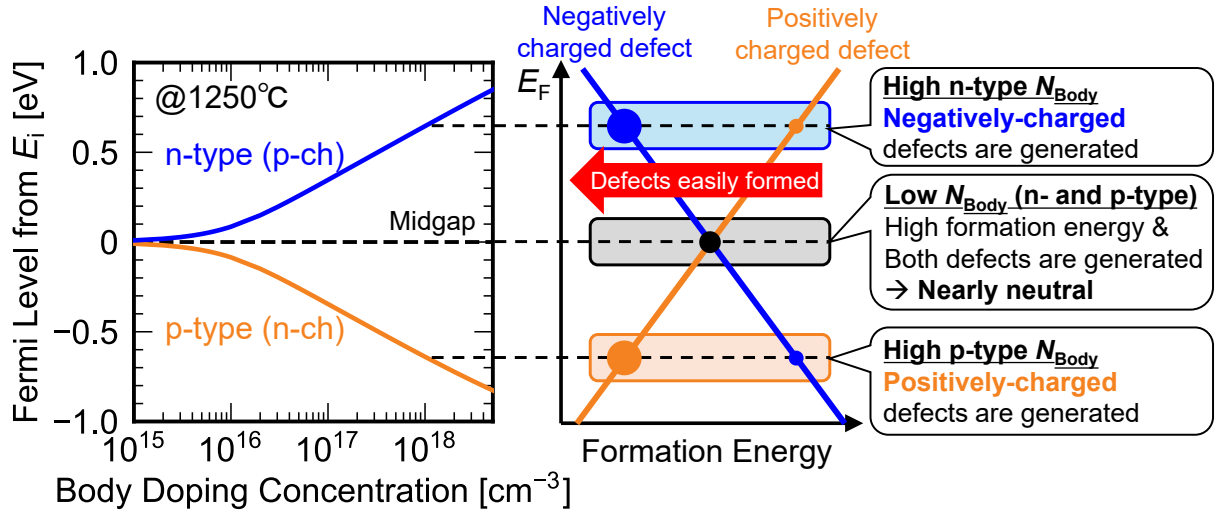


Figure 5.13: Proposed model of fixed charge generation in SiC/SiO₂ structures. Due to the wide bandgap of SiC, the Fermi level in SiC is away from the midgap even at high temperatures, especially in the case of high body doping concentration (N_{Body}).

the increased negative Q_{eff} in the heavily-doped n-bodies (p-channel MOSFETs) as shown in Fig. 5.4. In the same manner, the increased positive Q_{eff} in the heavily-doped p-bodies (n-channel MOSFETs) could be caused by a smaller formation energy of positively-charged defects because the Fermi level is located in the valence band side. Additionally, the same Q_{eff} of $6.6 \times 10^{11} \text{ cm}^{-2}$ for both n- and p-type lightly-doped bodies can be attributed to a higher formation energy of negatively- and positively-charged defects and balancing out by negative and positive fixed charges since the Fermi level is located near the midgap. Note that the Q_{eff} for the lightly-doped samples is a positive value of $6.6 \times 10^{11} \text{ cm}^{-2}$, even though the Fermi level at 1250°C is located near the midgap. Moreover, the p-body samples show a positive Q_{eff} increase of $2.1 \times 10^{12} \text{ cm}^{-2}$ when N_{Body} increases from 1.5×10^{15} to $4.2 \times 10^{17} \text{ cm}^{-3}$, while the n-body samples show a negative Q_{eff} increase of $1.4 \times 10^{12} \text{ cm}^{-2}$ when N_{Body} increases from 4.5×10^{15} to $5.3 \times 10^{17} \text{ cm}^{-3}$. In other words, the body doping dependence for p-body samples is stronger than that for n-body samples. Thus, it is expected that the formation energy of positively-charged defects is lower than that of negatively-charged defects in SiC/SiO₂ structures.

5.4.2 Validity of Proposed Model

The proposed model can explain doping-dependent fixed charges in SiC/SiO₂ structures well. However, further investigation is necessary to verify the Fermi-level-based model. In this section, the validity of the proposed model is examined with respect to different dopant species and final annealing temperature.

5.4.2.1 Influence of Dopant Species

If the Fermi-level-based model is correct, the density of doping-dependent fixed charges should not depend on dopant species. Therefore, the author fabricated the n-type MOS capacitors with either nitrogen- or phosphorus-doped n-type bodies. The nitrogen- and phosphorus-doped bodies were prepared by ion implantation into a lightly-doped n-type epilayer on an n-type substrate. After post-implantation annealing and sacrificial oxidation, the gate oxide was formed by dry oxidation at 1300°C for 20 min, followed by NO annealing at 1250°C for 70 min.

Figure 5.14 depicts the body doping dependence of Q_{eff} for the MOS capacitors with nitrogen- or phosphorus-doped bodies. Although Q_{eff} for the phosphorus-doped samples is slightly lower than that for the nitrogen-doped samples at a given N_{Body} , the increase in negative Q_{eff} with increasing N_{Body} for the phosphorus-doped samples is comparable to that for the nitrogen-doped samples. This result supports the Fermi-level-based model and suggests that the origin of doping-dependent fixed charges is intrinsic defects.

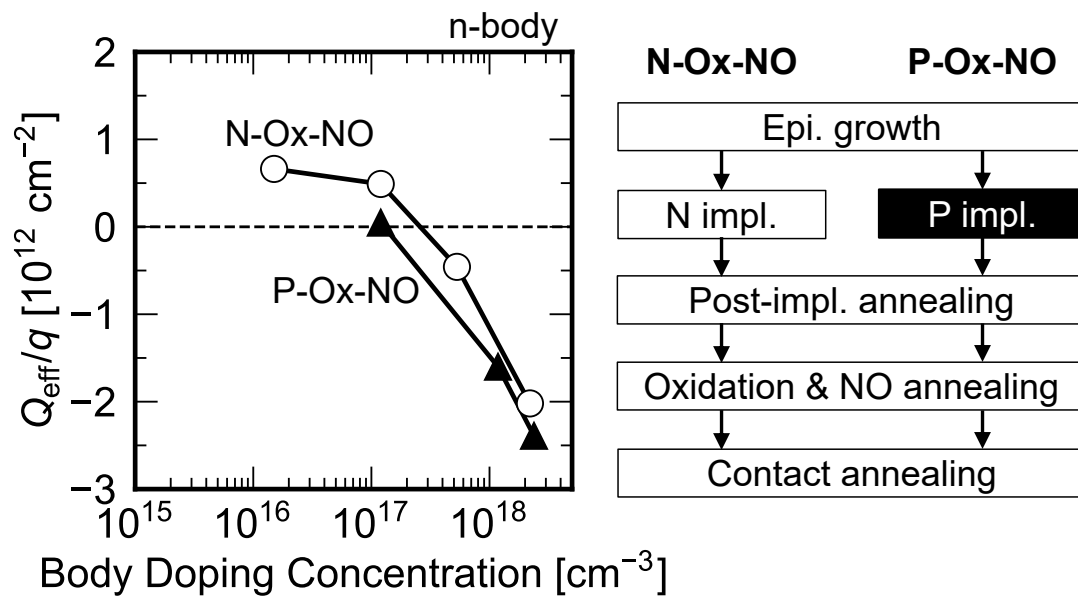


Figure 5.14: Body doping dependence of the density of effective fixed charges (Q_{eff}) for the fabricated n-type MOS capacitors of which body impurities are nitrogen or phosphorus.

5.4.2.2 Final Annealing Temperature Dependence

Since the density of fixed charges is expected to depend on the final annealing temperature, as discussed in the previous section, the dependence of Q_{eff} on the final annealing temperature is investigated. Lightly-doped and heavily-doped n-type epilayers on an n-type SiC (0001) substrate were prepared. The doping concentration was $1 \times 10^{16} \text{ cm}^{-3}$ by epitaxial growth for the lightly-doped samples and $2 \times 10^{18} \text{ cm}^{-3}$ by ion implantation for the heavily-doped samples. Post-implantation and sacrificial oxidation were conducted only for the ion-implanted samples. The gate oxide was formed by dry oxidation at 1300°C for 20 min. Post-oxidation annealing was performed in a cold-wall furnace for fast cooling. The annealing ambient, temperature, and time were N_2 , 1600°C , and 1 min, respectively. Subsequently, the annealed samples were immediately cooled down to 800°C within 1 min and RT in about 20 min. Some of the 1600°C -annealed samples were re-annealed at a lower temperature of 800, 1000, or 1200°C , followed by fast cooling. The annealing time is 3 hours at 800°C , 1 hour at 1000°C , and 1 hour at 1200°C . The gate and backside electrodes were Al.

Figure 5.15 (a) depicts the dependence of Q_{eff} on the final annealing temperature for the fabricated n-type MOS capacitors. The Q_{eff} for both lightly- and heavily-doped samples varies with the final annealing temperature. As the final annealing temperature changes from 800 to 1600°C , the obtained Q_{eff} changes $+4.6 \times 10^{11} \text{ cm}^{-2}$ (from $+5.0 \times 10^{11}$ to $+9.6 \times 10^{11} \text{ cm}^{-2}$) for the lightly-doped samples and $+1.1 \times 10^{12} \text{ cm}^{-2}$ (from -2.3×10^{12} to $-1.2 \times 10^{12} \text{ cm}^{-2}$) for the heavily-doped samples. Both samples showed a positive Q_{eff} increase, but the Q_{eff} variation was larger for the heavily-doped samples compared to the lightly-doped samples.

Figure 5.15 (b) illustrates the Q_{eff} plotted against the Fermi level relative to the midgap at the final annealing temperature. The black and blue lines are the Q_{eff} for the lightly- and heavily-doped samples. At a given $E_F - E_i$ such as 0.5 eV, there is a Q_{eff} difference between the lightly- and heavily-doped samples, suggesting that the Fermi level alone does not uniquely determine the density of doping-dependent fixed charges. One of the possible reasons for this phenomenon is the difference in defect formation energy. Even at the same Fermi level for the lightly- and heavily-doped samples, the final annealing temperature for the heavily-doped samples is much higher than that for the lightly-doped samples, which may lead to a lower formation energy of negatively-charged defects in the heavily-doped samples. Therefore, the density of doping-dependent fixed charges would be predicted by the Fermi-level-based model considering the temperature dependence of defect formation energy. Here, the red line in Fig. 5.15 (b) is the Q_{eff} for the $5^\circ\text{C}/\text{min}$ slow-cooling samples with different N_{Body} of which the final annealing temperature was assumed to be 1000°C . This assumption is plausible because the $5^\circ\text{C}/\text{min}$ slow-cooling samples were finally annealed at 1000°C for contact annealing. The fast and slow cooling samples showed a similar Q_{eff} for a given set of body doping concentrations (1×10^{16} or $2 \times 10^{18} \text{ cm}^{-3}$) and final annealing

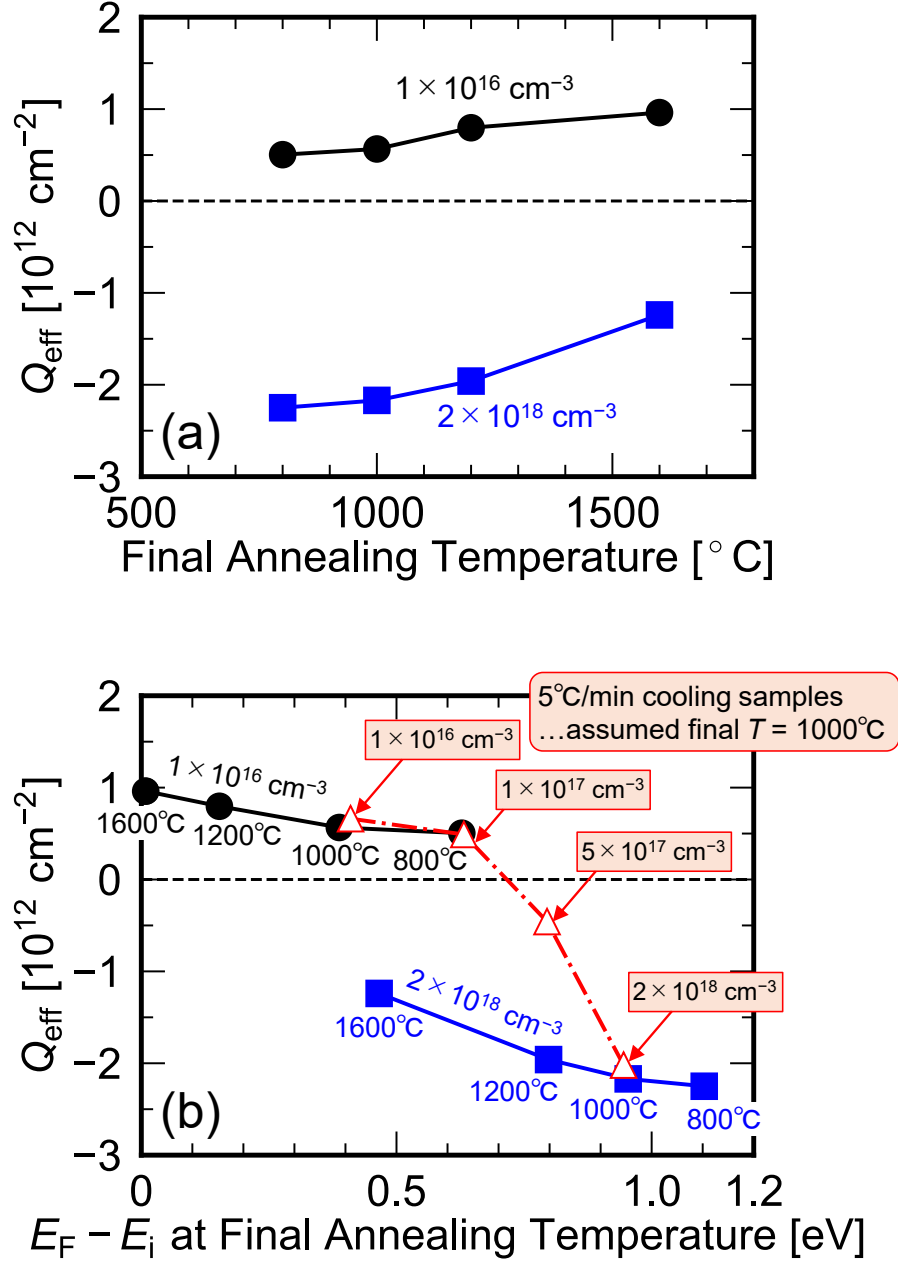


Figure 5.15: (a) Dependence of the density of effective fixed charges (Q_{eff}) on the final annealing temperature and (b) on the Fermi level from the midgap ($E_F - E_i$) at the final annealing temperature for the fabricated n-type MOS capacitors. The black and blue lines are the Q_{eff} for the lightly- ($1 \times 10^{16} \text{ cm}^{-3}$) and heavily-doped ($2 \times 10^{18} \text{ cm}^{-3}$) samples. The red line is the Q_{eff} for the 5 $^{\circ}\text{C}/\text{min}$ slow-cooling samples with different body doping concentrations (1×10^{16} , 1×10^{17} , 5×10^{17} , and $2 \times 10^{18} \text{ cm}^{-3}$) assuming their final annealing temperature was 1000 $^{\circ}\text{C}$.

temperature (1000°C). Therefore, the final annealing conditions strongly affect the density of fixed charges. It is important to note that the conclusion in Section 5.3.4, stating that contact annealing is not the source of doping-dependent fixed charges, is incorrect.

5.5 Summary

In this chapter, the author investigated the body doping dependence of threshold voltage in both n-channel and p-channel SiC MOSFETs. It was found that the difference between the experimental and theoretical threshold voltages depends on the body doping (its density and n-/p-type). The threshold voltage shift is mainly caused by doping-dependent fixed charges, which have not been previously reported in Si/SiO₂ structures. As the body doping increases, positive fixed charges increase for the p-body (n-channel) devices, whereas negative fixed charges increase for the n-body (p-channel) devices. Based on various control experiments, it was revealed that the density of the fixed charges strongly depends not only on the body doping concentration but also on the final annealing temperature. The author has proposed a model of fixed charge generation based on the Fermi level at a final annealing temperature. It can be concluded that doping-dependent fixed charges should be carefully treated to control the threshold voltage precisely in SiC MOSFETs.

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Chapter 6

Conclusions

6.1 Conclusions

In this thesis, the author investigated the interface states in SiC/SiO₂ structures and the body doping dependence of channel mobility and threshold voltage in 4H-SiC MOSFETs, mainly focusing on the p-channel MOSFETs, towards realization of SiC CMOS integrated circuits. The main conclusions obtained in this study are summarized as follows.

In Chapter 2, the interface states whose energy levels are near the valence band edge were investigated by three methods, the high-low, $C-\psi_s$, and conductance methods. The $C-\psi_s$ and conductance methods revealed that the interface state density near the valence band edge exponentially increases towards the band edge. Specifically, the density rises to $3.9 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$, which is almost the same as that near the conduction band edge. The interface states located close to the valence band edge are likely donor-type states, which can be expected from the capture cross section obtained by the conductance method. In addition, the conductance method revealed that the standard deviation of surface potential fluctuation (σ) is significantly small for the valence band side (a few meV), whereas the conduction band side has a larger σ of about 100 meV.

In Chapter 3, the body doping dependence of p-channel mobility on SiC (0001) was investigated. Considering the difference between electron ($1020 \text{ cm}^2/\text{Vs}$) and hole mobility ($95 \text{ cm}^2/\text{Vs}$) in bulk SiC, the normalized p-channel mobility (13%) is about twice as high as the normalized n-channel mobility (5%). This phenomenon originates from the less carrier trapping at the interface states in the p-channel MOSFETs because the larger effective mass of holes brings weak quantum-confinement effects. In the high effective-normal-field (E_{eff}) regions, it was found that the p-channel mobility slightly decreases with increasing E_{eff} , while the n-channel mobility sharply drops. The analysis using body biasing technique indicated that the different mobility drop between the n- and p-channel MOSFETs is caused by the difference in dominant scattering mechanisms. The possible scattering mechanisms are surface-roughness scattering, Coulomb scattering due to trapped carriers, and scattering caused by the surface potential fluctuation, which would be strong in the

n-channel MOSFETs but weak in the p-channel MOSFETs.

In Chapter 4, the mobility in p-channel MOSFETs on SiC (11 $\bar{2}$ 0) and (1 $\bar{1}$ 00) was investigated towards SiC-FinFET-based circuits. The highest mobility ever reported for SiC p-channel MOSFETs (28–31 cm²/Vs) was achieved on (1 $\bar{1}$ 00). The crystal-face dependence of p-channel mobility, which is the highest on (1 $\bar{1}$ 00) followed by (11 $\bar{2}$ 0) and (0001), can be explained by the lower interface state density on the nonpolar faces. The nonpolar-face p-channel MOSFETs showed anisotropic mobility: The mobility perpendicular to the *c*-axis is higher than that parallel to the *c*-axis. The anisotropic mobility is mainly caused by the anisotropy of the effective mass of holes in the inversion layer, which was revealed by the calculation of the effective mass taking account of three different holes (heavy, light, crystal-field split-off holes) in 4H-SiC and quantum confinement effects in the inversion layer. Based on these results, the author has proposed the FinFET structure with (1 $\bar{1}$ 00) sidewalls and channel direction perpendicular to the *c*-axis for high-performance SiC CMOS devices.

In Chapter 5, the author investigated the body doping dependence of threshold voltage in both n- and p-channel SiC MOSFETs. The difference between the experimental and theoretical threshold voltages, particularly large in heavily-doped MOSFETs, is caused by doping-dependent fixed charges that have not been reported in Si/SiO₂ structures. When the body doping increases, the density of fixed charges increases negatively for the n-body (p-channel) devices and positively for the p-body (n-channel) devices. Based on various control experiments, the author proposed a model of fixed charge generation based on the Fermi level at a final annealing temperature.

6.2 Future Outlook

The author conducted several studies towards establishing a physics-based device model of both n- and p-channel SiC MOSFETs. Although the fundamental knowledge was obtained, several issues still remain for SiC CMOS applications, and one new research subject became clear through this study.

1. Elucidation of hole transport properties in SiC p-channel MOSFETs

The author focused on channel mobility (field-effect mobility) to discuss the mobility in SiC p-channel MOSFETs because of its simple characterization. However, channel mobility includes carrier trapping effects and is not a true drift mobility of carriers. Since the drift mobility is essential to establish a device model of MOSFETs, the drift mobility of holes in SiC p-channel MOSFETs should be investigated by MOS-Hall effect measurements, which can directly extract drift mobility (strictly speaking, Hall mobility), as in the case of the n-channel MOSFETs [1–3]. In addition, a combination of MOS-Hall effect and Split *C*–*V* measurements [4] should be conducted to obtain the interface state density located at energy levels shallower than those in this study,

and the influence of Coulomb scattering due to trapped holes on the drift mobility should be clarified quantitatively.

2. Reduction of doping-dependent fixed charges in SiC/SiO₂ structures

The density of doping-dependent fixed charges in SiC/SiO₂ structures reaches a high density of 10^{12} cm^{-2} for the heavily-doped samples and 10^{11} cm^{-2} even for the lightly-doped samples. In Si/SiO₂ structures, the density of fixed charges is less than 10^{11} cm^{-2} [5], and the appropriate oxidation and annealing results in an extremely low fixed charge density of $2 \times 10^{10} \text{ cm}^{-2}$ [6]. Such a high density of fixed charges in SiC/SiO₂ structures would cause significant degradation of drift mobility. Thus, reduction of doping-dependent fixed charges is a critical issue to maximize the potential of SiC MOSFETs for power and high-temperature applications. One of the possible methods is low-temperature processes from oxide formation to the end of the device process because the results obtained in this study implied that high-temperature processes intrinsically generate doping-dependent fixed charges in SiC/SiO₂ structures.

3. Determination of physical factors limiting high-temperature operation of SiC CMOS devices

So far, it has been demonstrated that SiC CMOS devices operate at high temperatures of 300–532°C [7–9], but the maximum and stable operating temperature has not been clarified. Even though the gate leakage current through the oxide layer and the operation of parasitic pn diodes are the possible factors limiting the high-temperature operation, their influence has not been investigated based on semiconductor physics. Therefore, it is necessary to clarify the limiting factors of the high-temperature operation of SiC CMOS devices fabricated by the current process, and by feeding back the results, the maximum and stable operating temperature should be determined.

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List of Publications

A. Full Length Papers and Letters

1. K. Mikami, K. Tachiki, K. Ito, and T. Kimoto,
“Body doping dependence of field-effect mobility in both n- and p-channel 4H-SiC metal-oxide-semiconductor field-effect transistors with nitrided gate oxides,”
Applied Physics Express **15**, 036503 (2022).
2. K. Tachiki, K. Mikami, K. Ito, M. Kaneko, and T. Kimoto,
“Mobility enhancement in heavily doped 4H-SiC (0001) (11 $\bar{2}$ 0), and (1 $\bar{1}$ 00) MOSFETs via an oxidation-minimizing process,”
Applied Physics Express **15**, 071001 (2022).
[Featured as an Spotlight 2022]
3. X. Chi, K. Tachiki, K. Mikami, M. Kaneko, and T. Kimoto,
“Different temperature dependence of mobility in n- and p-channel 4H-SiC MOSFETs,”
Japanese Journal of Applied Physics **62**, 110906 (2023).
4. K. Mikami, K. Tachiki, M. Kaneko, and T. Kimoto,
“Insight Into Mobility Improvement by the Oxidation-Minimizing Process in SiC MOSFETs,”
IEEE Transactions on Electron Devices **71**, 931 (2024).
5. K. Mikami, M. Kaneko, and T. Kimoto,
“High-mobility 4H-SiC p-channel MOSFETs on nonpolar faces,”
IEEE Electron Device Letters **45**, 1113 (2024).
[Featured as an Editor’s Pick & the cover of the July 2024 issue]
6. K. Mikami, M. Kaneko, and T. Kimoto,
“Doping-dependent fixed charges near SiC/SiO₂ interface,”
in preparation.

7. K. Mikami, M. Kaneko, and T. Kimoto,
 “Characterization of interface state density near the valence band edge in nitrated 4H-SiC/SiO₂ structures by conductance method,”
 in preparation.

B. Conference Proceedings

1. T. Kimoto, M. Kaneko, K. Tachiki, K. Ito, K. Mikami, H. Fujii, A. Inoue, and N. Maeda
 “An Overview of SiC High-Voltage Power Devices and High-Temperature ICs,”
Proc. of 2024 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (2024), pp. 88-94.

C. International Conferences

1. K. Mikami, K. Ito, K. Tachiki, and T. Kimoto,
 “Channel mobility of NO- and N₂-annealed 4H-SiC(0001) p-channel MOSFETs with various donor concentrations of n-body,”
European Conference on Silicon Carbide and Related Materials 2020–2021, Tours (France)/Virtual, Oct. 2021, Oral, Tu-1B-01.
2. K. Mikami, K. Tachiki, K. Ito, and T. Kimoto,
 “Body doping dependence of channel mobility in both n- and p-channel 4H-SiC MOSFETs,”
International Symposium on Creation of Advanced Photonic and Electronic Devices 2022, Kyoto (Japan), Mar. 2022, Poster, P-69.
3. T. Kimoto, K. Tachiki, K. Ito, K. Mikami, M. Kaneko, M. Horita, and J. Suda,
 “High Mobility in SiC MOSFETs with Heavily-Doped p-Bodies” (invited),
14th Topical Workshop on Heterostructure Microelectronics, Hiroshima (Japan), Aug. 2022, Oral, 2-2.
4. K. Mikami, K. Tachiki, M. Kaneko, and T. Kimoto,
 “High-quality MOS interface on 4H-SiC(11 $\bar{2}$ 0) formed by the oxidation-minimizing process,”
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10th Asia-Pacific Workshop on Widegap Semiconductors, Taoyuan (Taiwan)/Virtual,
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9. K. Mikami and T. Kimoto,
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10. T. Kimoto, K. Tachiki, K. Mikami, and M. Kaneko,
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11. X. Chi, K. Tachiki, K. Mikami, M. Kaneko, and T. Kimoto,
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13. S. Tshimitsu, K. Mikami, K. Tachiki, M. Kaneko, and T. Kimoto,
 “SiC n-channel MOSFETs fabricated on a high-purity semi-insulating substrate,”
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14. T. Kimoto, K. Tachiki, K. Mikami, X. Chi, and M. Kaneko,
 “Physics and Performance Improvement of SiC MOSFETs” (invited),
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16. M. Kaneko, K. Tachiki, K. Mikami, and T. Kimoto,
 “Mobility enhancement in SiC n- and p-channel MOSFETs” (invited),
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17. K. Mikami, M. Kaneko, and T. Kimoto,
 “Doping-dependent fixed charges in SiC MOSFETs” (invited),
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18. R. Ito, A. Inoue, K. Mikami, M. Kaneko, and T. Kimoto,
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19. T. Kimoto, R. Ishikawa, X. Chi, K. Mikami, K. Tachiki, and M. Kaneko,
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20. T. Kimoto, M. Kaneko, K. Tachiki, K. Ito, K. Mikami, H. Fujii, A. Inoue, R. Ito, and
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