KYOTO UNIVERSITY

DEVELOPMENT OF $In_xGa_{1-x}As$–BASED OHMIC CONTACTS TO n–TYPE GaAs PREPARED BY RF–SPUTTERING

A dissertation submitted

in

partial satisfaction of the requirements

for

the degree of Doctor of Engineering

by

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To My Parents

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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ABSTRACT OF THE DISSERTATION

DEVELOPMENT OF $In_xGa_{1-x}As$–BASED OHMIC CONTACTS TO n–TYPE GaAs PREPARED BY RF–SPUTTERING

by

C. Uchibori

With increasing the integration level of the very large scale integrated (VLSI) GaAs devices, low contact resistance and excellent thermal stability of the Ohmic contacts become the main issues to improve the device performance and reliability. The contact resistance is determined with the depletion with at the contact metal /GaAs interface, which limits the current flow through the interface. One of the effective methods to fabricate the low Ohmic contact to the n-type GaAs is formation of an InGaAs layer between the contact metal and the GaAs substrate, which provides low energy barrier at the metal/GaAs interface. In order to reduce the contact resistance of the InGaAs–based Ohmic contacts, a large area of the GaAs surface should be covered by the epitaxially grown InGaAs layer with graded In composition.

In this study, by extending the results of the microstructural and the electrical analyses of the previously developed InAs/Ni/W contact, the new InGaAs–based Ohmic contacts to n-type GaAs, which provide low contact resistance, excellent thermal stability and excellent reprodcibility, have been successfully developed.

In order to grow the InGaAs layers epitaxially on the GaAs substrate, an addition of Ni to the InAs/W contact was found to be essential. Ni broke the compositional stoichiometry of the InAs layer and enhanced the interfacial reaction between the InAs layer and the GaAs substrate, resulting in reduction of the contact resistances. Although the InAs/Ni/W contact provided the contact resistance of 0.4 Ωmm after annealing at 750 °C and the excellent thermal stability at 400 °C for 10 h, the surface morphology was rough and the reproducibility of the contact was poor.

The results of the microstructural analysis of the InAs/Ni/W contact suggested

that the suppression of the In out–diffusion was necessary to improve the surface morphology and the reproducibility. In addition, by comparing the temperature dependence of the measured contact resistances and that of the simulated values, total area of the InGaAs/GaAs interface should be increased to reduce the contact resistance.

One of the effective methods to suppress the In out–diffusion was the reduction of the contact formation temperature. Since $In_{0.7}Ga_{0.3}As$ was expected to react with GaAs at the temperature lower than that of the InAs–GaAs reaction, $In_{0.7}Ga_{0.3}As$ instead of InAs was deposited. The surface morphology of the $In_{0.7}Ga_{0.3}As/Ni/W$ contact was smooth, because the formation temperature was reduced to 600 °C. However, reproducibility of the low resistance Ohmic contacts was still poor, because the olarge amounts of the In atoms diffused to the W surface.

In order to suppress the In out–diffusion and to control the In composition in the InGaAs layer, a WN diffusion barrier was introduced in the $In_{0.7}Ga_{0.3}As/Ni/W$ contact. The reproducibility of the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contact was excellent and the surface morphology was smooth. In addition, the contact resistance was reduced to 0.1 Ωmm, which is believed to be due to the large total area of the InGaAs/GaAs interface. Since the contact resistance and the thermal stability were not deteriorated even after depositing an Al overlayer, the contact formation process of this contact is believed to be compatible with the current Si device technology.

1. Outline

In this section, Ohmic contacts in the GaAs devices are briefly introduced and the outline of the following sections is described. For the semiconductor devices, the most extensively used material is Silicon (Si). However, Si is not suitable for the microwave application and the photonic application. Gallium arsenide (GaAs) is one of the best candidates for the microwave devices and the photonic devices, because it has an electron mobility higher than that of the Si and has a wide energy bandgap with a direct band structure. These devices need contact metals to inject an external electrical current into the active GaAs layers. As a result, the metal/semiconductor interfaces are formed. When the current flows through the interfaces, a voltage drop is measured as a contact resistance. With shrinking the device dimensions of the GaAs microwave devices to improve the device performance, the effects of the contact resistances on the device performance become large. In addition, the light emitting efficiency of the GaAs photonic devices is reduced by the high contact resistance. Therefore, development of the Ohmic contacts, which have a negligibly small contact resistances at the metal/GaAs interface compared with that of the active GaAs layer in the device is necessary to improve the GaAs devices.

In Sec. 2, three carrier transport mechanisms through the interface were explained based on the energy band diagrams at the metal/n–GaAs interface. Since the doping level in the n–GaAs and the barrier height at the metal/n–GaAs interface determine the carrier transport mechanism, the equations of the contact resistances for the three mechanisms are functions of the doping level and the barrier height. These equations indicate that the increasement of the doping level and/or the reduction of the barrier height are effective to reduce the contact resistance. Based on these theories, various in–situ and annealed Ohmic contacts have been developed. These previously developed contacts are reviewed in this section.

In Sec. 3, based on the previously developed annealed Ohmic contacts, develop-

ment of new Ohmic contacts to n-type GaAs was challenged. In this study, reduction of the contact resistance was challenged by growing an intermediate layer with low energy barrier between the contact metal and the GaAs substrate. An $In_xGa_{1-x}As$ was the best candidate for the intermediate layer for the n–type GaAs, because the energy barrier at the metal/$In_xGa_{1-x}As$ interface is lower than that of the metal/n–GaAs interface and the lattice mismatch between the GaAs and the $In_xGa_{1-x}As$ is smaller than 7%. The Ohmic contacts, which have extremely low contact resistances were previously developed by depositing a compositionally graded $In_xGa_{1-x}As$ layer by using the Molecular Beam Epitaxy (MBE) technique. However, from a manufacturing process view point, this technique is not suitable for mass production. In this study, development of $In_xGa_{1-x}As$–based Ohmic contacts were carried out by using the radio frequency (rf) sputtering technique. The rf sputtering technique is suitable for mass production of the electrode materials and allows us to deposit various materials such as refractory metals, composite materials, and semiconductor materials.

In Sec. 3. 1, details of the formation mechanism of the previously developed InAs/Ni/W contacts were investigated. In order to understand the effects of the Ni atoms on the formation mechanism, formation mechanisms of the InAs–Ni–W contacts with different deposition sequences were studied. The first Ni layer was found to diffuse deeply into the GaAs substrate and formed large amounts of a NiAs phases after annealing, leading to reduction of the area contacting the $In_xGa_{1-x}As/GaAs$ interface. As a result, a high energy potential barrier was formed at the metal/GaAs interface and the contact resistance (R_c) was high. The Ni atoms in the second Ni layer broke the compositional stoichiometry of the InAs layer and enhanced the interfacial reaction between InAs and GaAs. After high temperature annealing, a large area of the GaAs surface was covered by the epitaxially grown $In_xGa_{1-x}As$ layer. In addition, the In composition x in the $In_xGa_{1-x}As$ layer was about 1.0 at the metal/$In_xGa_{1-x}As$ interface and about 0.5 at the $In_xGa_{1-x}As/GaAs$ interface. The InAs/Ni/W contact provided the low contact resistance (R_c) and excellent thermal stability. However, the surface of the

contacts was rough and the reproducibility was poor. These deterioration was found to be due to the In out diffusion to the W layer.

In addition to the investigation of the formation mechanism, the current transport mechanism of the InAs/Ni/W contacts was investigated. The R_c values of the contacts at the various temperatures were measured and compared with the calculated values, which determined the carrier transport mechanism to be a thermionic field emission and the effective barrier height to be about 0.13 eV. Since the low contact resistance was measured when the In composition x at the metal /$In_xGa_{1-x}As$ interface was 1.0 and 0.5 at the $In_xGa_{1-x}As$/GaAs interface, the measured barrier height would represent a barrier formed due to about 4% lattice mismatch between the $In_xGa_{1-x}As$ and the GaAs.

In Sec. 3. 2, the formation temperature was reduced to prevent the In out diffusion to the W layer. By depositing the $In_{0.7}Ga_{0.3}As$ layer instead of the InAs layer, the formation temperature of the $In_{0.7}Ga_{0.3}As$/Ni/W contacts was reduced, resulting in the smooth surface. However, the R_c values were not changed. In order to produce the low R_c, the In concentration x in the $In_xGa_{1-x}As$ should be higher than 0.7 at the metal/$In_xGa_{1-x}As$ interface and should be lower than 0.5 at the $In_xGa_{1-x}As$/GaAs interface.

In Sec. 3. 3, improvement of the surface morphology and the reproducibility of the $In_xGa_{1-x}As$–based contacts were achieved by developing the $In_{0.7}Ga_{0.3}As$/Ni /W_2N/W contacts. The W_2N layer was expected to prevent the In out diffusion and increase the area contacting the $In_xGa_{1-x}As$/GaAs interface, resulting in reduction of the R_c values. The lowest R_c value of this contacts was by a factor of three smaller than that of the InAs/Ni/W contacts. The low R_c values were found to be due to formation of the large total area of the $In_xGa_{1-x}As$/GaAs interface.

In Sec. 4, the R_c values of the $In_xGa_{1-x}As$–based contacts with the wiring metals were investigated, because the Ohmic contacts are contacted with the wiring metals in the actual devices. The lowest R_c values and the thermal stability of the $In_{0.7}Ga_{0.3}As$

/Ni/W_2N/W contact during 400 °C annealing was not deteriorated with an Al overlayer. Therefore, this contact is compatible with an Al wiring process, which is extensively used in the Si device technology. However, Cu atoms were found to deteriorate the electrical properties of this contacts. This contact is not compatible with Cu wiring process.

The last section described the conclusion of this thesis.

2. Background of the thesis

2.1 Introduction

Since 1947, when the bipolar transistor was invented at Bell Laboratory, the field of the semiconductor devices has been rapidly grown. The semiconductor devices are mainly fabricated by using silicon (Si). Demands for these devices are the reduction of the processing time, the rapid data transformation, and the application to the opto-electronics. Increase of the processing speed has been achieved by shrinking the device dimension and by increasing the integration level of the Si devices. However, further improvement will not be expected without using other semiconductors which have higher electron mobilities than that of Si. In addition, when the device dimension shrinks down to that of the quantum dots, the semiconductors which can grow the heterostructure easily should be used. In order to transfer the data rapidly, the transformation techniques using a microwave or photon have been developed. For the microwave applications, the materials which have high electron mobilities should be used. For the photonic application, the materials which have direct band structures are useful.

Gallium arsenide (GaAs) is one of the best candidates for the high speed switching devices, the microwave devices and the photonic devices, because it has an electron mobility higher than that of Si and a direct band structure. (These electrical properties are summarized in Table 2. I.) For the microwave application, high electron mobility transistor (HEMT) and metal semiconductor field–effect transistor (MESFET) have been developed. The schematic illustration of the GaAs MESFET is shown in Fig. 2. 1. In order to inject a current into the device, contact metals are fabricated on the semiconductor and the metal/semiconductor interfaces are formed. When the current flows through these interfaces, a voltage drop is measured as a contact resistance. (The details of the current transport mechanism at these interface will be described in the

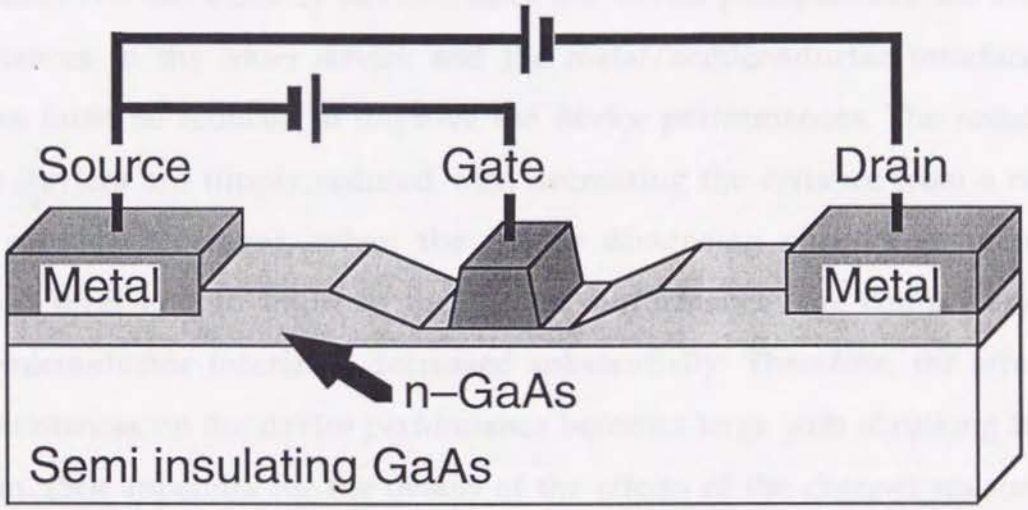

Fig. 2. 1 Schematic illustration of the GaAs MESFET.

Table 2. I Electrical properties of Si and GaAs.

	Si	GaAs
Bandgap (300K) (eV)	1.12	1.42
Electron mobility (300K) (cm^2/V–s)	1500	8500
Band structure	Indirect	Direct
Heterostructure	Difficult	Easy

next section.) For the MESFET devices, since the device performances are affected by the resistances in the inner device and the metal/semiconductor interfaces, these resistances must be reduced to improve the device performances. The resistances in the inner devices are simply reduced with decreasing the distance from a contact to another contact. However, when the device dimension shrinks to increase the integration level and to improve the device performance, the contact area of the metal/semiconductor interfaces decreased substantially. Therefore, the effect of the contact resistances on the device performance becomes large with shrinking the device dimension. (See appendix for the details of the effects of the channel resistances and the contact resistances on the device performance.) For the photonic devices, laser diode (LD) and light emitting diode (LED) have been developed. The schematic illustration of the GaAs LED is shown in Fig. 2. 2. In this device, contact metals are also fabricated. When the contact resistance at the metal/semiconductor interface is higher than that of the inner device, the light emitting efficiency will be small.

An Ohmic contact is the contact that has a negligibly small contact resistance at the contact metal/semiconductor interface compared with that of the bulk semiconductor in the device. Other requirements for the Ohmic contact are schematically shown in Fig. 2. 3. Since the fabrication process after contact formation requires

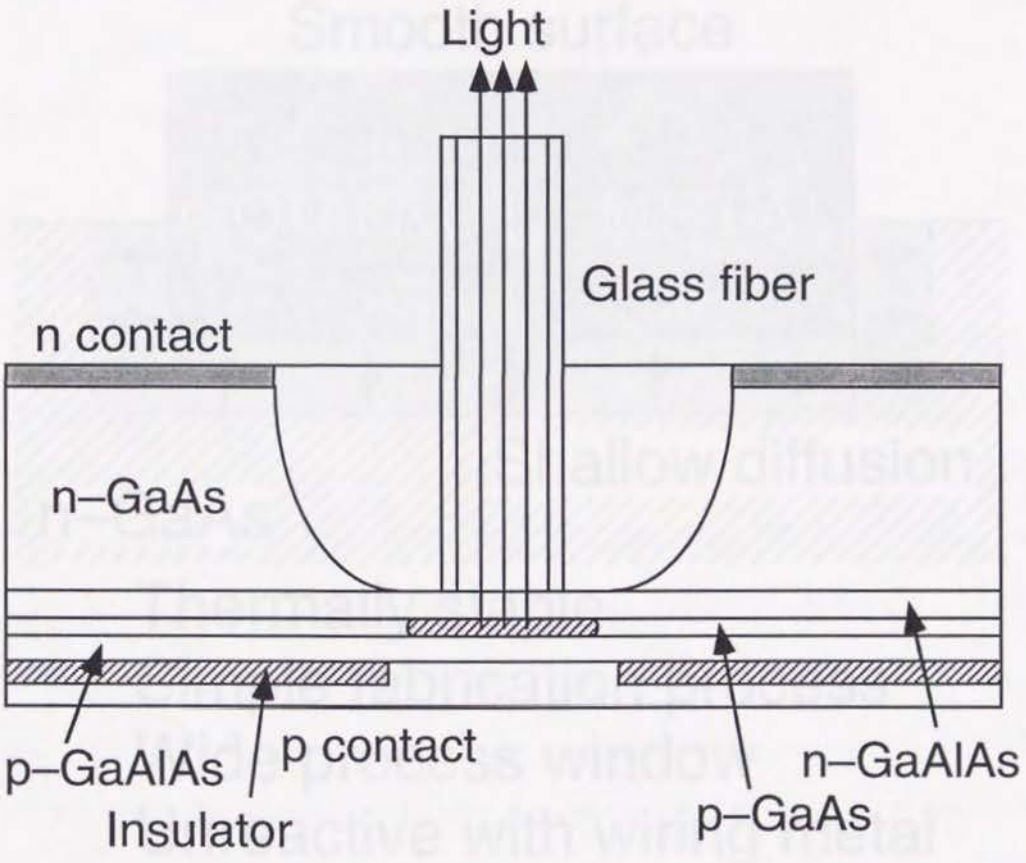

Fig. 2. 2 Schematic illustration of the GaAs LED.

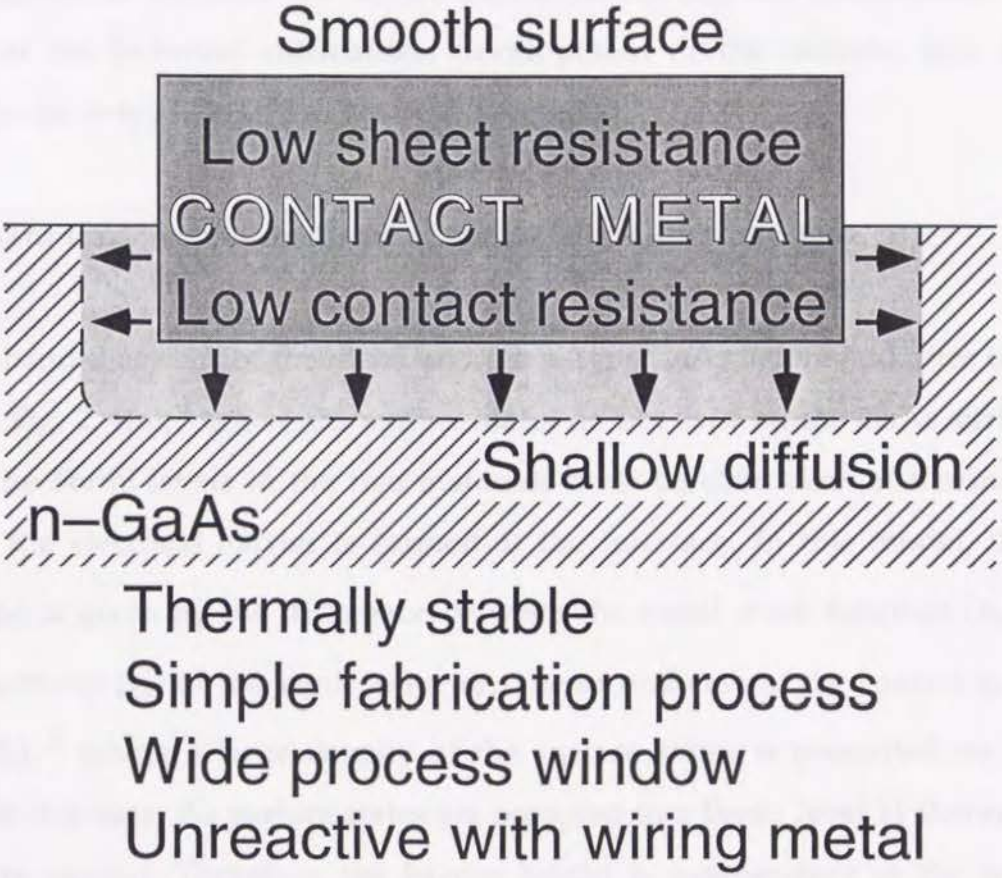

Fig. 2. 3 An ideal Ohmic contact to GaAs devices.

annealing at elevated temperatures up to 400 °C, the Ohmic contact should be stable at this temperature. In addition, since GaAs have a band gap wider than that of Si, the GaAs devices can operate at 350 °C or above. Also, the temperature of the device rises during operation. Therefore, thermal stability of the Ohmic contact is one of the requirements.

As described above, the device performance and the efficiency are effected by thecontact resistance. Therefore, development of the reliable Ohmic contacts is one of the key factors to improve the device performances and the reliabilities. However, because of the technical difficulties, development of the reliable, low resistance contacts to the n–type GaAs has not been succeeded.

2. 2. Current transport mechanisms at the metal/n–GaAs interface

The band diagrams of the metal and the n–type GaAs before and after contact are shown in Fig. 2. 4(a), [1] where the surface states do not exist on the GaAs surface. After contact, the Fermi levels in the two materials must be coincident at thermal equivalent and the electrical barrier is formed at the interface. In this model, the barrier height (ϕ_B) is given by the difference between the metal work function (ϕ_m) and the electron affinity (χ_s) of the semiconductor. The second case of the contact is shown in Fig. 2. 4(b), [2] where a large density of the surface states is presented on the GaAs surface. In this case, the surface states are occupied to a Fermi level at thermal equivalent before contact. Therefore, the barrier height is independent of the metal work function. The measured barrier height for n–Si and n–GaAs are shown in Fig. 2. 5 as a function of the metal work function. [3] The dependence of the barrier height of the n–GaAs to the metal work function is weaker than that of the n–Si, because the Fermi level of the GaAs is pinned by the surface states, as shown in Fig. 2. 4(b).

The electron transport mechanism is due to the dominant carrier through the

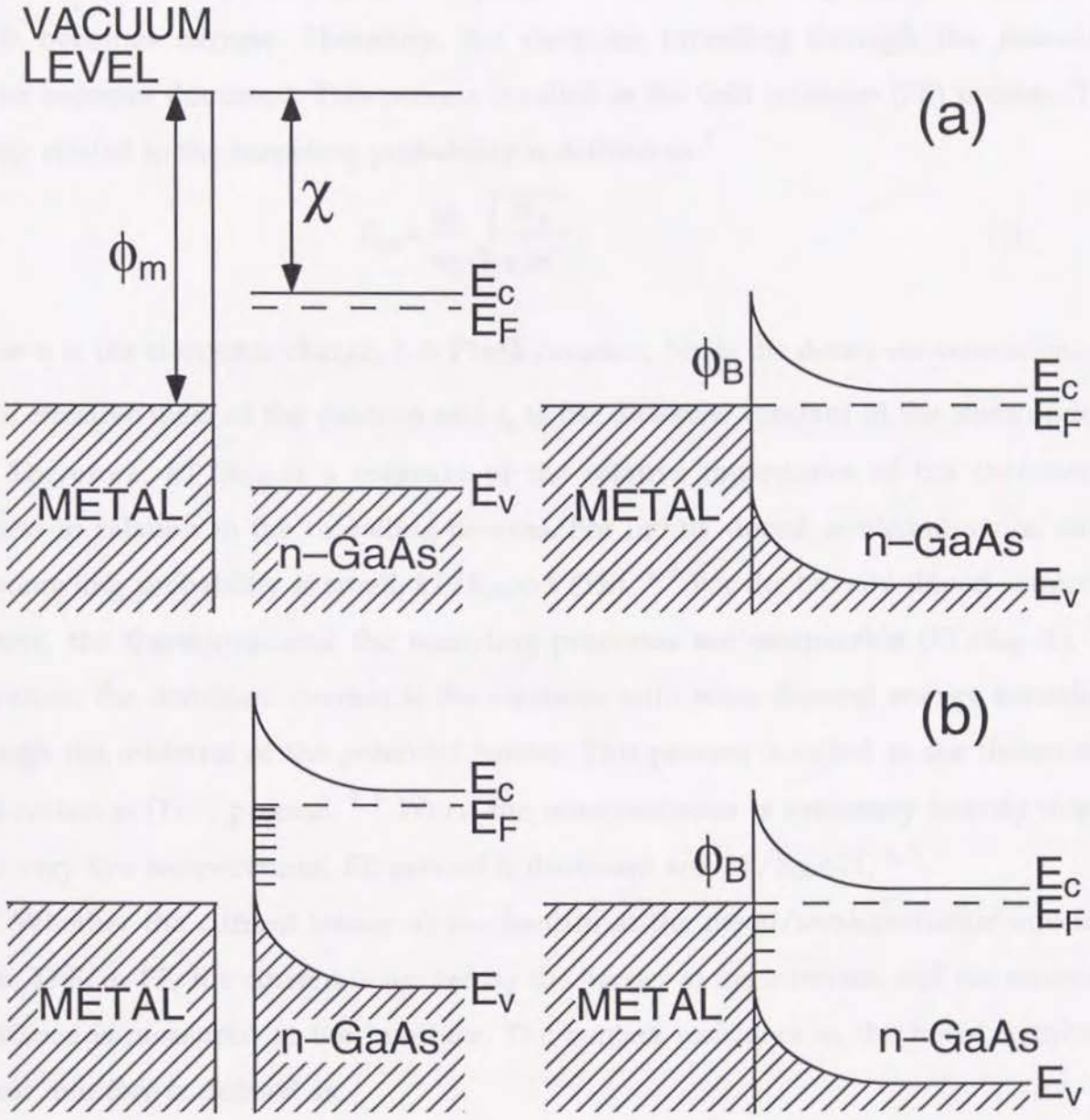

Fig. 2. 4 Energy band diagrams of metal/n–GaAs contacts.

metal/semiconductor interface. Three cases of the carrier transport mechanisms at the interface are shown in Fig. 2. 6. The electron transport mechanism where the dominant carrier is the electrons transport over the potential barrier is called as the thermionic emission (TE) process. This mechanism is dominant when the semiconductor is lightly doped. When the doping concentration is very high, the depletion width becomes narrow. Therefore, the electrons tunneling through the potential barrier becomes dominant. This process is called as the field emission (FE) process. The energy related to the tunneling probability is defined as [4]

$$E_{00}=\frac{qh}{4\pi}\sqrt{\frac{N_D}{\varepsilon_s m^*}}, \qquad (1)$$

where q is the electronic charge, h is Plank constant, N_D is the donor concentration, m^* is the effective mass of the electron and ε_s is the dielectric constant of the semiconductor. Therefore, kT/E_{00} is a measure of the relative importance of the thermionic process in relation to the tunneling process. For lightly doped semiconductors, since the tunneling probability is small, $kT/E_{00}>>1$ (TE). [4, 5] For the heavily doped semiconductors, the thermionic and the tunneling processes are comparable ($kT/E_{00}\sim1$). [4, 5] Therefore, the dominant current is the electrons with some thermal energy tunneling through the midstate of the potential barrier. This process is called as the thermionic field emission (TFE) process. [4, 5] When the semiconductor is extremely heavily doped or at very low temperatures, FE current is dominant and $kT/E_{00}<<1$. [4, 5]

Whether the current transport mechanism at the metal/semiconductor interface is TE, TFE, or FE, the current is limited by the barrier at the interface, and the electrical resistance is measured at the interface. The contact resistance at the metal/semiconductor interface is defined as

$$R_c \equiv \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0} \left(\Omega\text{-cm}^2\right), \qquad (2)$$

where J is the current density and V is the applied voltage. In the FE region, the

specific contact resistance is calculated by the Wentzel–Kramers–Brillouin (WKB) approximation. The result is [6]

$$R_c=\left[\frac{AT^2\pi q}{kT\sin(\pi c_1 kT)}\exp\left(\frac{-\phi_B}{E_{00}}\right)-\frac{AT^2 c_1 q}{(c_1 kT)^2}\exp\left(\frac{-\phi_B}{E_{00}}-c_1 u_F\right)\right]^{-1}, \quad (3)$$

where

$$A=\frac{4\pi m^* qk^2}{h^3} \quad (4)$$

is the Richardson constant,

$$c_1=\frac{1}{2E_{00}}\ln\left(\frac{4\phi_B}{u_F}\right), \quad (5)$$

and u_F is an energy difference between the Fermi level and the conduction band edge.

Similarly, the specific contact resistance in the TFE region is calculated to be

$$R_c=\left(\frac{kT}{qAT^2}\right)\frac{kT}{\sqrt{\pi(\phi_B+u_F)E_{00}}}\cosh\left(\frac{E_{00}}{kT}\right)\sqrt{\coth\left(\frac{E_{00}}{kT}\right)}\exp\left(\frac{\phi_B+u_F}{E_{00}\coth\left(\frac{E_{00}}{kT}\right)}-\frac{u_F}{kT}\right). \quad (6)$$

In the TE region, the specific contact resistance is given by

$$R_c=\frac{kT}{qAT^2}\exp\left(\frac{\phi_B}{kT}\right). \quad (7)$$

Note that the calculated values obtained by these equations are the specific contact resistance (R_c) in the unit of Ωcm^2. However, the contact resistance measured by transmission line method (TLM) [7] provides the contact resistance (R_c') in the unit of Ωmm and the channel sheet resistance (R_{ch}) in the unit of $\Omega/\square$. The R_c' values are converted to the R_c values by using an equation of $R_c=R_c'^2/R_{ch}$, assuming the sheet resistance in the channel of the semiconductor being equal to the sheet resistance under the contacts. [8]

The expected R_c values are plotted in Fig. 2. as a function of the doping

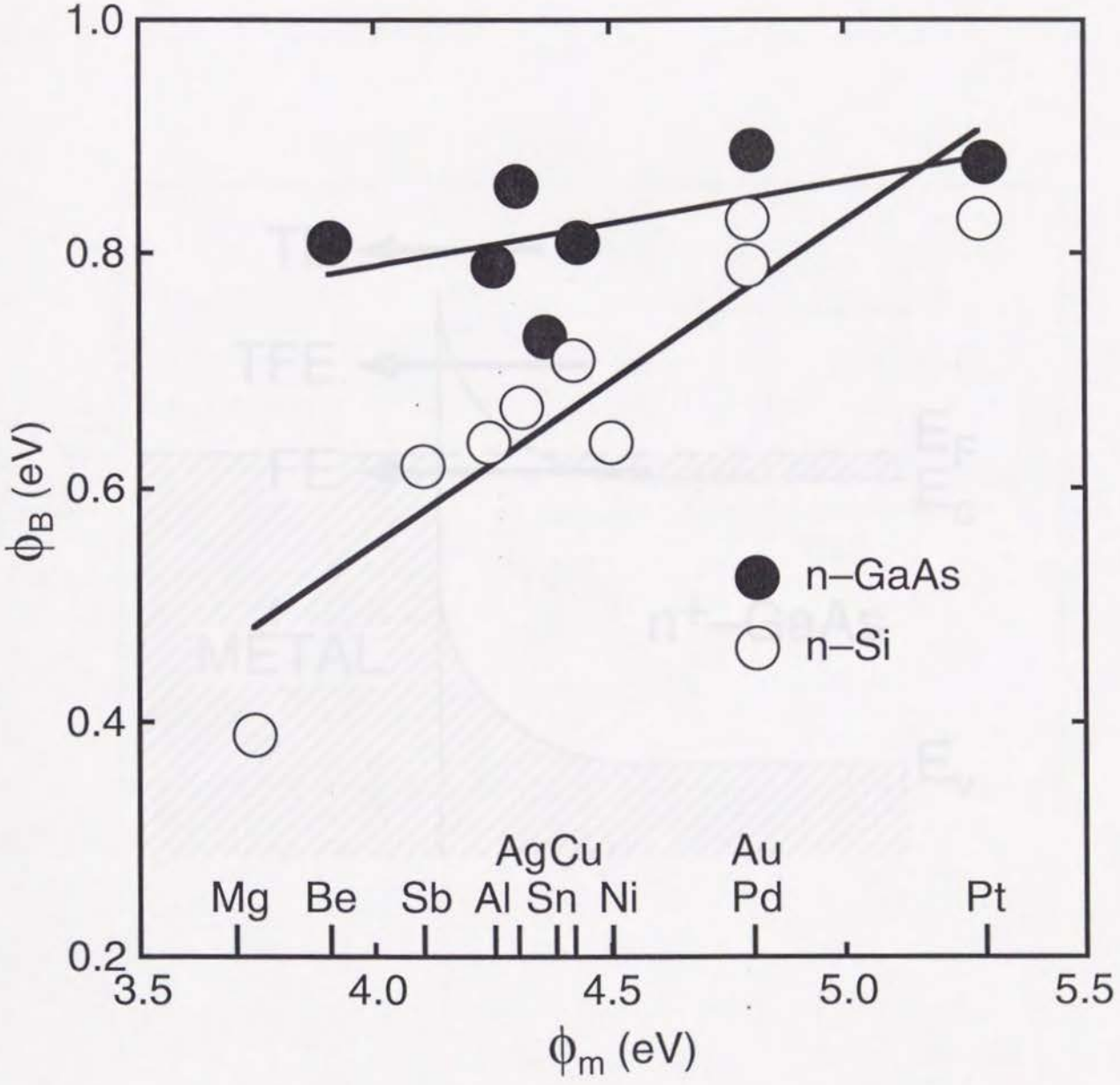

Fig. 2. 5 Experimental results of barrier heights for metal/n–type Si and metal/n–type GaAs contacts. [Ref. 3]

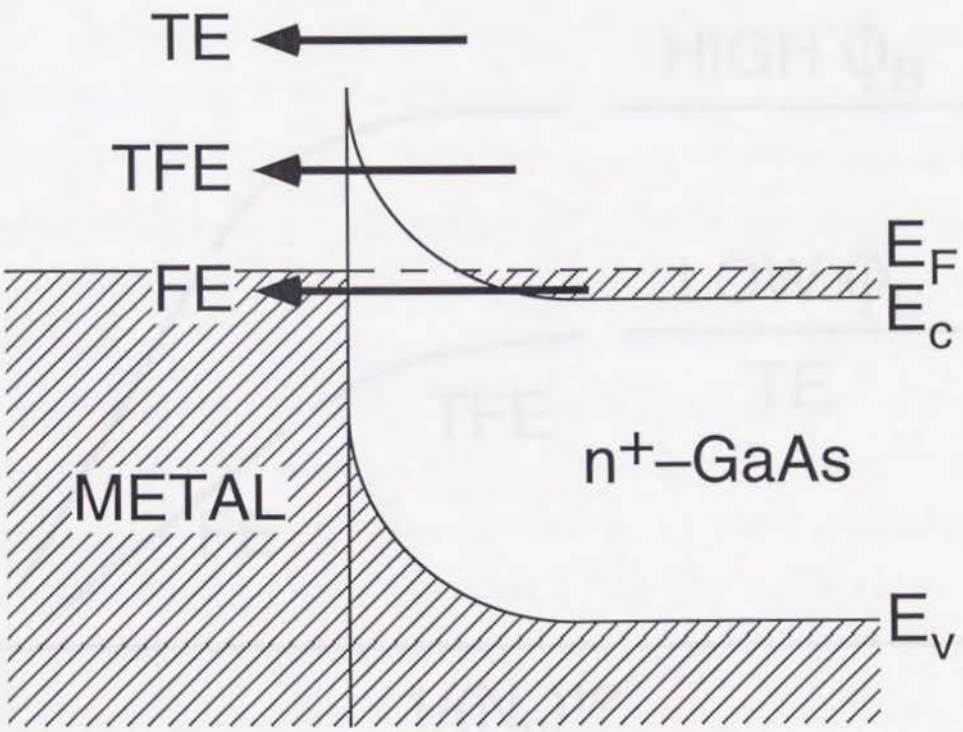

Fig. 2. 6 Three transport mechanisms at the metal/n–GaAs interface.

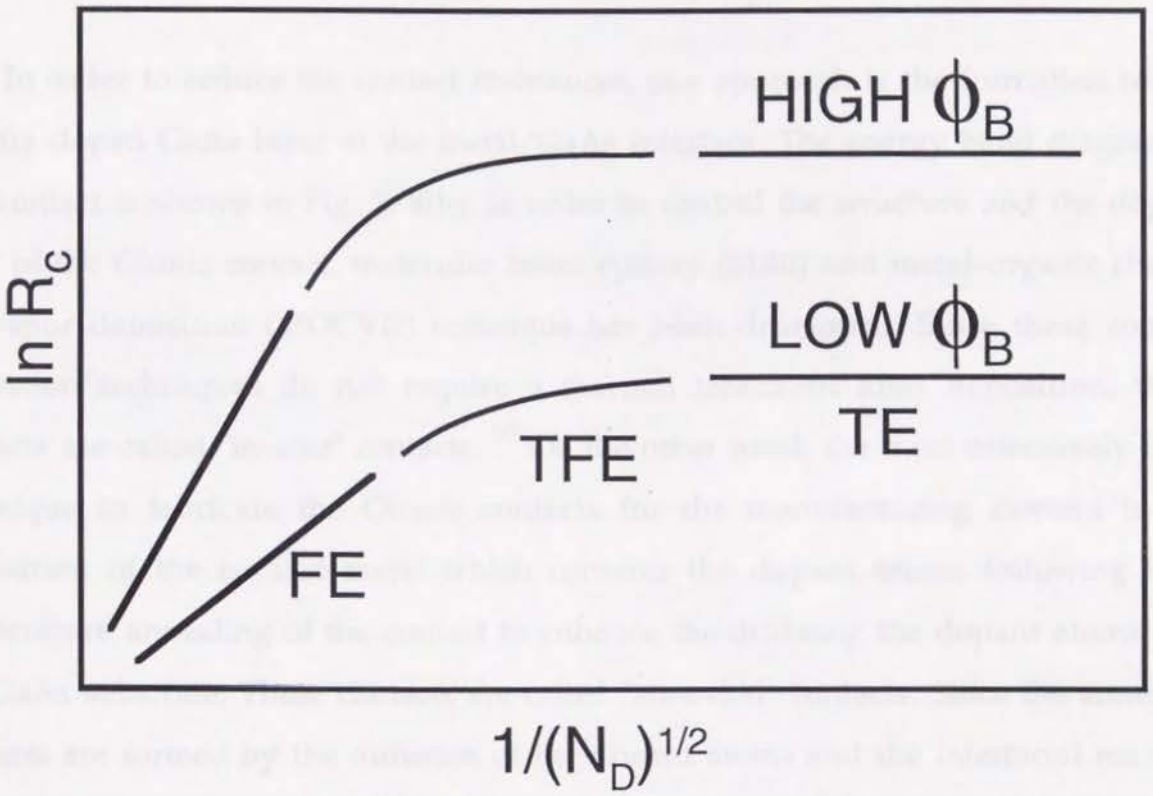

Fig. 2. 7 Theoretical dependence of the contact resistance on the doping concentration.

concentration for a high and a low barrier height. [6] The reduction of the specific contact resistance is expected with increasing the doping level and reducing the barrier height. Excellent agreement between the above theory and the experimental value was observed for n–type Si. [6, 9] Similarly, in order to reduce the specific contact resistance to n–type GaAs, increase of the doping level and/or the reduction of the barrier height are necessary.

2. 3 Various Ohmic contacts to n–type GaAs

In order to reduce the contact resistances, one approach is the formation of the heavily doped GaAs layer at the metal/GaAs interface. The energy band diagram of this contact is shown in Fig. 2. 8(b). In order to control the structure and the doping level of the Ohmic contact, molecular beam epitaxy (MBE) and metal–organic chemical vapor deposition (MOCVD) technique has been developed. Since these contact formation techniques do not require a thermal treatment after deposition, these contacts are called "in–situ" contacts. [10] On the other hand, the most extensively used technique to fabricate the Ohmic contacts for the manufacturing devices is the deposition of the contact metal which contains the dopant atoms following high temperature annealing of the contact to enhance the diffusing the dopant atoms into the GaAs substrate. These contacts are called "annealed" contacts. Since the annealed contacts are formed by the diffusion of the dopant atoms and the interfacial reaction between the contact metal and the GaAs substrate, control of the doping level and the microstructure is essential.

In order to reduce the contact resistances, reduction of the barrier height is most effective. However, since the fermi level of the GaAs is pinned at the surface states, [11] the barrier height is independent of the work function of the contact metals. Low resistance cannot be obtained only by depositing the contact metal, and the reduction of the contact resistances has been achieved by forming the middle layer which has a

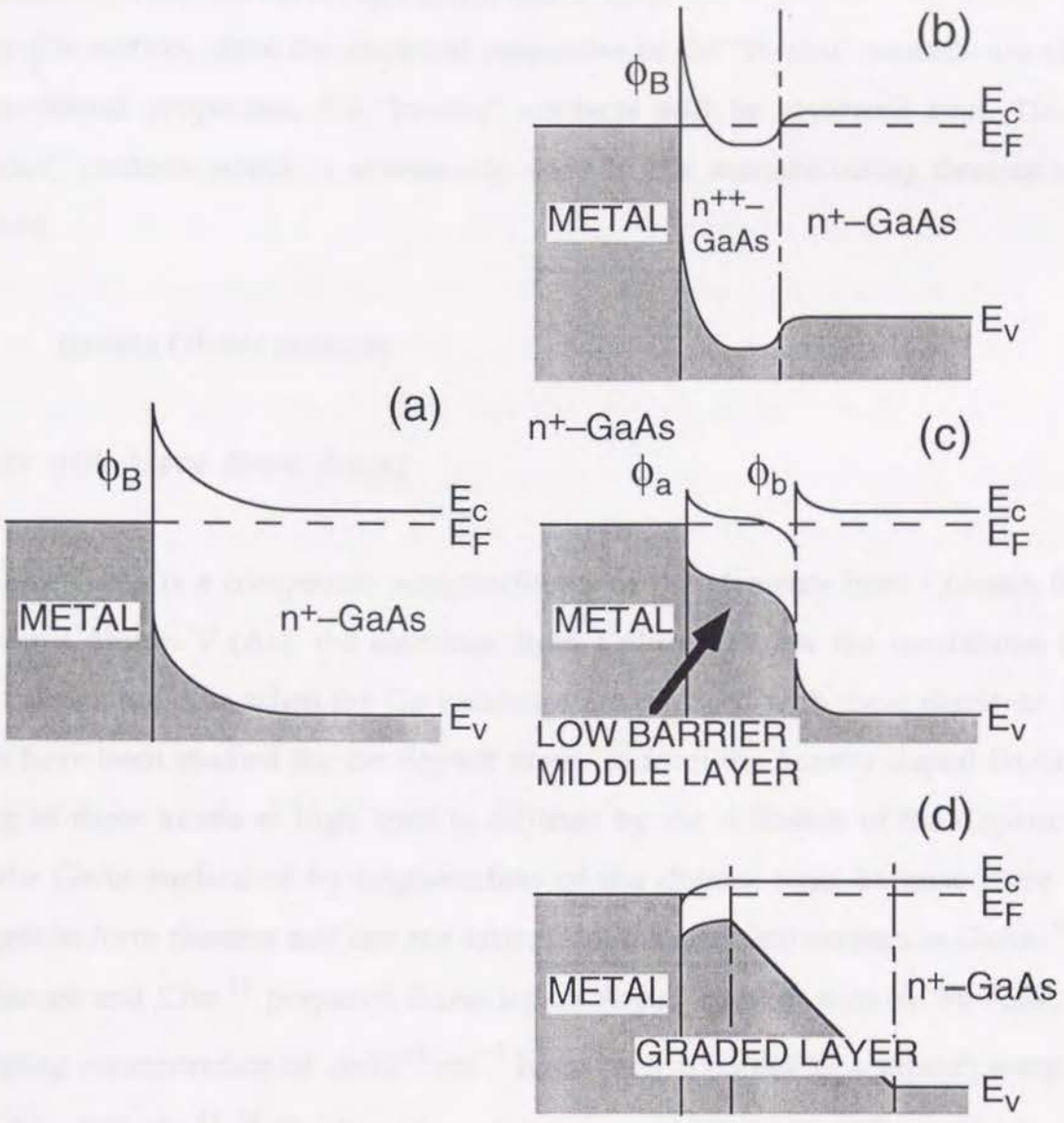

Fig. 2. 8 Energy band diagrams of metal/n–GaAs contacts with (a) intermediate doping, (b) heavy doping, (c) abrupt layer with low ϕ_B, and (d) graded layer with low ϕ_B.

narrow energy band gap or the low barrier height at the metal/middle layer interface. Also the barrier at the middle layer/GaAs interface should be low. The band diagrams of these contacts are shown in Figs. 2. 8(c) and 2. 8(d).

In this section, since the electrical properties of the "in–situ" contacts are close to the theoretical properties, the "in–situ" contacts will be reviewed first. Then, the "annealed" contacts which is extensively used in the manufacturing devices will be reviewed.

2. 3. 1 In–situ Ohmic contacts

Contacts with heavy donor doping

Since GaAs is a compound semiconductor of the elements from Column III (Ga) and from Column V (As), the elements from Column IV are the candidates for the dopant atoms to GaAs when the Ga vacancies are replaced with these elements. Si, Ge, and Sn have been studied for the dopant atoms to form the heavily doped GaAs layer. Doping of these atoms at high level is difficult by the diffusion of the dopant atoms from the GaAs surface or by implantation of the dopant ions, because these atoms segregate to form clusters and can not activate as the electrical carriers in GaAs. [10]

Barnes and Cho [12] prepared GaAs layers doped heavily with Sn by MBE, where the doping concentration of 6×10^{19} cm^{-3} have been achieved at a growth temperature lower than 580 °C. [13, 14] The R_c value of this contacts was 1.9×10^{-6} Ωcm^2. The similar heavily doped layers were also prepared by Tsang [15] at the Sn level of 8×10^{18} cm^{-3}. He obtained the R_c value of 3×10^{-5} Ωcm^2 before annealing and this value was reduced to 6×10^{-6} Ωcm^2 after annealing at 510 °C for 15 sec. Several other researchers have developed the Sn doped Ohmic contacts by MBE. [16, 17] However, since the Sn atoms segregate on the surface and it is difficult to prepare a layer with an abruptly in high doping

concentration, these Sn-doped MBE grown contacts are not suitable for GaAs devices. [18]

Chai *et al.* [19] selected Si as a dopant element to GaAs because Si has a large sticking coefficient on the GaAs, does not segregate on the GaAs surface, and is relatively insensitive to changes in growth conditions. [20, 21] Although efforts were made to dope GaAs with Si at a level higher than high–10^{18} cm^{-3}, Si precipitates were detected and the free–carrier concentration and the Hall mobility decreased. They found that Si was far less amphoteric than Ge and the free carrier concentration was a function of the substrate temperature and the As_4/Ga ratio. Kirchner *et al.* [21] measured the carrier density and calculated the space charge density of the Si doped MBE grown GaAs by Hall measurement and the contact resistivity, respectively. At Si density above 1×10^{19} cm^{-3}, although the bulk carrier density was independent of the Si concentration, the space charge density at the metal interface was equal to the Si concentration. The R_c value of 1.3×10^{-6} Ωcm^2 was measrued to the GaAs layers doped at 1×10^{20} cm^{-3} with Si. If the solubility limit of Si in GaAs was 2×10^{20} cm^{-3}, the R_c value of the "in–situ" contacts could be reduced as low as 5×10^{-7} Ωcm^2.

Heavily Si doped GaAs layers in the range of 10^{20} cm^{-3} were prepared by Schubert *et al.* [23] and Marcy *et al.* [24] by using the δ–doping technique. [25] The contact resistances measured by Cox and Strack [26] were in the 10^{-6} Ωcm^2 range with the doping concentration of 3.5×10^{20} cm^{-3}. [Ref. 23] The δ–doping technique would be effective to increase the surface donor concentrations that exceed those obtained by other growth techniques. [24]

Ge is also an n–type dopant in the GaAs. However, Ge was found to be an amphoteric dopant in GaAs. [27] By doping the Ge atoms at concentrations higher than 10^{15} cm^{-3} and annealing at temperatures higher than 950 °C, Ge was found to act as an n-type dopant. However, since Ge form a low barrier intermediate layer as described in the next section, Ge has been investigated to form an intermediate low barrier layer.

In order to reduce the contact resistance, the barrier at the metal/intermediate layer should be low and the lattice constant should be close to that of the GaAs. From these point of view, Ge, InAs and $In_xGa_{1-x}As$ were used for the low barrier intermediate layers.

Low contact resistances are expected at the metal/Ge interface, because the barrier heights of most metals on Ge are relatively low (ϕ_B~0.45 eV) [28] and the Ge layer can be doped heavier than that to the GaAs. In addition, since the lattice constant of Ge is close to GaAs, the barrier formed at the Ge/GaAs interface by the lattice mismatch is expected to be low. Stall *et al.* [29, 30] grew a heavily As doped (N_D=1.4×10^{20} cm^{-3}) Ge layer epitaxially on the GaAs substrate by MBE and deposited Au, subsequently. The R_c value of this contact was 1×10^{-7} Ωcm^2. The similar heavily doped Ge layer was prepared by Yamane *et al.* [31] by using MOCVD, where P was used as the dopant to the Ge layer. The MOCVD deposition technique has an advantage to grow selectively a layer in the SiO_2 window. The R_c value of this cotnact was higher than that prepared by MBE (1×10^{-5} Ωcm^2), because the doping concentration in the Ge layer was 1×10^{19} cm^{-3}.

The barrier height at the metal/n–InAs is lower than zero, because the Fermi-–level of the InAs is pinned in the conduction band. [32–34] In addition, band gap of InAs is four times narrower than that of GaAs. Therefore InAs is one of the best candidates for the intermediate layer. However, since the lattice constant of InAs is 7 % larger than that of GaAs, high density of misfit dislocation is expected at the InAs/GaAs interface, inducing the high potential barrier at the InAs/GaAs interface. In order to avoid these defects at the interface, Woodall *et al.* [35] deposited a graded $In_xGa_{1-x}As$ layer with composition from x=0 at the GaAs interface to 0.8≤x≤1 at the metal interface by MBE. The donor doping concentrations in the GaAs substrate and the middle layer were 2×10^{17} and 3×10^{18} cm^{-3}, respectively. They measured the contact resistances by TLM

and obtained the R_c values in the range of $5\times10^{-7} \sim 5\times10^{-6}$ Ωcm^2. The energy band diagram of this sample is shown in Fig. 2. 8(d). Nittono *et al.* [36, 37] deposited a compositionally graded n^+–$In_xGa_{1-x}As$ ($N_D = 1.5\times10^{19}$ cm^{-3}) by MBE, where x=0 at the GaAs interface and x=0.65 at the metal interface. The R_c value of this contact was 5×10^{-8} Ωcm^2 and reduced by a magnitude by heating the substrate temperatures at 450 °C during deposition. The R_c value of this contact increased after subsequential annealings at the temperature higher than 400 °C with a Ti/Pt/Au or a WSi contact metal. However, the R_c values of $\leq2\times10^{-7}$ Ωcm^2 were measured even after annealing at 800 °C with a WSi contact metal. A similar graded layer which deposited by using MOCVD have been reported. [38] However, the R_c value of this contact was 4×10^{-7} Ωcm^2 which was higher than that prepared by using MBE. Low resistance Ohmic contact was also prepared by Wright *et al.* [39] simplty by depositing the abrupt n^+–InAs layer which doped at the mid–10^{19} cm^{-3} directly on the GaAs substrate by MBE. The R_c value of 1×10^{-6} Ωcm^2 was obtained on the 5×10^{17} cm^{-3} doped GaAs. Some groups [40, 41] have been developed the low resistance Ohmic contacts by depositing a few monolayers of InAs and GaAs for a several periods to form a strained layer super lattice (SLS). In these contacts, low R_c value of 8.5×10^{-8} Ωcm^2 was obtained.

As described above, "in–situ" Ohmic contacts prepared by MBE showed extremely low contact resistances. However, the MBE deposition technique is not suitable for mass production, because this technique requires the high vacuum system and the growth rates of the intermediate layer are slow compare to other deposition techniques such as a vacuum deposition or a sputtering technique.

2. 3. 2 Annealed Ohmic contacts

Control of the doping level in the contact layer and the structure of the contacts are difficult by the deposition and the annealing technique, because the interfacial reaction between the cotnact metals and the GaAs substrate is difficult to control. However, the deposition and the annealing techniques are widely used in the manufacturing process, because the reproducibility of the deposition condition is excellent and the cost for the equipment is low. In this section, conventionally used AuGeNi contacts will be reviewed first.

Contacts with heavy donor doping

As described in Section 2. 3. 1, Ge works as a dopant in GaAs. Ge–based contacts were first developed by depositing Ge with Au. [42] Formation of AuGa compound is believed to enhance the formation of Ga vacancy and enhance the Ge doping in the GaAs substrate, [43, 44] leading to the reduction of the contact resistance. This contact can be prepared by using the conventional deposition system such as a vacuum evaporation [42, 43] and the various annealing systems such as furnace annealing, [46] e-beam annealing, [47] ramp annealing, [47] and laser annealing, [48–53] and the process window is wide. However, the surface of this contact was rough [54, 55] because the wetness of AuGe on the GaAs surface is poor. In addition, the diffusion depth of the contacts to the GaAs was deep and the thermal stability was poor.

Improvement of the AuGe contacts was first acheived by depositing Ni. [56] Addition of Ni to the AuGe contact improved the wetness [57–59] and the adhesion, leading to the formation of uniform contacts and the improvement of the reproducibility. [43] The AuGeNi contacts provided the R_c value of mid 10^{-7} Ωcm^2 after annealing at the temperature range between 420 and 550 °C. [60] Because of its low contact resistance and high reproducibility, the AuGeNi contact is the most widely

used in the GaAs device manufacturing process for more than 30 years. However, the surface of this contacts is still rough [57, 58, 61] and the thermal stability at 400 °C after contact formation is poor. [60] By the microstructural analysis, these weak points were found to be due to the formation of low melting point β– and β'–AuGa phases. [61–63]

Since the low melting point Au–Ga compounds are formed by the reaction between Au and GaAs, one approach to improve the thermal stability and the surface morphology is the formation of the contacts which do not contain Au atoms. Non gold Ge based contacts have been developed by Anderson *et al.*, [64, 65] where Ge was deposited on the GaAs substrate at the substrate temperatures of 425 °C to enhance the epitaxial growth, followed by the deposition of Ni. The lowest R_c value of 2×10^{-6} Ωcm^2 was measured after leaser beam annealing at the temperatures near the melting points of Ni and Ge. This contacts were stable at 350 °C for 6 h. Tanahashi *et al.* [66] prepared NiGe contacts by the conventional deposition and annealing system. This contact was thermally stable at 400 °C for 5 h and had a smooth surface. However, this contact provided a relatively high R_c value of low–10^{-5} Ωcm^2 to the n–type GaAs with the doping concentration of 1×10^{18} cm^{-3}.

In order to reduce the R_c value of NiGe contacts, addition of a small amount of third element, which will enhance the Ge doping into the GaAs or which will work as a dopant, is believed to be effective. Au, [67] Ag, [68] Pt, Pd, and Cu [69] were selected as the candidates for the third element because these atoms were expected to increase the Ge doping concentration at the metal/GaAs interface by forming the compounds with Ga. The lowest R_c values was observed after adding a small amount of Au. NiGe(Au) contacts provided the R_c value of 2×10^{-6} Ωcm^2 and this R_c value did not change at 400 °C for 3 h. [67] (Note that the addition of a small amount of Pt or Pd was also found to be effective to reduce the R_c values. [69] However, the formation mechanism of these contacts was found not to be the formation of heavily doped layer. Therefore these contacts will be reviewed in the next section.)

Te and Sn were also selected as a third element, [69] because the elements from Column VI are also expected to work as a dopant in the GaAs. The NiGe(Te) contacts provided the lowest R_c value of 1.7×10^{-6} Ωcm^2 and the smooth surface. This R_c value increased slightly after annelaing at 400 °C for 10 h. The temperature dependence of the R_c values of the NiGe(Te) contacts indicated that the formation mechanism of this contacts was the formation of the heavily doped layer at the metal/GaAs interface.

Another approach is the formation of the "non–gold" contacts by replacing the Au with other metals. AlNiGe contacts have been developed by Zuleeg *et al.* [70] because the eutectic temperature of AlGe is higher than that of the AuGe and therefore improvement of the thermal stability is expected. This contacts provided the R_c value of 1.4×10^{-6} Ωcm^2 and a smooth surface. Thermal stability of this contacts is not clear at the moment.

Non gold Ge–based contacts were also developed by Shinha *et al.* [71] where Ge and Pd were sequentially deposited, becasue Pd was found to be reactive with Ga atoms [72–74] and the similar effects of the Ni addition were expected by the Pd addition. This contact provided the R_c value of 3.5×10^{-5} Ωcm^2 after annealing at 500 °C. The detail investigation of the formation mechanism of the PdGe contacts was reported by Marshall *et al.* [75] and other groups. [76, 77] In the PdGe contacts, deposition of Pd directly onto the GaAs substrate was found to be necessary and the thickness of Ge layer should be larger than that required for the PdGe formation to reduce the contact resistance. [75] Marshall *et al.* [75] prepared Pd/Ge contacts and obtained the R_c value of less than 2×10^{-6} Ωcm^2 where the doping concentration of the GaAs substrate was 1×10^{18} cm^{-3}. The carrier transport mechanism of the PdGe contacts is believed to be the tunneling mechanism by measuring the temperature dependence of the contact resistances. [78] Although this contact provided a low contact resistance and a smooth surface, [79] thermal stability at 410 °C was poor. [80]

Another dopant to n–type GaAs is Si. The advantages to use Si as a donor were

described in the previous section. In addition, Si is expected to be doped heavily in the GaAs than Ge, leading to reduction of the contact resistances. However, Ohmic contacts were not formed only by depositing Si and annealing. Addition of P to the Si was found to be effective to enhance the Si diffusion into the GaAs substrate by Kavanagh *et al.* [81] They measured the contact resistance of Si(P)/GaAs contacts where the P concentration was 4 wt% and obtained the contact resistance of $\leq 2\times10^{-4}$ Ωcm^2 after annealing at 800 °C for 15 min. The doping concentration of Si was measured to be 4.8×10^{18} cm^{-3}.

Similar to the development of the Ge–based Ohmic contacts, Au was deposited with Si. [82, 83] AuSiNb contact was developed bu Coquat *et al.*, [84] where Nb was added to match the thermal expansion coefficient of the contacts with the GaAs substrate. This contacts provided the R_c value of 5×10^{-5} Ωcm^2. This R_c value deteriorated after annealing at 300 °C for 90 h. Ag instead of Au was also deposited with Si, because the eutectic temperature of AgSi is higher than that of AuSi and therefore thermal stability was expected. This contact provided the R_c value of 2.5×10^{-5} Ωcm^2. In order to improve the adhesion betweent the contact metal and the substrate, Ni was added to the AgSi contacts, however, significant reduction of the R_c value was not measured.

From the similar view point of the development of non–gold Ge–based Ohmic contacts, non–gold Si–based contacts have been developed. Near noble metals such as Pt, [85] Ni, [86-88] and Pd [71, 89, 90] were deposited with Si, because these metals are reactive with GaAs at relatively low temperatures and are expected to form high melting points silicide after contact formation. Budhani *et al.* [91] prepared Pt_xSi_{1-x} layers with various Si compositions by rf sputtering the Pt target in a silane diluted argon plasma. In order to reduce the R_c value, deposition of the Si rich layer was found to be necessary. However, the R_c values of this contacts were high. The R_c values of NiSi contacts were first measured by Takata *et al.* [92] They deposited NiSiW contacts by e–beam evaporation, where the W was used as a cap layer. The NiSiW contacts provided the

R_c values of 6×10^{-5} Ωcm^2 to the GaAs substrate with a doping concentration of 1×10^{18} cm^{-3}, showed a smooth surface and were thermally stable. Development of PdSi have been investigated by Wang *et al.* [93] They found that the deposition of PdSi layers whose initial atomic ratio of Si to Pd was 0.65 or higher was necessary to prepare the R_c values of low–10^{-6} Ωcm^2 to the GaAs substrate with a doping concentration of 1×10^{18} cm^{-3}. The R_c value of this contacts was increased to 2×10^{-5} Ωcm^2 after annealing at 410 °C for 33 h. The carrier transport mechanism is believed to be the tunneling mechanism through the interface between the metal and the n^+–GaAs, which was formed by the excess Si.

Another dopant which has been widely investigated is Sn. Sn was deposited directly on the GaAs to fabricate Gunn oscillators. [94] The sputter deposited Sn/W contacts showed the R_c values of $\leq1\times10^{-5}$ Ωcm^2 to the GaAs substrate with a doping concentration of 2×10^{18} cm^{-3} after laser annealing. [95] Since Sn does not wet the GaAs uniformly, Ni, [96, 97] Ag, [98, 99] Au [100], Pd [95] and Au–Ni [101, 102] were deposited with Sn. AgSn contacts showed the lowest R_c value of 1×10^{-5} Ωcm^2 to the GaAs with a doping concentration of 6×10^{18} cm^{-3}. [98] The surface mophologies of these Sn–based contacts were rough [100, 103] and the significant reduction of the contact resistances has not been observed.

The elements from Column VI are also the dopants to GaAs. A few investigations of AuTe, [82] AuTeNi [104] and AuTeAu [105] have been reported. The lowest R_c value was reported on the AuTeNi contacts, where Ni and AuTe alloy was deposited on the GaAs substrate by e–beam evaporation. After annealing at 510 °C for 1.5 min, this contact provided the low R_c value of 5×10^{-7} Ωcm^2 and was thermally stable at 250 °C for 1 h. However, surface morphology was rough. [104, 106]

Summarizing the alloyed Ohmic contacts with heavy donor doping layer the Ge–based contacts are the most extensively used contacts in the manufacturing GaAs

devices, becase the Si, Sn and Te–based contacts did not provided the R_c values lower than those of the Ge–based contacts. Thermal stability and surface morphology of the AuGeNi contact were improved by reducing the amount of Au atoms. Although non gold NiGe contacts provided high R_c values, significant reduction of the R_c values were obtained by depositing a small amount of dopant atoms such as Te. Therefore, the NiGe–based contacts with a small amount of third layer these contacts are attractive for the contacts to the VLSI GaAs devices or submicron gate length MESFET.

Contacts with low barrier height

As described in the previous section, Ge forms a low barrier intermediate layer between the contact metal and the GaAs substrate. Furumai *et al.* [69] reported the detail investigation of the formation mechanism of NiGe(Pd) and NiGe(Pt) contacts. In these contacts, reduction of the contact resistances is believed to be the formation of heavy As doped epitaxial Ge layer. This As atoms would be supplied from the GaAs substrate after forming a Pd–Ga or Pt–Ga phase. The NiGe(Pd) contact provided the R_c value of 6×10^{-7} Ωcm^2 after annealing at 400 °C for 5 s. However, thermal stability at 400 °C of this contact was poor.

Indium (In) was used as a contact metal at the earliest stages of development of the GaAs devices, because the melting point of In is low (~156 °C). The relationship between the doping concentration and the contact resistances of the In/GaAs contacts was first reported by Gol'dberg and Tsarenkov. [107] The $In_xGa_{1-x}As$ layer which is believed to reduce the contact resistance as described above have been first detected by Hartnagel *et al.* [108] by analyzing the microstructures of the InGeAg contacts. However, carrier transport mechanism of the In–based contact have not been understood yet. Lakhani[109] examined the reaction between the In film and the GaAs substrate during heat treatment. He found that the $In_{0.8}Ga_{0.2}As$ layer was formed on the contact surface

and the compositionaly graded $In_xGa_{1-x}As$ layer was grown on the GaAs substrate. The energy band diagram he proposed was close to that of the MBE grown $In_xGa_{1-x}As$ contacts developed by Woodall *et al.* [35] However, the R_c value of this contact was 1.2×10^{-5} Ωcm^2 which is higher than that prepared by MBE by a factor of two. Kim *et al.*[110] prepared In/W contacts with various In thicknesses and found that the contact with a few nm thickness In provide the low R_c value of 1.3×10^{-6} Ωcm^2 and an excellent thermal stability at 400 °C. However, surface morphology of these In–based contacts were poor.

In order to reduce the contact resistances and improve the thermal stability of the In–based contacts, various metals were deposited with In. Au was deposited with In, [82, 114, 115] however, significant improvement has not been achieved. AgGeIn contacts have been developed by Cox and Strack [26] and other researchers, [98, 111] although their interests in the In layer was the reduction of the liquid alloy surface tension and the promotion of the good wetting of the GaAs. Ag was chosen as a major component because the Ag–GaAs eutectic occurs at 650 °C [112] and Ge was chosen as a dopant in the GaAs. AgGeIn contacts provided the R_c value of 7.5×10^{-6} Ωcm^2 and rough surface. Similar results were obtained in the AuGeIn contacts. [111, 113] This contact provided the R_c value of 1.3×10^{-6} Ωcm^2 after annealing by laser, however the surface morphology was still poor. [113] Thermal stability of the In contacts was improved by adding the Pd layer. Allen *et al.* [116] deposited Pd and In on the GaAs substrate with a Si doping concentration of 2×10^{18} cm^{-3}. After annealing at 500 °C for 20 s, this contact provided the R_c value of 7×10^{-7} Ωcm^2. This R_c value increased slightly after annealing at 400 °C for 30 min. Wang *et al.* [117] deposited a Pd layer on the GaAs followed by 20–period Pd–In multilayer. After annealing at the temperature in the range between 600 and 650 °C, this contact provided the R_c values of $\leq2\times10^{-6}$ Ωcm^2. Reduction of the R_c value was achieved by depositing a Ge layer on the InPd

contact. [117] This contact provided the R_c values less than 1×10^{-6} Ωcm^2 and the thermal stability at 400 °C for 30 h.

Significant improvement of the In–based contacts have been achieved by depositing Ni. Murakami *et al.* [118, 119] deposited Ni/In–Ni/Ni/W contacts by e–beam evaporation and radio frequency (rf) induction heater, where the second layer was coevaporated from Ni and In. After deposition, the samples were covered by a 50 nm thick Si_3N_4 layer which required the heat treatment of 300 °C for 30 min. The R_c value of this contacts was 3×10^{-6} Ωcm^2 at the annealing temperature range between 800 and 1000 °C. This contact also provided the smooth surface and the thermal stability at 400 °C for 100 h. This excellent thermal stability is believed to be due to the formation of the high melting points Ni_3In (T_m ~ 908 °C), NiAs (T_m ~ 962 °C) and $In_xGa_{1-x}As$ ($T_m \geq$ 940 °C) compounds. [119, 120] This excellent thermal stability did not deteriorate at 400 °C for 100 h after depositing Al over layer, which is the key element of the wiring metal in the Si device technology. By comparing the results of the microstructural analysis of InGeW, [120] InGeMoW, [121] and InNiW [120] contacts, they found that the contact resistances will be reduced with increasing the total contact area of the $In_xGa_{1-x}As$ /GaAs interface. Similar NiInW contacts have been developed by Hugon *et al.* [122] by using sputtering deposition technique. Further reduction of the contact resistances of the InNiW contacts was achieved by adding Si atoms. [123] Addition of a small amount of Si reduced the R_c values by the factor of two, which is believed by the effects of the heavy donor doping to the $In_xGa_{1-x}As$ layer and the GaAs. Note that the addition of Ge did not reduce the R_c values significantly. The reason has not been understood. The InNi(Si)W contact provided excellent thermal stability at 400 °C for 100 h. However, the thermal stability of this contact deteriorated after depositing TiAlCu over layer which is widely used in the Si device technology. Since these InNiW and InNi(Si)W contacts are formed at the annealing temperatures around 850 °C, the implanted dopants in the GaAs substrate can be activated simultaneously during the

contact formation. [118, 119] Therfore, these contacts can be formed in the one–step annealing process, which is believed to improve the device performance and reduce the fabrication costs.

InAs–based annealed contacts have been first developed by Kim *et al.* [124] They deposited the InAs/W contact where the InAs layer was not intentionally doped. The InAs layer was sputter–deposited from the InAs target by Ar ions and the W layer was deposited by e–beam deposition. This InAs/W contacts did not show Ohmic behavior at the annealing temperature below 850 °C and provided the R_c value of low–10^{-6} Ωcm^2 after annealing at 1000 °C for 1 sec. The reason that this contact did not show Ohmic behavior after annealing below 850 °C is believed that the thin oxide layer on the GaAs substrate prevent the interfacial reaction between the InAs and the GaAs at the low temperatures. The formation temperature was reduced by depositing Ni layer in the InAs/W contacts. InAs/Ni/W and Ni/InAs/Ni/W contacts were deposited where Ni was deposited by e–beam deposition. These contacts provided the R_c value of mid–10^{-6} Ωcm^2 after annealing at 750–850 °C and the excellent thermal stability at 400 °C for 100 h. The effect of the Ni addition is believed to be the enhancement of the reaction between the InAs and the GaAs substrate, leading the improvement of the adhesion by removing the surface oxide layer and the improvement of thermal stability by forming the high melting point NiIn compounds. They found another effect of Ni addition that the Ni destroyed the compositional stoichiometry of the InAs layer by forming NiAs compounds and enhanced the reaction between the InAs and the GaAs. The high R_c value of these contacts compare to other In–based contacts is believed to be due to the high potential barrier at the $In_xGa_{1-x}As$/GaAs interface due to the presence of defects.

Summarizing the alloyed Ohmic contacts with low barrier height, the InNiW contacts are attractive for their smooth surface and thermal stability even after depositing the wiring metals and the InNi(Si)W contacts are attractive for their low contact resistances and thermal stability without wiring metals. However, fabrication

process of these contacts were not simple and the patterning of the W layer deposited by e-beam deposition is difficult by the lift off technique. Sputter-deposited In As-based contacts are attractive for the manufacturing process because the fabrication process is easy and the contacts are thermally stable. However, the contact resistances of this contact are not sufficiently low. Therefore, sputter-deposited InAs-based contacts are believed to be the promising cotnacts to the manufactureing GaAs technology, if the cotnact resistances are reduced.

2.4 Thesis objective

As reviewed in the previous section, in spite of the continuous efforts to develop the reliable and low resistance Ohmic contacts for more than 30 years, the contact which satisfy all of the ideal conditions has not yet been developed. Therefore, the goal of the present study is the development of the Ohmic contacts which satisfy all the requirements to the Ohmic cotnacts as descrived in Fig. 2. 3. In this thesis, because the extremely low resistance Ohmic contacts have been developed in the "in-situ" $In_xGa_{1-x}As$ based contacts, development of the annealed $In_xGa_{1-x}As$-based contacts are challenged. In addition, radio frequency (rf) sputtering deposition technique is used to deposit the contacts, becasue this technique is easy to apply to the manufacturing process. Therefore, the main objective of this thesis is the development of low resistance $In_xGa_{1-x}As$-based Ohmic contacts by rf sputter deposition and annealing.

2.5 References

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3.1 Formation mechanism of InAs/Ni/W contact

3.1.1 Introduction

As described in Sec. 2, one of the most effective methods to reduce the contact resistance is to form an intermediate layer with low energy barrier between the contact metal and the GaAs substrate. Stoichiometric InAs is the best candidate for the intermediate layer for n–type GaAs, because it has a narrow energy gap, the Fermi level of the InAs is pinned in the conduction band,[1,2] and therefore a "zero" barrier between the metal/InAs interface is expected. However, there is about 7 % lattice mismatch between the InAs and the GaAs, and a high density of misfit dislocations is expected at the InAs/GaAs interface, which prevents reduction of the contact resistance.

Wright *et al.* [3] prepared Ohmic contacts by growing a nearly abrupt n^+–InAs layer directly on the n–GaAs layer using the molecular beam epitaxy (MBE) technique, which provided the R_c values of 0.3~0.5 Ω–mm. Molecular beam epitaxy is a very attractive deposition technique, because the compositions of deposited materials can be controlled precisely. However, from a manufacturing process view point, this technique is not suitable for mass production.

Recently, Kim *et al.* [4] prepared InAs/Ni/W and Ni/InAs/Ni/W Ohmic contacts by both the sputter–deposition and e–beam evaporation techniques without intentional donor doping in the InAs layer. They added Ni layer to the InAs contact, because Ni is expected to improve the adhesion between the contacts and the GaAs substrate by forming Ni_xGaAs during heating process. This role of the Ni layer was found in the conventionally used AuGeNi contacts. [5–11] In addition, Ni is expected to improve the thermal stability after contact formation by forming high melting point In-Ni compounds. They obtained the R_c value of ~0.4 Ω–mm after annealing at temperatures in the range of 750–850 °C. They found that the Ni enhanced the interaction between the

InAs and the GaAs by forming NiAs compounds and breaking the compositional stoichiometry of the InAs. [4] However, other roles of the Ni layer and the effects of thermal hysteresis on the Ohmic contact formation were not understood.

The main purposes of this section are twofold. The first is to understand the roles of Ni during a various thermal hysteresis on the InAs–based contacts. For this purpose, various samples with different deposition sequences were prepared. These contacts were prepared using the radio frequency sputtering technique, because this technique is suitable for mass production of the electrode materials and allows us to deposit various materials such as refractory metals, composite materials, and semiconductor materials. After deposition, the samples were annealed by a rapid thermal annealer (RTA) at high temperatures for short time, which gave a "thermal shock" to the contacts. Thus, in order to understand the effect of the thermal hysteresis on Ohmic contact formation, pre–annealing of the samples at 300 °C for 30 min prior to high temperature annealing was also carried out. The interfacial micro–structures were analyzed by x–ray diffraction (XRD), cross–sectional transmission electron microscopy (XTEM) and Auger electron microscopy (AES). The electrical properties were measured by the transmission line method (TLM). [12] The second is to understand the current transport mechanism of the InAs/Ni/W contacts. For this purpose, the electrical properties were characterized by measuring the contact resistances at various temperatures.

3.1.2 Experimental Procedure

The samples used in the present study were sequentially deposited by the rf sputtering technique. Prior to metal deposition, the wafers were chemically cleaned by rinsing in HCl for 3 min and then deionized water for 1 min. The vacuum system was pumped down to ~2×10^{-5} Pa before deposition. The mean deposition rates of InAs, Ni,

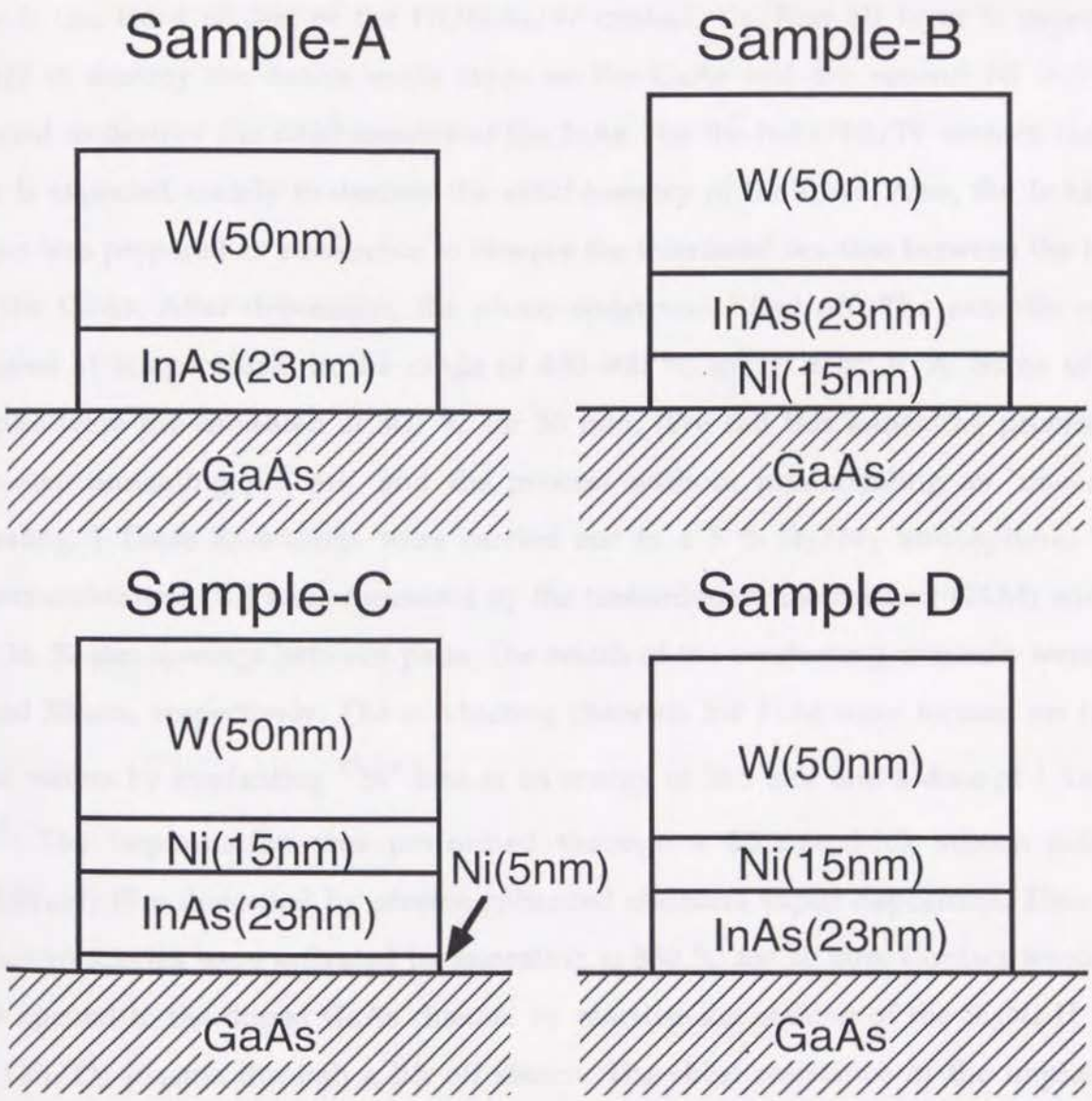


Fig. 3. 1 Cross sections of InAs/W, Ni/InAs/W, Ni/InAs/Ni/W, and InAs/Ni/W contacts.

and W were about 7 nm/min, where the Ar pressure during the deposition was kept at 4×10^{-1} Pa. The thicknesses of each layer of the InAs/W, Ni/InAs/W, Ni/InAs/Ni /W, and InAs/Ni/W contacts are schematically shown in Fig. 3. 1. For the Ni/InAs/W contact, the first Ni layer is expected mainly to destroy the native oxide layer on the GaAs substrate. For the Ni/InAs/Ni/W contact where the thickness of the first Ni layer is one third of that of the Ni/InAs/W contact, the first Ni layer is expected mainly to destroy the native oxide layer on the GaAs and the second Ni layer is expected to destroy the stoichiometry of the InAs. For the InAs/Ni/W contact, the Ni layer is expected mainly to destroy the stoichiometry of the InAs. Also, the InAs/W contact was prepared as a reference to observe the interfacial reaction between the InAs and the GaAs. After deposition, the photo–resist was lifted off. The samples were annealed at temperatures in the range of 400–900 °C for ~1 s by RTA. Some of the samples were pre–annealed at 300 °C for 30 min. (We call this annealing process as "two–step annealing process" and the process without preannealing as "one–step annealing.") These annealings were carried out in a 5 % H_2/N_2 atmosphere. The contact resistances (R_c) were measured by the transmission line method (TLM) with 2, 4, 8, 16, 32 μm spacings between pads. The width of the conducting channels were 15, 25 and 30 μm, respectively. The conducting channels for TLM were formed on (100) GaAs wafers by implanting $^{29}Si^{+}$ ions at an energy of 38.5 keV and a dose of 1.3×10^{14} cm^{-2}. The implantation was performed through a 50 nm thick silicon nitride (a-Si_3N_4:H) film deposited by plasma enhanced chemical vapor deposition. Then the implanted species were activated by annealing at 850 °C for 20 min. Contact windows were opened to the doped GaAs channel by reactive–ion etching of the Si_3N_4:H film in a CF_4/O_2 plasma through a lift off stencil. The sheet resistance of the implanted layer was measured to be about R_{ch}~160 Ω/□.

Microstructures of the contacts were analyzed by XRD, AES, and XTEM. A computer controlled Rigaku x–ray diffractometer using Cu*K*α radiation, operated at 40

kV and 30 mA, was used. The diffracted intensities were measured using a scintillation counter with the soller slits and a singly bent graphite monochrometer. For cross-sectional TEM study, specimens were mechanically polished by Gatan dimple grinder and then ion milled by Ar^+ ion. A JEM-4000EX was operated at 400 kV to obtain lattice images.

In order to understand the current transformation mechanism, the Rc values at 27 °C to -196 °C were measured for the InAs/Ni/W contacts, where the wafers were mounted on the connector, and the contact metals and the terminals were connected with Al-Si (1 %) wires using an ultrasonic wire bonder.

3.1.3 Experimental Results

Effects of thermal hysteresis

Current-Voltage (I-V) measurements were carried out for Sample A and Sample D and three types of I-V characteristics were observed. The observed I-V behaviors are listed in Table 3. I, where symbols ×, △, and ○ indicate non-ohmic, ohmic-like, and

Table 3. I. I-V Characteristics of Sample A and D.

Sample Number	Structure	Annealing Process	Annealing temperature (°C)					
			400	500	600	700	800	900
A	InAs/W	one-step	×	×	×	×	×	×
		two-step	×	×	△	△	△	△
D	InAs/Ni/W	one-step	×	×	×	×	×	○
		two-step	×	○	○	○	○	○

Ohmic behavior, respectively. (Here the "ohmic behavior" means perfect linear I–V characteristics and the "ohmic–like behavior" means straight line I–V characteristics.) Note that Ohmic behaviors were observed in the samples which were annealed by the two–step annealing process and this behavior was not observed in the samples which were prepared by the one–step process.

The XTEM micrographs of Sample D annealed at 750 °C for 1 s by one–step annealing process is shown in Fig. 3. 2. $In_xGa_{1-x}As$ phases are observed between the W layer and the GaAs substrate. As seen in this micrograph, a high density of stacking faults are observed in the $In_xGa_{1-x}As$ layer and at the $In_xGa_{1-x}As$/GaAs interface. These defects are believed to be introduced by thermal shock (quick heating to high temperature) as will be discussed later.

Effects of Ni addition

The XRD profiles of Sample A before annealing, after pre–annealing, and after annealing at 650 °C for 1 s (called as "high temperature annealing") are shown in Figs. 3. 3(a), 3(b), and 3(c), respectively. Note that since the GaAs substrate was cut an angle of 2° off the (100) plane, the (200) peak of GaAs was not observed, while the broad weak (400) peak was detected. In the as-deposited sample, only diffraction peaks corresponding to β–W are observed and no peaks corresponding to InAs are detected. This indicates that the InAs have an amorphous structure. After pre–annealing at 300 °C, the (111) InAs peak is detected. After high temperature annealing, the peaks corresponding to α–W, β–W and InAs are detected. The preferred crystal orientation relationship between the InAs and the GaAs is not observed, indicating that the InAs layer and the GaAs substrate do not react at this temperature. (Note that the R_c value of 1.2 Ω–mm was measured for this sample after annealing at 900 °C for 1 s, which indicates that the reaction between the InAs layer and the GaAs substrate occurred at

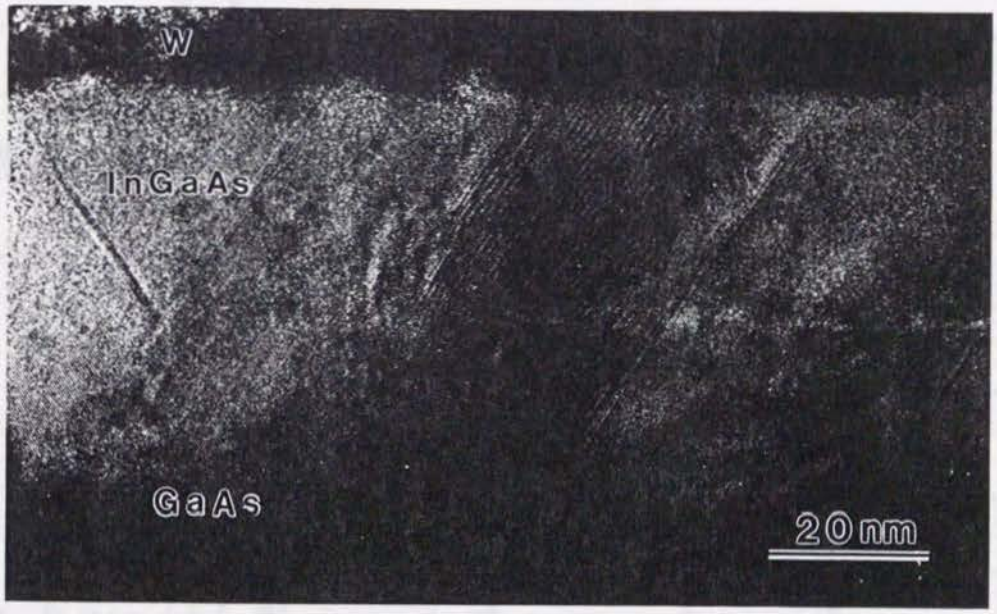


Fig. 3. 2 The XTEM micrograph of Sample D after annealing at 750 °C for 1 s by one–step annealing process.

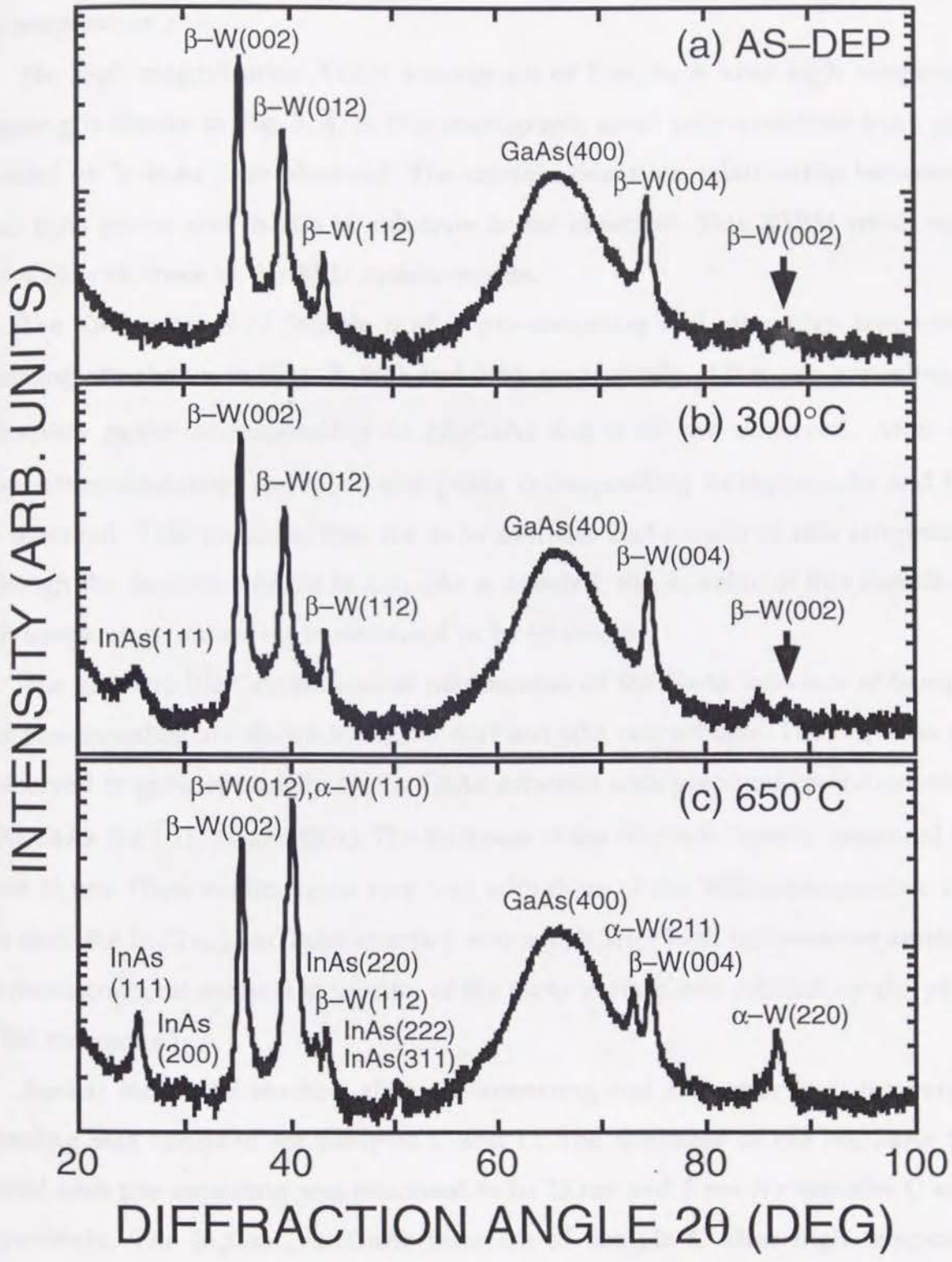


Fig. 3. 3 The XRD profiles of Sample A: (a) as–deposited, (b) after annealing at 300 °C for 30 min, and (c) after annealing at 650 °C for 1 s.

this temperature.)

The high magnification XTEM micrograph of Sample A after high temperature annealing is shown in Fig. 3. 4. In this micrograph, small polycrystalline InAs grains (denoted as "c–InAs") are observed. The crystal orientation relationship between the small InAs grains and the GaAs substrate is not observed. This XTEM result agrees very well with those of the XRD measurements.

The XRD profiles of Sample B after pre–annealing and after high temperature annealing are shown in Figs. 3. 5(a) and 5(b), respectively. After pre–annealing, the diffraction peaks corresponding to Ni_xGaAs and α–W are observed. After high temperature annealing, the diffraction peaks corresponding to $In_xGa_{1-x}As$ and NiAs are observed. This indicates that the InAs and the GaAs react at this temperature. Although the formation of the $In_xGa_{1-x}As$ is detected, the R_c value of this sample after high temperature annealing is measured to be 66 Ω–mm.

The low and high magnification microscopes of the GaAs interface of Sample B after pre–annealing are shown in Figs. 3. 6(a) and 6(b), respectively. The Ni_xGaAs layer is observed to grow epitaxially on the GaAs substrate with preferred crystal orientation of Ni_xGaAs $(10\bar{1}1)//GaAs$ (001). The thickness of the Ni_xGaAs layer is measured to be about 20 nm. These results agree very well with those of the XRD measurement. (Note that since the $In_xGa_{1-x}As$/GaAs interface was rough after high temperature annealing, the microstructural analysis at vicinity of the GaAs surface was difficult by the present XTEM technique.)

Similar interfacial reaction after pre–annealing and also after high temperature annealing was observed for Samples C and D. The thickness of the Ni_xGaAs layer formed after pre–annealing was measured to be 25 nm and 5 nm for Samples C and D, respectively. The $In_xGa_{1-x}As$/GaAs interface of Sample C after high temperature annealing was rough. The R_c value of Sample C after high temperature annealing was measured to be 2.1 Ω–mm. For Sample D, the $In_xGa_{1-x}As$/GaAs interface after high

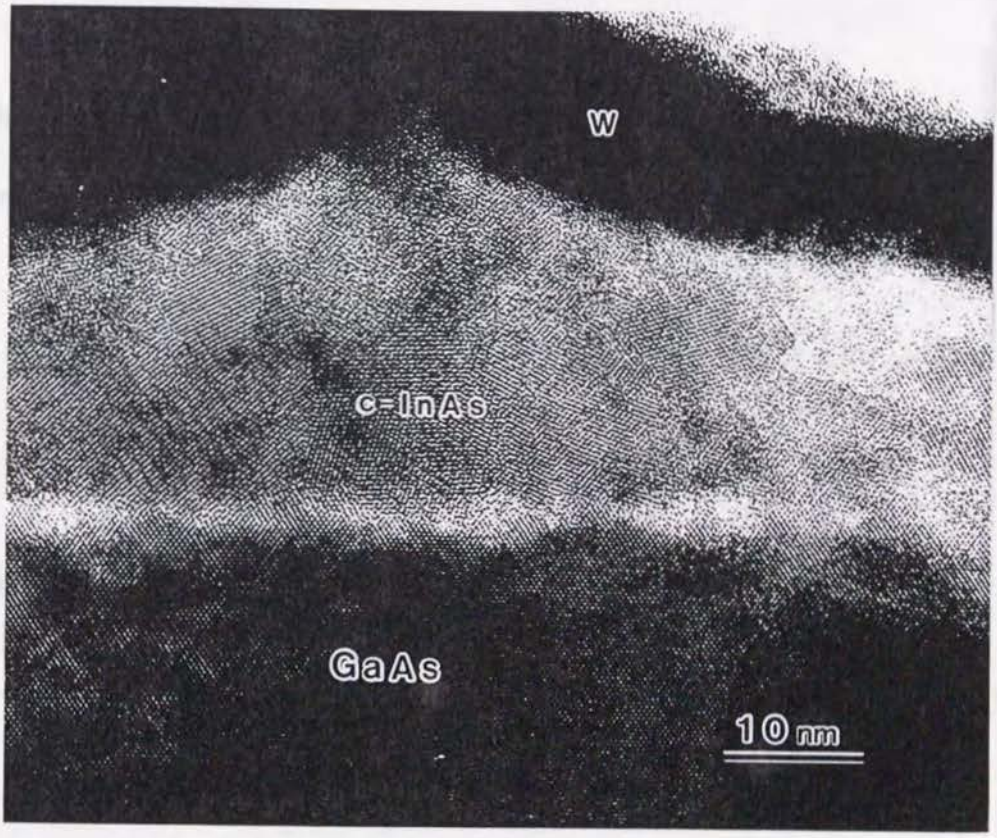


Fig. 3. 4 The XTEM micrograph of Sample A after annealing at 650 °C for 1 s.

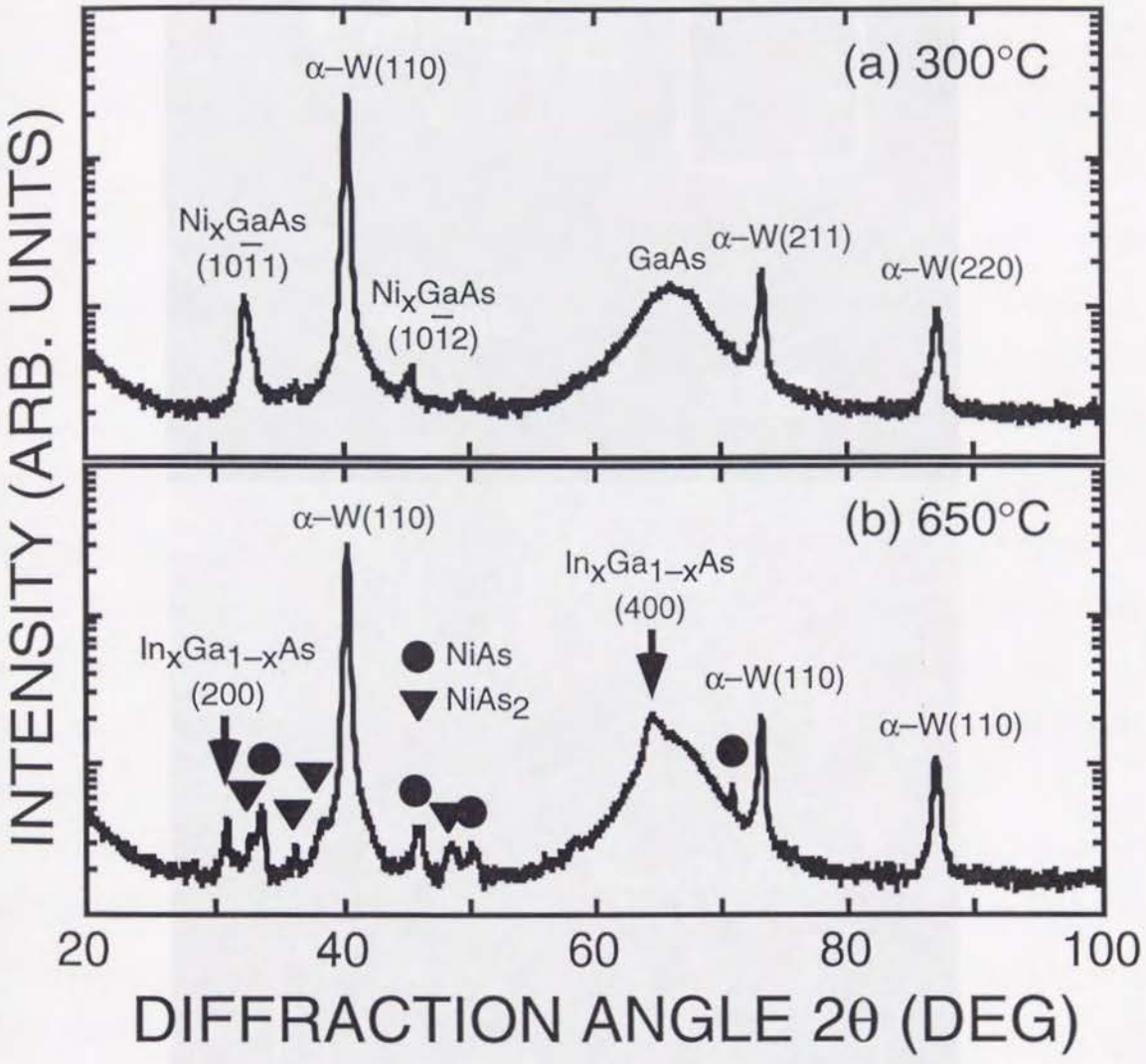


Fig. 3. 5 The XRD profiles of Sample B: (a) after annealing at 300 °C for 30 min and (b) after annealing at 650 °C for 1 s.

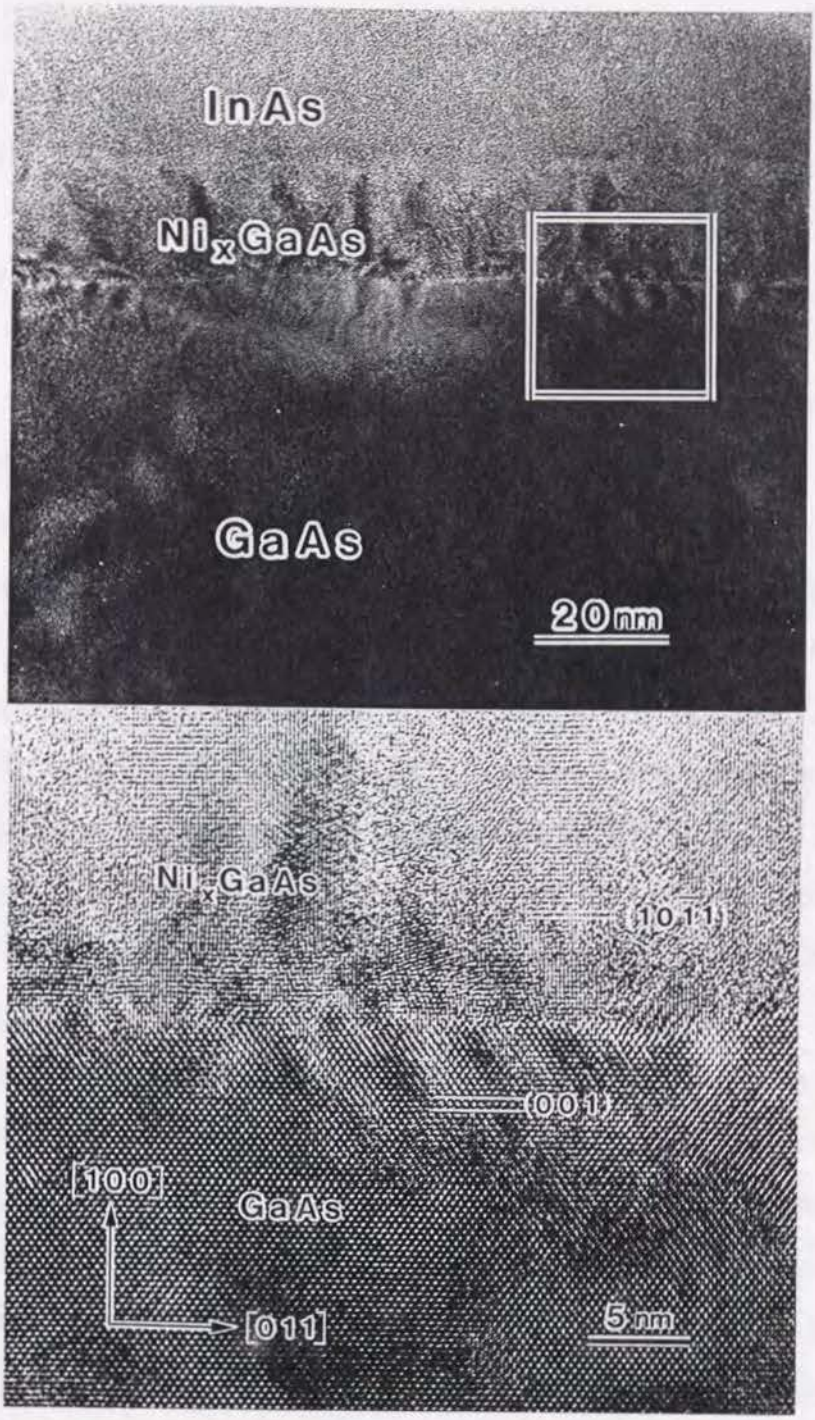


Fig. 3. 6 The XTEM micrograph of Sample B after annealing at 650 °C for 1 s : (a) low magnification and (b) high–resolution micrograph of $Ni_xGaAs/GaAs$ interface.

temperature annealing was smooth and the lowest R_c value of 0.3 Ω–mm was measured. The detail results of the microstructural analysis and the electrical measurements of Sample D will be shown in the next section.

Ohmic contact formation mechanism

The AES depth profiles of Sample D as–deposited, annealed at 300 °C for 7.5 min and 30 min, are shown in Figs. 3. 7(a), 7(b), and 7(c), respectively. In the as–deposited sample, interfaces between each layer of the InAs/Ni/W structure are clearly seen. However, it surprised us that the significant amounts of oxygen are incorporated in the W layer. After annealing at 300 °C for 7.5 min, Ni is found to diffuse toward the GaAs substrate through the InAs layer, and diffuse to the W layer. After subsequent annealing at 300 °C for 30 min, diffusion of Ni into the GaAs substrate is clearly seen.

The XTEM micrograph of Sample D annealed at 300 °C for 30 min is shown in Fig. 3. 8. In this micrograph, formation of crystalline NiAs compounds and existence of amorphous InAs are observed. Also, thin (~5 nm thick) Ni_xGaAs layers are observed to form on the GaAs surface.

The variations of lattice spacings of the $In_xGa_{1-x}As$ and Ni_xGaAs layers of Sample D are plotted on Figs. 3. 9(a) and 9(b), respectively, as a function of annealing temperatures. After annealing at 300 °C, the formation of Ni_3GaAs is detected. The composition of this compound shifts to the NiAs side with increasing the annealing temperature. This indicates that Ni_3GaAs are unstable at temperatures above 400 °C, and NiAs compounds are stable even at 800 °C. The amorphous InAs phase crystallizes at 550 °C. Note that at this temperature, Ohmic behavior was observed in this sample (Table 3. I). After annealing at higher temperature, the InAs reacts with GaAs and formed $In_xGa_{1-x}As$. The In composition (x) of the $In_xGa_{1-x}As$ layer after annealing at 750 °C was ~0.7. The lattice spacings of the top W layer did not change even after annealing at high temperatures.

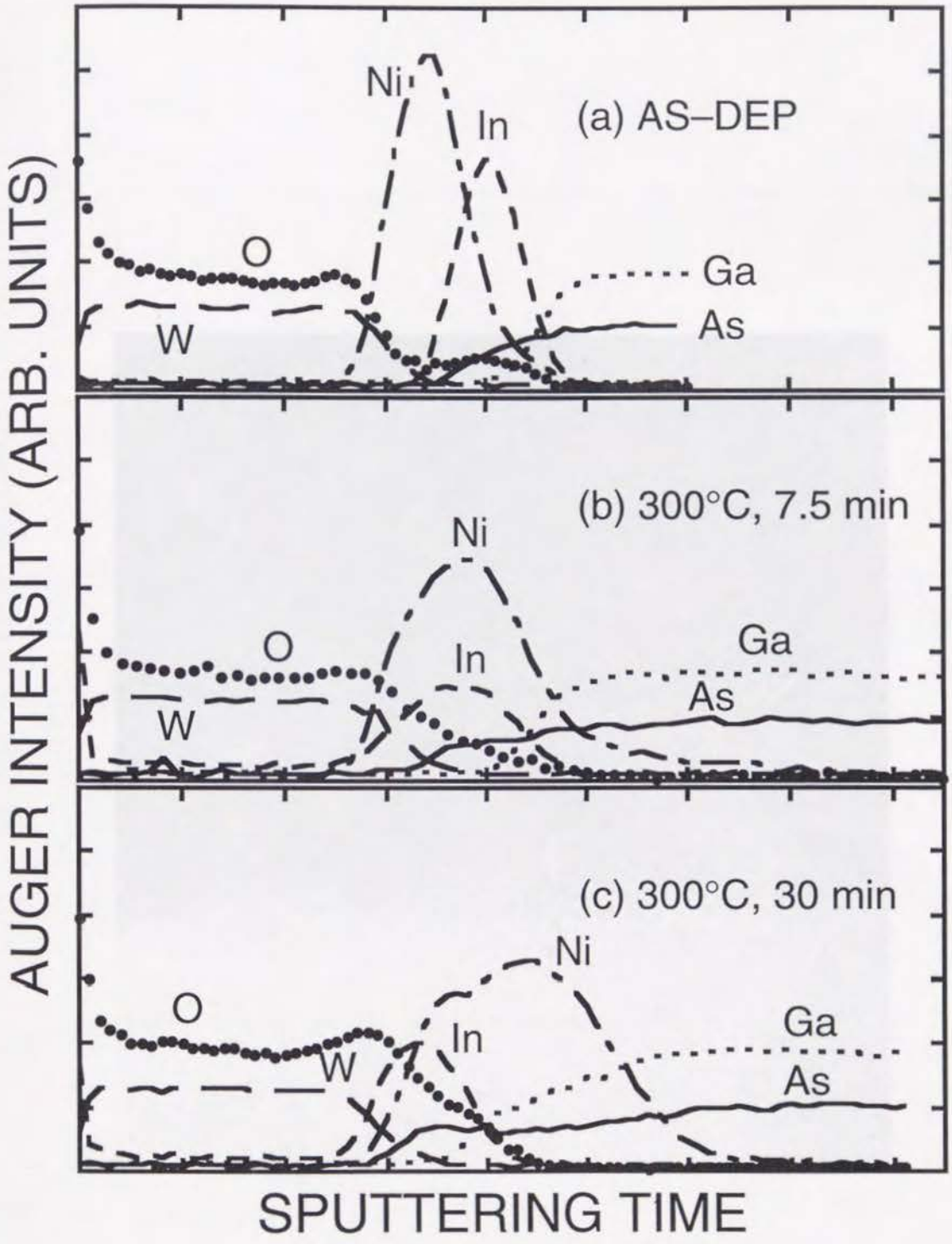


Fig. 3. 7 The AES profiles of Sample D: (a) as–deposited, (b) after annealing at 300 °C for 7.5 min, and (c) after annealing at 300 °C for 30 min.

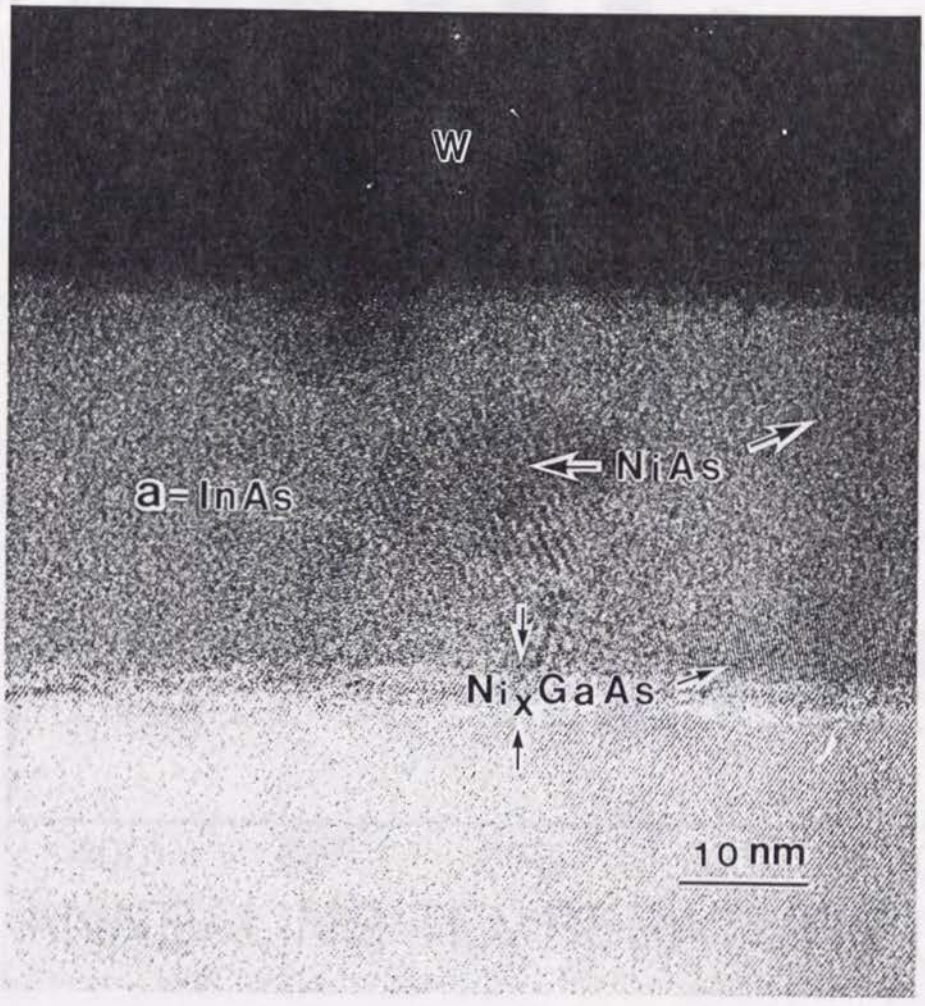


Fig. 3. 8 The XTEM micrograph of Sample D after annealing at 300 °C for 30 min.

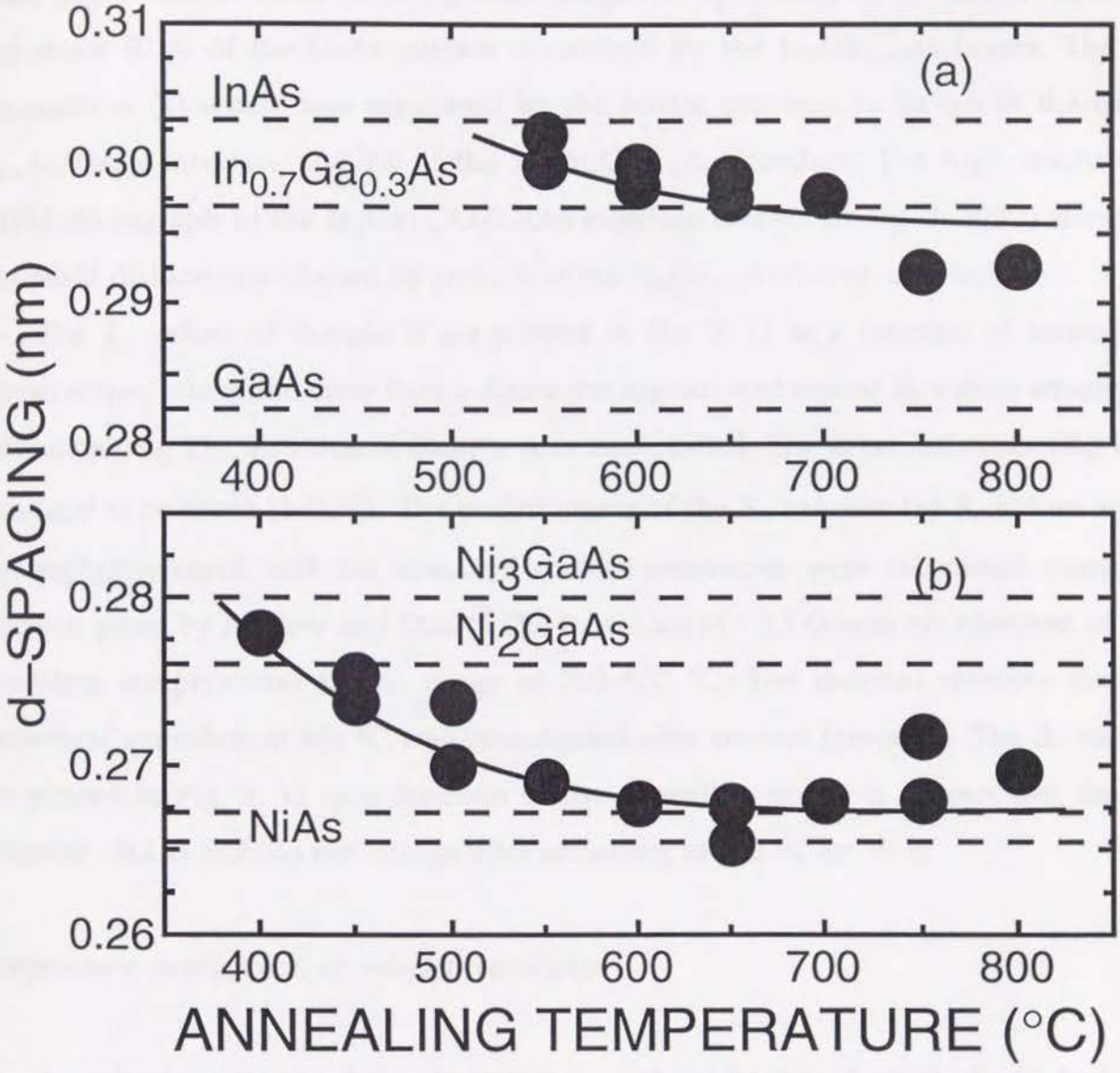


Fig. 3. 9 The variation of lattice spacings of (a) $In_xGa_{1-x}As$ and (b) Ni_xGaAs layers of Sample D during isochronal annealing.

The low magnification and high resolution XTEM micrographs of Sample D annealed at 750 °C for 1 s are shown in Figs. 3. 10(a) and 10(b), respectively. $In_xGa_{1-x}As$ phases with columnar grains are observed between the W layer and the GaAs substrate (Fig. 3. 10(a)). These ternary phases are grown epitaxially on the GaAs substrate and about 50 % of the GaAs surface is covered by the $In_xGa_{1-x}As$ layers. The In composition (x) which was measured by the lattice spacings to be 0.5 at the $In_xGa_{1-x}As$/GaAs interface and 1.0 at the W/$In_xGa_{1-x}As$ interface. The high resolution XTEM micrograph of the $In_xGa_{1-x}As$/GaAs interface (shown in Fig. 3. 10(b)) shows a few misfit dislocations (shown by arrows) at the $In_xGa_{1-x}As$/GaAs interface.

The R_c values of Sample D are plotted in Fig. 3. 11 as a function of annealing temperatures, where the error bars indicate the highest and lowest R_c values among 40 measurements. The R_c value of Sample A is also plotted. The sheet resistance (R_s) was measured to be about 11 Ω/□. The contributions of the R_s value to the R_c values were not negligibly small, and the measured contact resistances were subtracted using an equation given by Marlow and Das. [13] The R_c values of ~0.3 Ω–mm are obtained at the annealing temperatures in the range of 700–800 °C. The thermal stability during isothermal annealing at 400 °C was investigated after contact formation. The R_c values are plotted in Fig. 3. 12 as a function of the annealing times. It is seen that the R_c values of ~0.4 Ω–mm do not change after annealing at 400 °C for 10 h.

Temperature dependence of contact resistance

In order to understand the electron transport mechanism through the GaAs/contact metal interface of the InAs/Ni/W contact, the R_c values were measured at low temperatures and these values are plotted in Fig. 3. 13 as a function of the measured temperatures. Since the R_c values measured after wire bonding were about three times larger than those measured before bonding, the measured R_c values are plotted after reducing the measured R_c values by a factor of three. The reason of the deterioration

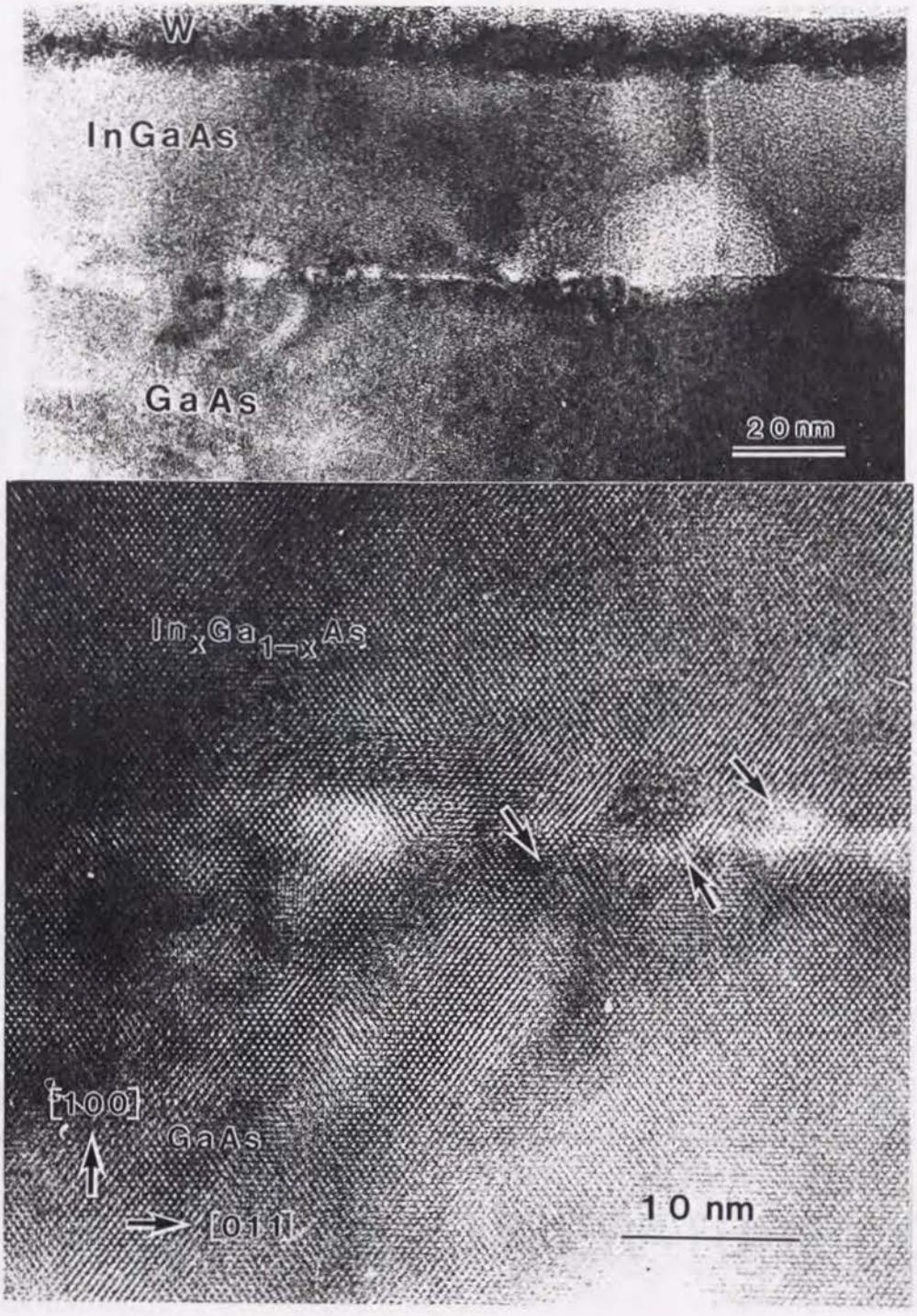


Fig. 3. 10 (a) Low magnification and (b) high resolution XTEM micrograph of Sample D after annealing at 750 °C for 1 s by two–step annealing process.

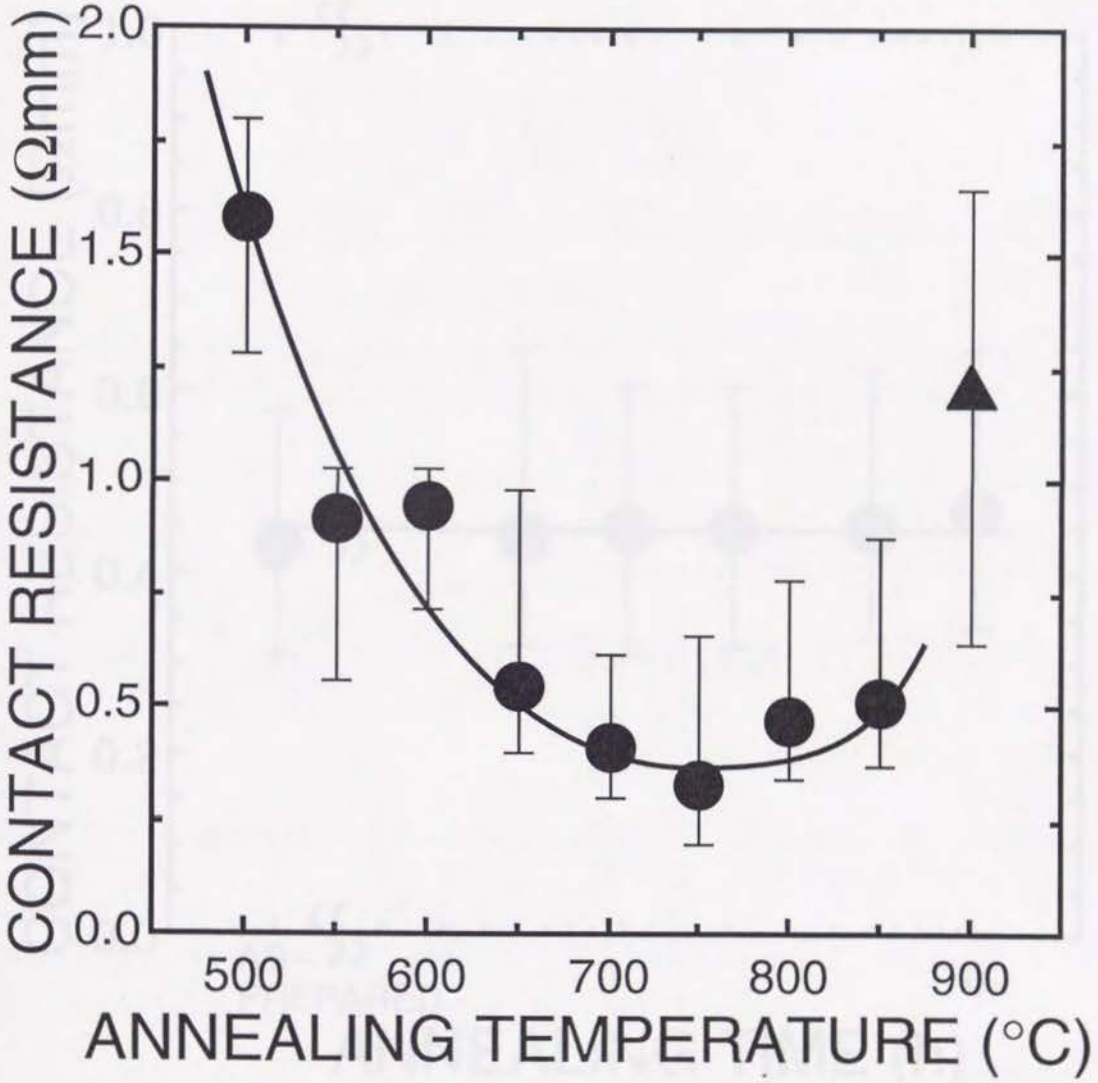


Fig. 3. 11 Contact resistances of Sample A (▲)and Sample D (●)annealed at various temperatures by RTA for 1 s.

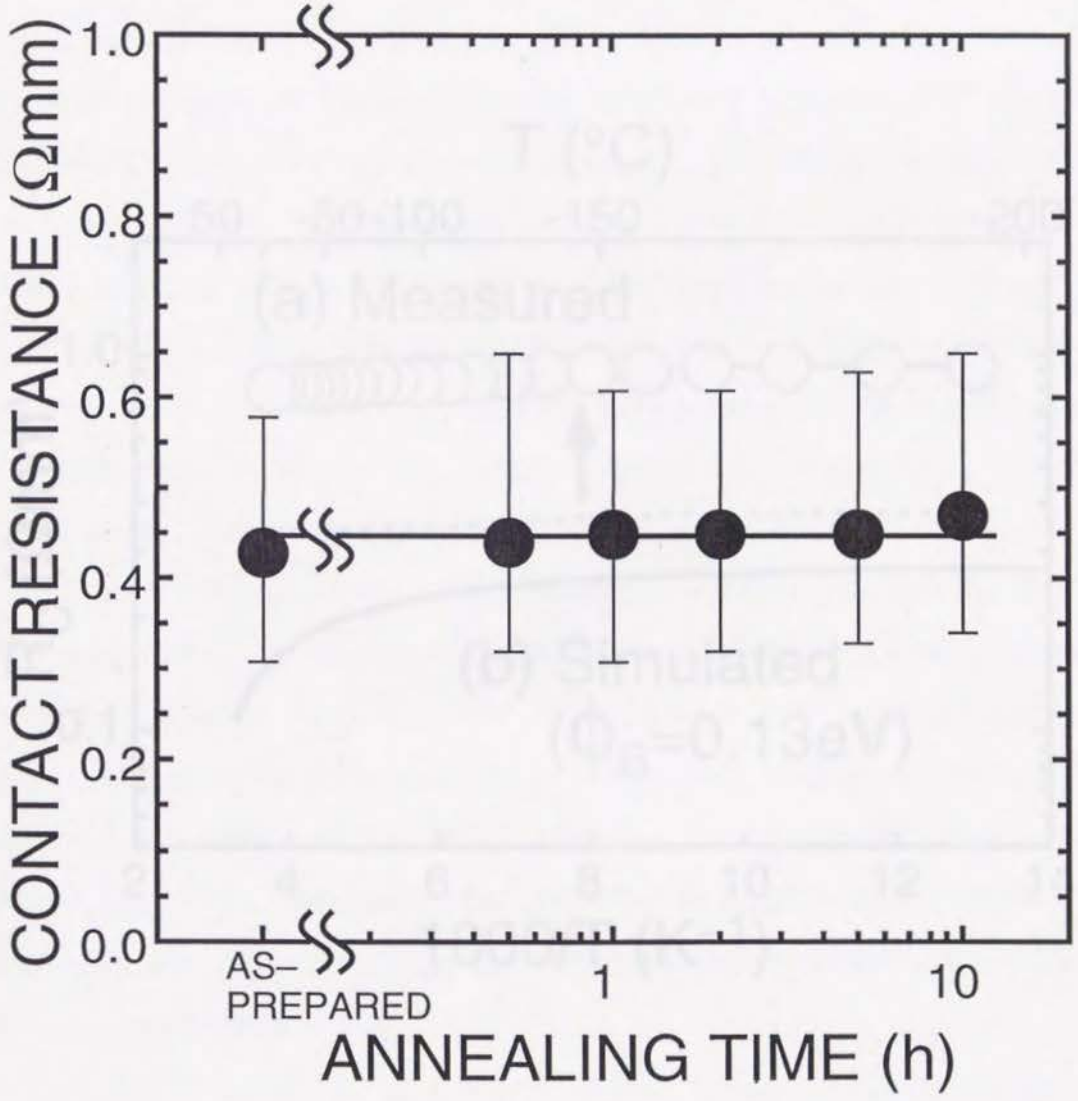


Fig. 3. 12 Contact resistances of Sample D during isothermal annealing at 400 °C.

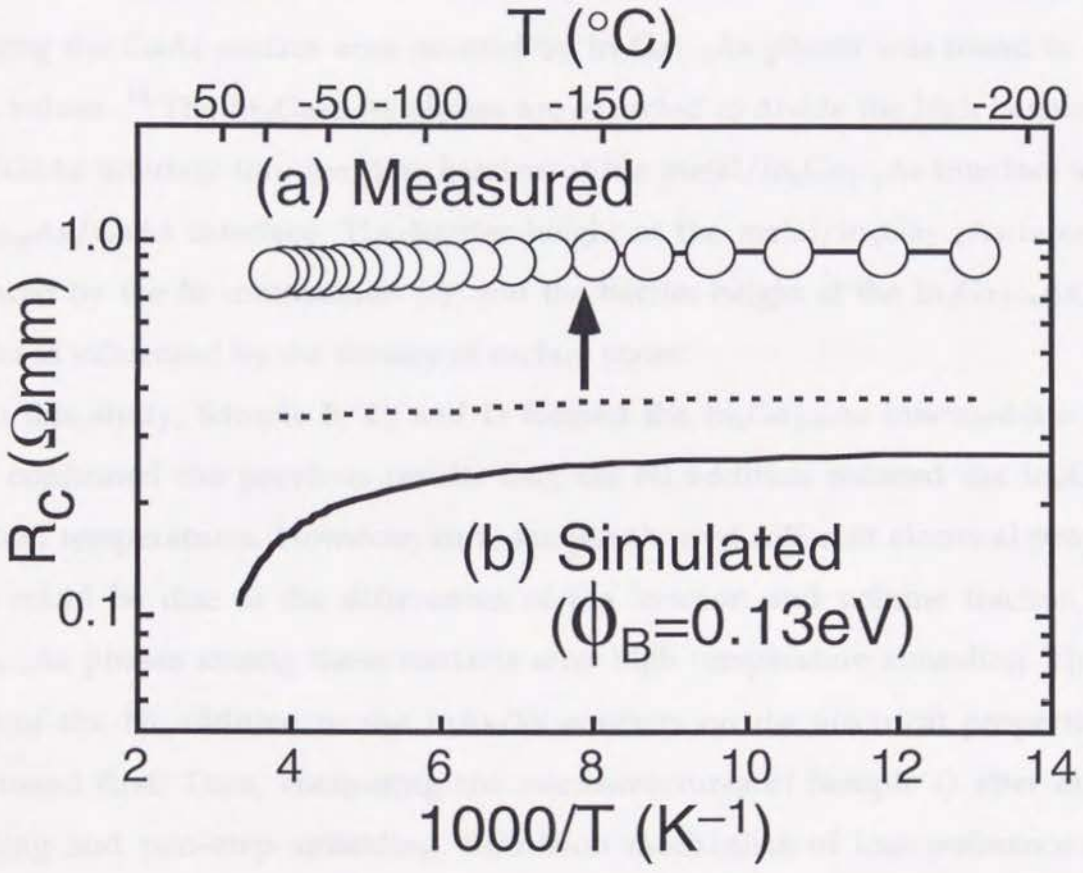


Fig. 3. 13 The contact resistances at various temperatures: (a) the measured contact resistances of the InAs/Ni/W contacts and (b) the calculated contact resistances with the effective barrier of ϕ_B=0.13 eV.

of the R_c values after bonding is not understood at the moment. The R_c of 0.3 Ω–mm measured at 27 °C increased slightly to 0.4 Ω–mm at –196°C. The carrier transport mechanism analysis based on these data will be carried out later.

3.1.4 Discussion

It was reported that the formation of $In_xGa_{1-x}As$ phases at the metal/GaAs interface was essential to convert Schottky to Ohmic behavior. [14–16] In addition, increasing the GaAs surface area covered by $In_xGa_{1-x}As$ phases was found to reduce the R_c values. [14] The $In_xGa_{1-x}As$ phases are expected to divide the high barrier at the metal/GaAs interface into two low barriers at the metal/$In_xGa_{1-x}As$ interface and the $In_xGa_{1-x}As$/GaAs interface. The barrier height at the metal/$In_xGa_{1-x}As$ interface is influenced by the In composition (x), and the barrier height at the $In_xGa_{1-x}As$/GaAs interface is influenced by the density of surface states.

In this study, Sample B, C, and D formed the $In_xGa_{1-x}As$ intermediate phases which confirmed the previous results that the Ni addition reduced the $In_xGa_{1-x}As$ formation temperatures. However, each sample showed different electrical properties, which could be due to the differences of the location and volume fraction of the $In_xGa_{1-x}As$ phases among these contacts after high temperature annealing. Thus, the effects of the Ni addition to the InAs/W contacts on the electrical properties will bediscussed first. Then, comparing the microstructures of Sample D after one–step annealing and two–step annealing, formation mechanism of low resistance Ohmic contacts will be discussed.

Role of Ni addition to InAs/W contacts

$In_xGa_{1-x}As$ forms solid solution between InAs and GaAs by annealing at temperatures below 940 °C. However, the low temperature reaction is not easy in case when a

thin oxide layer exists at the interface between the InAs and the GaAs substrate, because the melting points of InAs (~942 °C) and GaAs (~1238 °C) are relatively high. An addition of Ni to the InAs–based contact was reported to reduce the contact formation temperature. [14] It was found that Ni diffused to the GaAs substrate and formed a Ni_xGaAs layer at relatively low temperature (below 400 °C), and that this Ni_xGaAs layer decomposed to NiAs and NiGa at temperatures above 400 °C. [17, 18] Therefore, when the Ni_xGaAs grows on the GaAs substrate, a large area of the GaAs surface is covered by the NiAs and/or NiGa layer after high temperature annealing, leading to reduction of the total area of the GaAs surface covered by $In_xGa_{1-x}As$, which causes an increase to the contact resistances.

The relationship among the thicknesses of the Ni_xGaAs layer after pre-annealing, the percentages of the GaAs surface covered by the $In_xGa_{1-x}As$ layer after annealing at 650 °C, and the contact resistances obtained in this study are summarized in Table 3. II for Samples B, C, and D, respectively. The cross sections of the interfacial microstructures of Samples B and D are shown in Figs. 3. 14(a) and 14(b), respectively. These figures are deduced from XRD and TEM results. For Sample B, since the Ni_xGaAs layer with 20 nm thickness formed after preannealing. A large area of the GaAs surface is believed to be covered by the NiAs layer upon heating at 650 °C which was formed by decomposition of the Ni_xGaAs. By using the R_c value of 66 Ω–mm, the total area of the GaAs surface covered by $In_xGa_{1-x}As$ is estimated to be nearly zero based on the previous result by Murakami *et al.* [14] Note that since the $In_xGa_{1-x}As$ /GaAs interface of this sample was rough, the total area of the GaAs surface covered by $In_xGa_{1-x}As$ could not be measured by the present XTEM observation. The rough $In_xGa_{1-x}As$/GaAs interface of the sample is believed to be due to the formation and the decomposition of the large amounts of Ni_xGaAs. Although $In_xGa_{1-x}As$ layers were detected by XRD after high temperature annealing, this layer are believed to be formed by reaction between the InAs and the NiGa because NiGa was not detected by the XRD measurement of Fig. 3. 5(b).

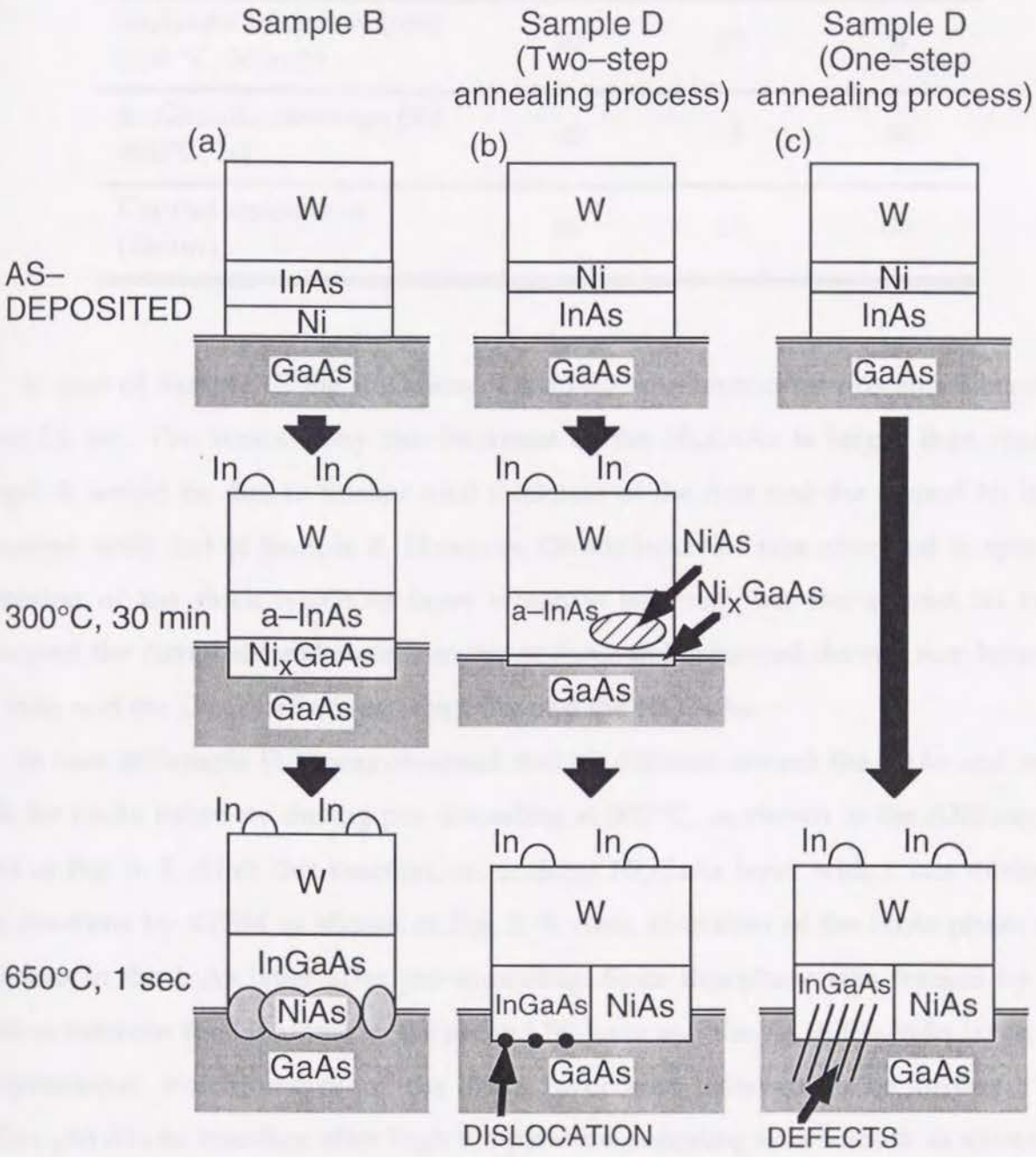


Fig. 3. 14 Schematic illustrations of interfacial reaction: (a) Sample B with two–step annealing process, (b) Sample D with two–step annealing process, and (c) Sample D with one–step annealing process.

Table 3. II. Thickness of Ni_xGaAs, $In_xGa_{1-x}As$ coverages on the GaAs substrate, and the contact resistances of Samples B, C, and D

Sample Number	B	C	D
Ni_xGaAs thickness (nm) (300 °C, 30 min)	20	25	5
$In_xGa_{1-x}As$ coverage (%) (650°C, 1s)	~0	~0	50
Contact resistances (Ωmm)	66	2.1	0.3

In case of Sample C, the thickness of the Ni_xGaAs layer after pre–annealing was about 25 nm. The reason why the thickness of the Ni_xGaAs is larger than that of Sample B would be due to thicker total thickness of the first and the second Ni layer compared with that of Sample B. However, Ohmic behavior was observed in spite of formation of the thick Ni_xGaAs layer which is believed that the second Ni layer destroyed the compositional stoichiometry of InAs and enhanced the reaction between the InAs and the GaAs or between the InAs and the Ni_xGaAs.

In case of Sample D, it was observed that Ni diffused toward the GaAs and react with the GaAs substrate during pre–annealing at 300 °C, as shown in the AES experiment of Fig. 3. 7. After this reaction, an uniform Ni_xGaAs layer with 5 nm thickness was observed by XTEM as shown in Fig. 3. 8. Also, formation of the NiAs phase was observed in the InAs layer after pre–annealing. Since this phase was formed by the reaction between the Ni atoms in the second Ni layer and the As in the InAs layer, the compositional stoichiometry of the InAs layer was believed to be broken. The $In_xGa_{1-x}As$/GaAs interface after high temperature annealing was smooth as shown in Fig. 3. 10(a), because a thin Ni_xGaAs layer was formed after pre–annealing. In addition, the wide area of the GaAs surface was covered by the $In_xGa_{1-x}As$/GaAs interface, because the unstoichiometric InAs was reactive with the GaAs substrate. Since half of

the GaAs surface was covered with the smooth $In_xGa_{1-x}As$/GaAs interface, the R_c value of 0.3 Ω–mm was obtained.

Formation mechanism of InAs/Ni/W contact

As listed in Table 3. I, Sample D which was prepared by two–step annealing process showed Ohmic behavior. The result indicates that the annealing process had an important role in forming low resistance Ohmic contacts. In this section, differences of the microstructures of Sample D prepared by the "one" or "two–step" process are discussed.

The cross sections of the interfacial microstructures of the contacts prepared by the "two–step" and "one–step" annealing processes are shown in Figs. 3. 14(b) and 14(c), respectively. The sample prepared by one–step process had a high density of stacking faults in the $In_xGa_{1-x}As$ layer and at the $In_xGa_{1-x}As$/GaAs interface as observed in Fig. 3. 2. It was previously reported when As atoms segregated at the crystal defects, such as dislocations and stacking faults, and the fermi–level of the GaAs would be pinned at the mid–point of the GaAs energy gap. [19] This pinning would increase the barrier height between the $In_xGa_{1-x}As$ and GaAs, resulting in an increase of the R_c values. In addition, a high density of the defects in the $In_xGa_{1-x}As$ layer would increase the channel resistance, which also results in an increase of the R_c values. These defects are induced by the stress due to the "instantaneous" reaction between the GaAs substrate and the amorphous InAs layer thorough the oxide layer upon annealing by RTA. The reduction of the defects is essential to reduce the R_c values of Sample D.

For the sample which is prepared by two–step process, a thin Ni_xGaAs layer was grown on the GaAs substrate at the initial stages of pre–heating at 300 °C, where InAs had an amorphous structure (denoted as "a"). Also formation of NiAs compounds which had polycrystalline structure was observed at this temperature. The InAs layer

crystallized at temperatures above 550 °C. After subsequent annealing at 750 °C, $In_xGa_{1-x}As$ and NiAs layers with columnar structures were observed between the GaAs substrate and the W layer as shown in Fig. 3. 10(a). The $In_xGa_{1-x}As$ layer was formed by the reaction of the GaAs substrate and the crystallized InAs. Since the oxide layer on the GaAs substrate was removed during pre–heating by forming thick Ni_xGaAs, the InAs and GaAs reaction was not intervened by the oxide layer and the "gradual" reaction might occur during heating at 750 °C. Thus, the stress induced by the reaction was considered to be relaxed, leading to reduction of the defect density at the $In_xGa_{1-x}As$ and GaAs interface. In the previous experiments, Kim *et al.* [4] prepared low resistance Ohmic contacts without "intentional" pre–heating. However, they coated the contact metals with a Si_3N_4 layer by chemical vapor deposition in order to prevent out–diffusion of As from the GaAs substrate during contact formation. This coating process required the contacts to heat at 300 °C for 30 min, which turned out to be an essential heat treatment for the Ohmic contact formation.

As shown in Figs. 3. 7(b) and 7(c), In diffused to the W layer and condensed on the W surface. This In diffusion to the W layer deteriorates the surface roughness and reduces the In composition in the $In_xGa_{1-x}As$ layer, resulting the increase of the contact resistance. In addition, since the amount of In which diffused to the W cannot be controlled, run–to–run variation of the R_c values is large. In order to improve the electrical properties and reproducibility of the present contacts, an experiment to prevent the In diffusion is necessary.

Current transport mechanism of $In_xGa_{1-x}As$–based contact

The epitaxial growth of the $In_xGa_{1-x}As$ layer on the GaAs substrate was found to be essential to convert the I–V characteristics of the metal/n–GaAs contacts from Schottky behavior to Ohmic behavior by previous studies. [4, 20] In such the contacts two barriers exist at the metal/$In_xGa_{1-x}As$ interface and at the $In_xGa_{1-x}As$/GaAs interface,

and the R_c values are determined by the higher barrier between the two. Their barrier heights are determined by the In concentration (x) in the $In_xGa_{1-x}As$ layers and the percentage of the GaAs interface covered by the $In_xGa_{1-x}As$ layers. The correlation between the R_c values and the percentage of the GaAs interface covered by the $In_xGa_{1-x}As$ layers was extensively studied and it was found that the R_c values are almost constant when more than 50 % of the GaAs interface is covered by the $In_xGa_{1-x}As$ layers. [14]

In the present study, the distribution (normal to the contact surface) of the In concentrations (x) in the $In_xGa_{1-x}As$ layers was measured by TEM [Fig. 3. 10(b)]. To prepare Ohmic contacts with low Rc by sputtering the InxGa1–xAs targets, the low In concentration (x) is desirable at the $In_xGa_{1-x}As$/GaAs interface so that the lattice mismatch at the interface is small. From the present result, the x value at the $In_xGa_{1-x}As$/GaAs interface was about 0.5, and 1.0 at the metal/$In_xGa_{1-x}As$ interface. However, the effective barrier cannot be determined by these lattice spacings data.

In order to evaluate the effective barrier height, the contact resistances were calculated using an equation given by Yu, [21] where the Richardson constant A of 8.06 $A/cm^2/K^2$ and the ionized donor concentration N_D^+ of 2×10^{18} cm^{-3} were used. Since the Si impurity level (E_D) is sufficiently shallow (E_D=5.8 meV) compared with the activation energy of the electron, the N_D^+ value was assumed to be constant in the range of -196 °C to 27 °C. In order to compare the experimental values, the specific contact resistivities (R'_c) in the unit of Ωcm^2 were converted to the contact resistances (R_c) in the unit of Ω–mm through an equation of $R_c=\sqrt{R'_c R_{ch}}$, assuming the sheet resistance in the channel of the semiconductor being equal to the sheet resistance under the contacts. [22] In the InAs/Ni/W contacts, since the GaAs surface is covered by the NiAs phase and the $In_xGa_{1-x}As$ phase, the measured R_c values are calculated by the total current through the NiAs/GaAs interface (which shows high contact resistance (R_{high})) and the $In_xGa_{1-x}As$/GaAs interface (which shows low contact

resistance (R_{low})). However, when the difference between the low R_c value and the high R_c value is large, the properties of the measured R_c value is dominated by the properties of the current through the lower R_c interface. Therefore, the effective barrier was estimated from the slope of the R_c vs. T plots. The contact resistances, calculated by assuming the dominant carrier transport mechanism being field emission (FE), are plotted by a solid curve in Fig. 3. 13, where the effective barrier height of 0.13 eV was used. The slope of the measured R_c curve fits very well with that of the theory at the temperature range between 77K and 180 K. However, the calculated contact resistances showed lower values than these experimental values at the temperature range between 180 K and 300 K. The transport mechanism may shange from FE to TFE at this temperature region. In addition, the measured R_c values are about 1.5 times higher than that of the simulated values, because only 50 % of the GaAas surface is covered by the low R_c interface ($In_xGa_{1-x}As/GaAs$). Therefore, further reduction of the contact resistances is expected by increasing the contact area of the low R_c interface.

The band diagrams of the metal/GaAs contact and the metal/$In_xGa_{1-x}As$/GaAs contact are schematically shown in Fig. 3. 15. The ϕ_b value depends on the In concentration (x) in the $In_xGa_{1-x}As$ phases (ϕ_b=0.8 eV for x=0 and ϕ_b=–0.05 eV for x=1), [23] and ϕ_b is close to zero when the x value is greater than 0.8. The ϕ_c value also depends on the In concentration in the $In_xGa_{1-x}As$ phases. In this study, the In composition (x) in the $In_xGa_{1-x}As$ was measured to be x=1 at the metal interface and x=0.5 at the GaAs interface by the previous XTEM observation. [20] Therefore, the effective barrier height of 0.13 eV evaluated in the present calculation would correspond to the barrier height at the $In_xGa_{1-x}As/GaAs$ interface (ϕ_c).

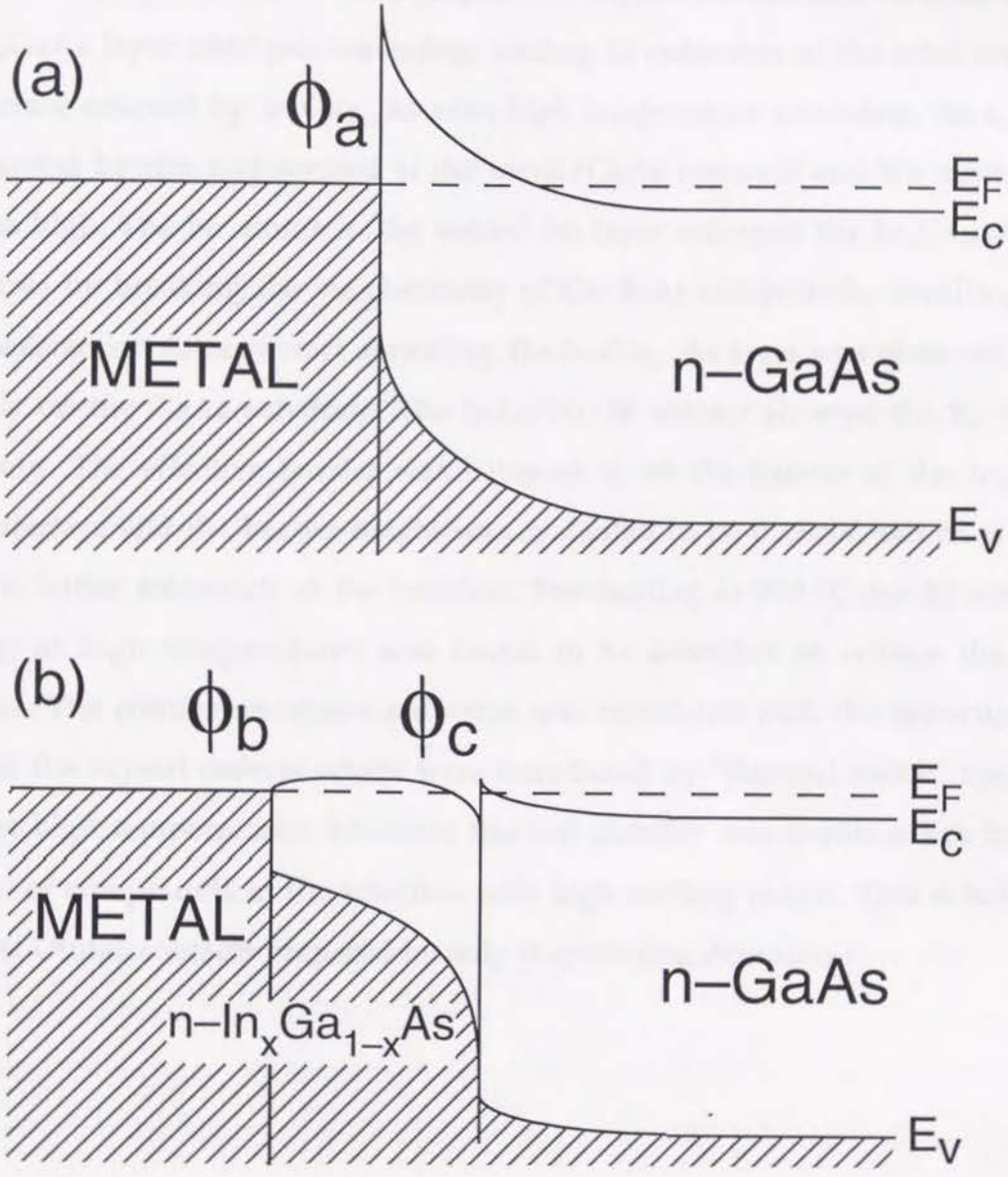


Fig. 3. 15 Energy band diagrams of (a) metal/n–GaAs interface and (b) metal/$In_xGa_{1-x}As$/n–GaAs contact.

3.1.5 Conclusion

The effects of the Ni addition to the InAs/W contacts on the interfacial reaction between the InAs and the GaAs substrate were studied by analyzing the microstructure of the contacts prepared with various deposition sequences. The first Ni layer formed a thick Ni_xGaAs layer after pre–annealing, leading to reduction of the total area of the GaAs surface covered by $In_xGa_{1-x}As$ after high temperature annealing. As a result, a high potential barrier was formed at the metal/GaAs interface and the contact resistance was high. The Ni atoms in the second Ni layer enlarged the $In_xGa_{1-x}As$/GaAs contact area by breaking the stoichiometry of the InAs compounds, resulting in low contact resistances. After contact annealing, the $In_xGa_{1-x}As$ layer was observed to grow epitaxially on the GaAs substrate. The InAs/Ni/W contact showed the R_c values of ~0.3 Ω–mm. The effective barrier was believed to be the barrier at the $In_xGa_{1-x}As$ /GaAs interface and the barrier height was evaluated to be 0.13 eV, which is induced by the 4% lattice mismatch at the interface. Pre–heating at 300 °C for 30 min before annealing at high temperatures was found to be essential to reduce the contact resistances. The contact resistance reduction was correlated with the reduction in the density of the crystal defects which were introduced by "thermal shock" upon quick heating at high temperatures. Excellent thermal stability was explained to be due to formation of compounds at the interface with high melting points. This is believed to be the first Ohmic contacts prepared by only rf sputtering deposition.

3.2 Development of $In_{0.7}Ga_{0.3}As$/Ni/W contact

3.2.1 Introduction

In Section 3. 1, the InAs/Ni/W Ohmic contacts with low resistances were prepared by rf sputter–deposition. It was found that the second Ni layer enlarged the $In_xGa_{1-x}As$/GaAs contact area by breaking the stoichiometry of the InAs compounds, resulting in low contact resistance (R_c). In addition, pre–annealing (300 °C for 30 min) prior to high temperature annealing was found to be essential to prepare low resistance Ohmic contact. However, the optimum temperature to prepare the lowest contact resistance was about 750 °C, which is too high to use this fabrication process in the manufacturing devices. Also, the surface morphology of this contact was rough, which was caused by In out–diffusion through the W top layer annealing at high temperature, although the amounts of In were small. Reduction of the optimum annealing temperature for low R_c is essential for application of this contact to manufacturing devices.

In addition, the In composition x at the metal/$In_xGa_{1-x}As$ interface and at the InxGa1–xAs/metal interface was correlated with the Rc value. The effective barrier to dominate the Rc value was evaluated to be 0.13 eV at the $In_xGa_{1-x}As$/GaAs interface, because the x value at the metal/$In_xGa_{1-x}As$ interface was larger than 0.8. However, the optimum distrubution of the In composition in the $In_xGa_{1-x}As$ layer to prepare low contact resistance was not understood.

The main purpose of this section is twofold. The first is to reduce the optimum temperature for low R_c and to improve the surface morphology of the previously developed rf sputter-deposited Ohmic contacts. For this purpose, $In_xGa_{1-x}As$ targets instead of the InAs target was used, where the In concentration (x) is 0.4 or 0.7. The samples were prepared by pre-annealing at 300 °C for 30 min and annealing at temperatures in the range of 400 to 800 °C for 1 s by a rapid thermal annealer (RTA). The

contact resistances were measured by TLM [12] and the microstructures of the contacts were analyzed by XRD, Rutherford backscattering spectometry (RBS) and XTEM. The second is to understand the optimum In composition in the $In_xGa_{1-x}As$ layer to prepare low Rc. For this purpose, Rc values of the $In_xGa_{1-x}As$/Ni/W contacts (x=1, 0.7 and 0.4) were correlated with the In composition at the metal/$In_xGa_{1-x}As$ interface and at the $In_xGa_{1-x}As$/GaAs interface.

3.2.2 Experimental Procedure

The $In_xGa_{1-x}As$/Ni/W samples were sequentially deposited by the rf sputtering technique and the samples used in the present experiment are schematically shown in Fig. 3. 16. The $In_xGa_{1-x}As$ layers were sputter-deposited by Ar using $In_{0.7}Ga_{0.3}As$ and $In_{0.4}Ga_{0.6}As$ targets. The deposition rate was about 0.1 nm/s. The In, Ga and As compositions in the $In_xGa_{1-x}As$ layers were analyzed by electron probe micro analysis (EPMA), and the In:Ga:As ratios of the targets and the deposited films are shown in Fig. 3. 17. The solid lines show the In and Ga compositions, respectively, of the targets and the films in case the compositions in both the targets and films are equal. The circles and squares show the measured In and Ga compositions, respectively. It is noted that the compositions in the films are close to those in the targets within experimental errors. The Ni and W layers were subsequently sputter-deposited. The thicknesses of $In_xGa_{1-x}As$, Ni and W layers of the samples used in the present experiment are listed in Table 3. III.

Microstructural analysis were carried out for the samples before and after annealing using XRD and TEM. Distribution of the In atoms was measured by RBS, where the $^4He^{2+}$ ions were accelerated with 2 MeV and 50–100nA, and the scattered ions were measured at a scattering angle of 170°. The surface morphology of samples were observed by the optical microscope.

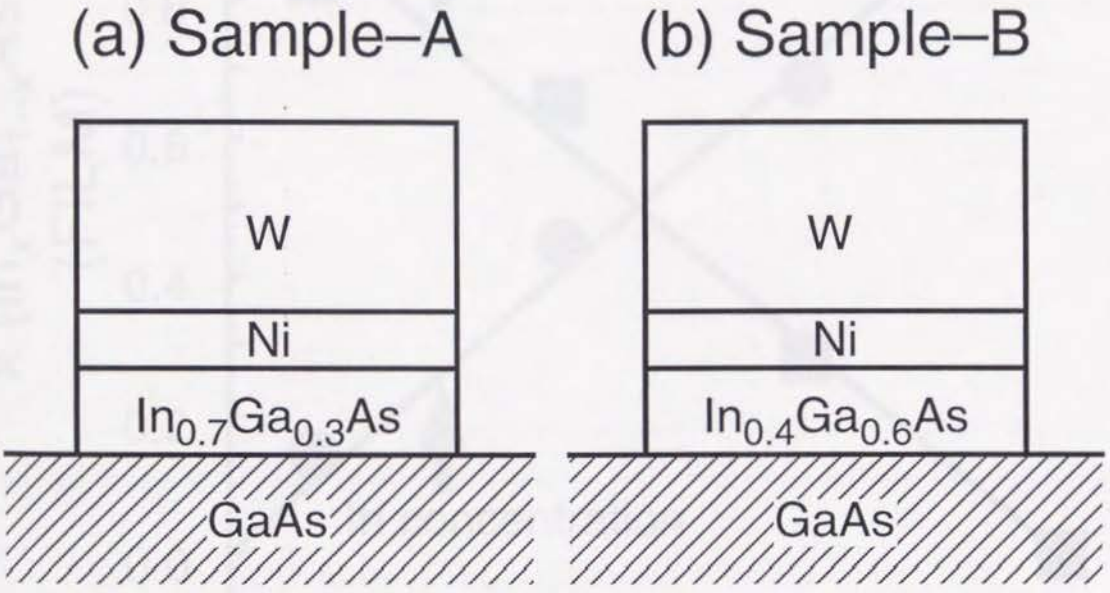


Fig. 3. 16 Cross sections of (a) $In_{0.7}Ga_{0.3}As$/Ni/W and (b) $In_{0.4}Ga_{0.6}As$/Ni /W contacts.

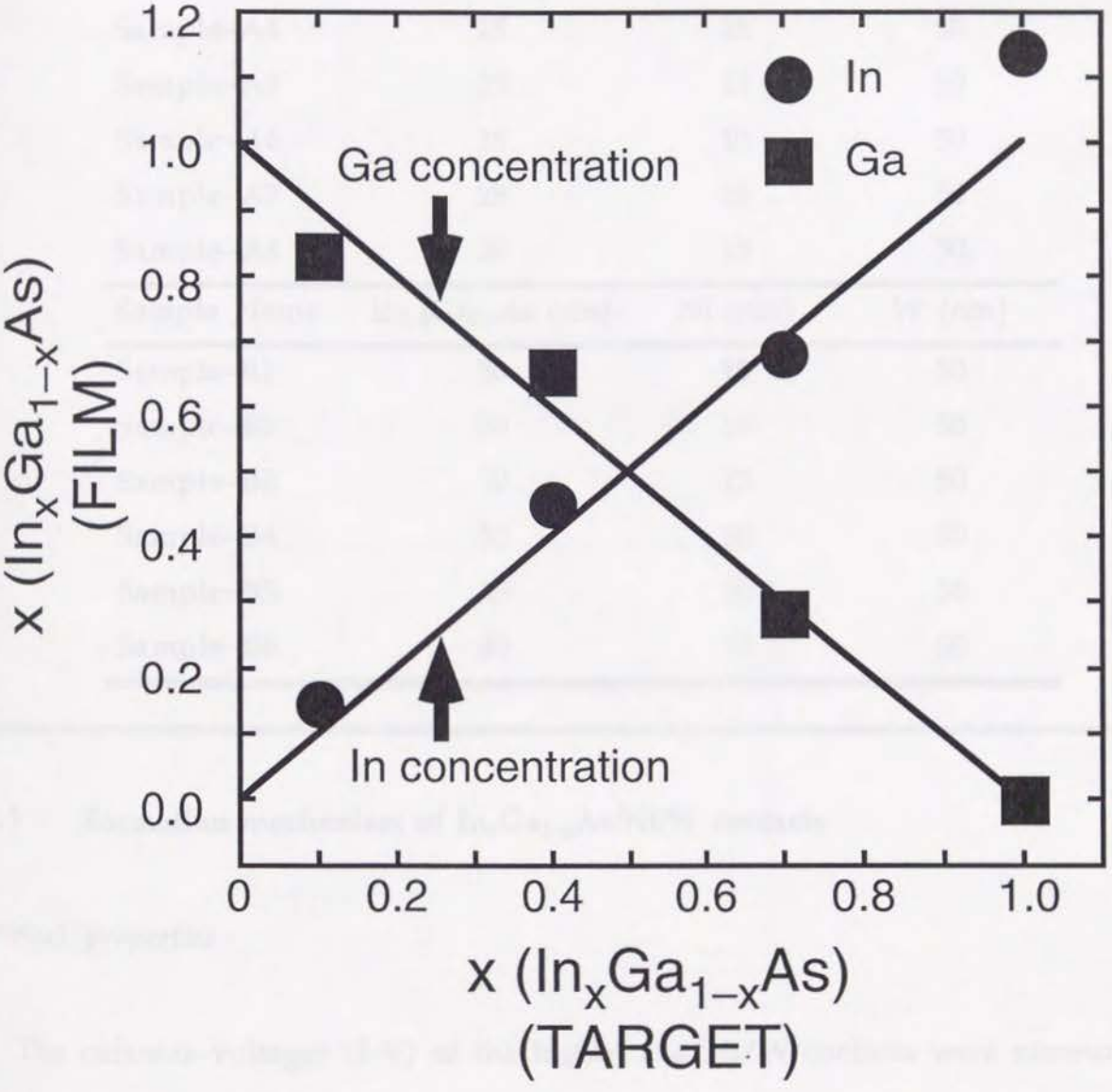


Fig. 3. 17 Compositional relation of In:Ga:As ratios between the targets and the deposited films.

Table 3. III. InGaAs, Ni, W thickness used in the present experiment.

Sample Name	$In_{0.7}Ga_{0.3}As$ (nm)	Ni (nm)	W (nm)
Sample–A1	20	15	50
Sample–A2	23	15	50
Sample–A3	25	18	50
Sample–A4	25	15	50
Sample–A5	25	13	50
Sample–A6	25	10	50
Sample–A7	28	15	50
Sample–A8	30	15	50
Sample Name	$In_{0.4}Ga_{0.6}As$ (nm)	Ni (nm)	W (nm)
Sample–B1	20	15	50
Sample–B2	30	10	50
Sample–B3	30	15	50
Sample–B4	30	20	50
Sample–B5	35	20	50
Sample–B6	40	15	50

3.2.3 Formation mechanism of $In_xGa_{1-x}As$/Ni/W contacts

Electrical properties

The currents–voltages (I–V) of the $In_xGa_{1-x}As$/Ni/W contacts were measured and the results are shown in Fig. 3. 18, where symbols ○ and × indicate Ohmic and Schottky behavior, respectively. Note that the Ohmic behavior was obtained only in Sample–A and that the electrical properties are very sensitive to the Ni layer thickness. The contact resistance (R_c) values of Sample–A4 are plotted in Fig. 3. 19 as a

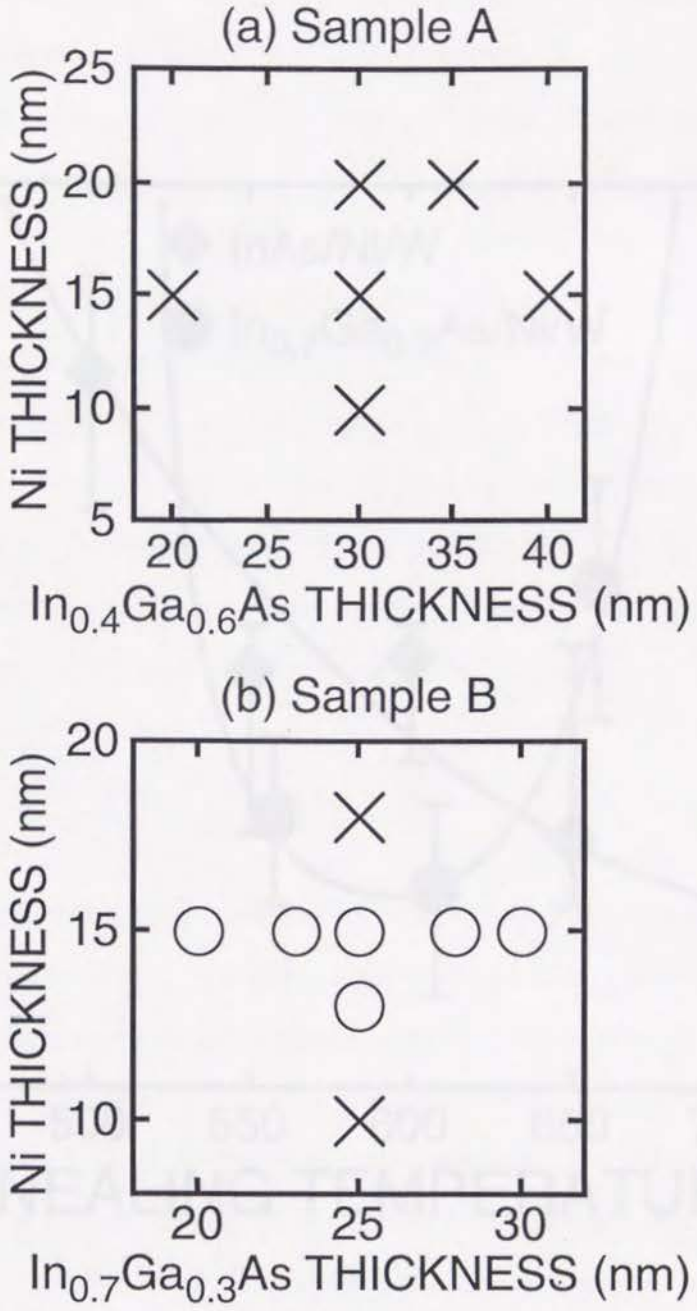


Fig. 3. 18 Current–voltages of the InGaAs/Ni/W contacts, where symbols ○ and × indicate Ohmic and non–Ohmic behavior, respectively.

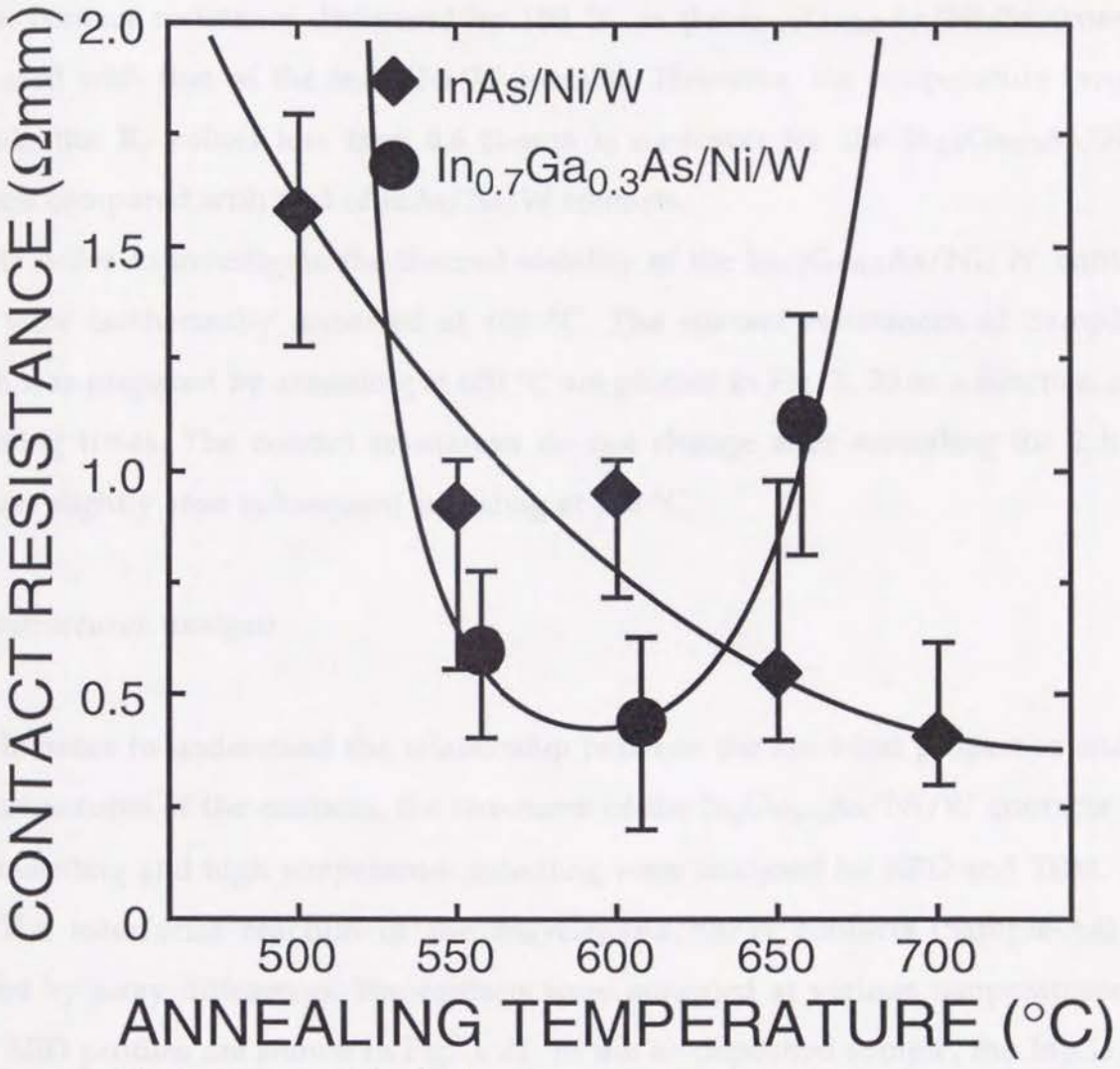


Fig. 3. 19 Contact resistances of Sample A–4 annealed at various temperatures by RTA.

function of annealing temperatures, where the contribution of the metal sheet resistance to the contact resistance was subtracted using an equation given by Marlow and Das. [13] The lowest value ~0.4 Ω–mm of the contact resistance was obtained in Sample–A4 after annealing at 600 °C. (In this figure the R_c values of the InAs/Ni/W (Sec. 3. 1) are shown for comparison.) The optimum temperature to produce the lowest contact resistance decreased by 150 °C in the $In_{0.7}Ga_{0.3}As$/Ni/W contacts compared with that of the InAs/Ni/W contacts. However, the temperature range to provide the R_c values less than 0.6 Ω–mm is narrower for the $In_{0.7}Ga_{0.3}As$/Ni/W contacts compared with that of InAs/Ni/W contacts.

In order to investigate the thermal stability of the $In_{0.7}Ga_{0.3}As$/Ni/W contacts, they were isothermally annealed at 400 °C. The contact resistances of Sample-A4 which was prepared by annealing at 600 °C are plotted in Fig. 3. 20 as a function of the annealing times. The contact resistances do not change after annealing for 2 h and increase slightly after subsequent annealing at 400 °C.

Microstructural analysis

In order to understand the relationship between the electrical properties and the microstructures of the contacts, the structures of the $In_xGa_{1-x}As$/Ni/W contacts after pre–annealing and high temperature annealing were analyzed by XRD and TEM.

The interfacial reaction of the $In_{0.7}Ga_{0.3}As$/Ni/W contacts (Sample-A4) was studied by x-ray diffraction. The contacts were annealed at various temperatures and their XRD profiles are shown in Fig. 3. 21. In the as–deposited sample, the $In_xGa_{1-x}As$ layer was observed to have an amorphous structure. After pre–annealing, Ni reacts with the $In_{0.7}Ga_{0.3}As$ layer and the peaks corresponding to $NiAs_2$ are detected. Crystallization of the $In_{0.7}Ga_{0.3}As$ layer is observed at 500 °C and this layer reacts with the GaAs at higher temperatures. The In composition (x) in the $In_xGa_{1-x}As$ phases was about 0.7 for the samples annealed at temperatures in the range of 500 to 600 °C and

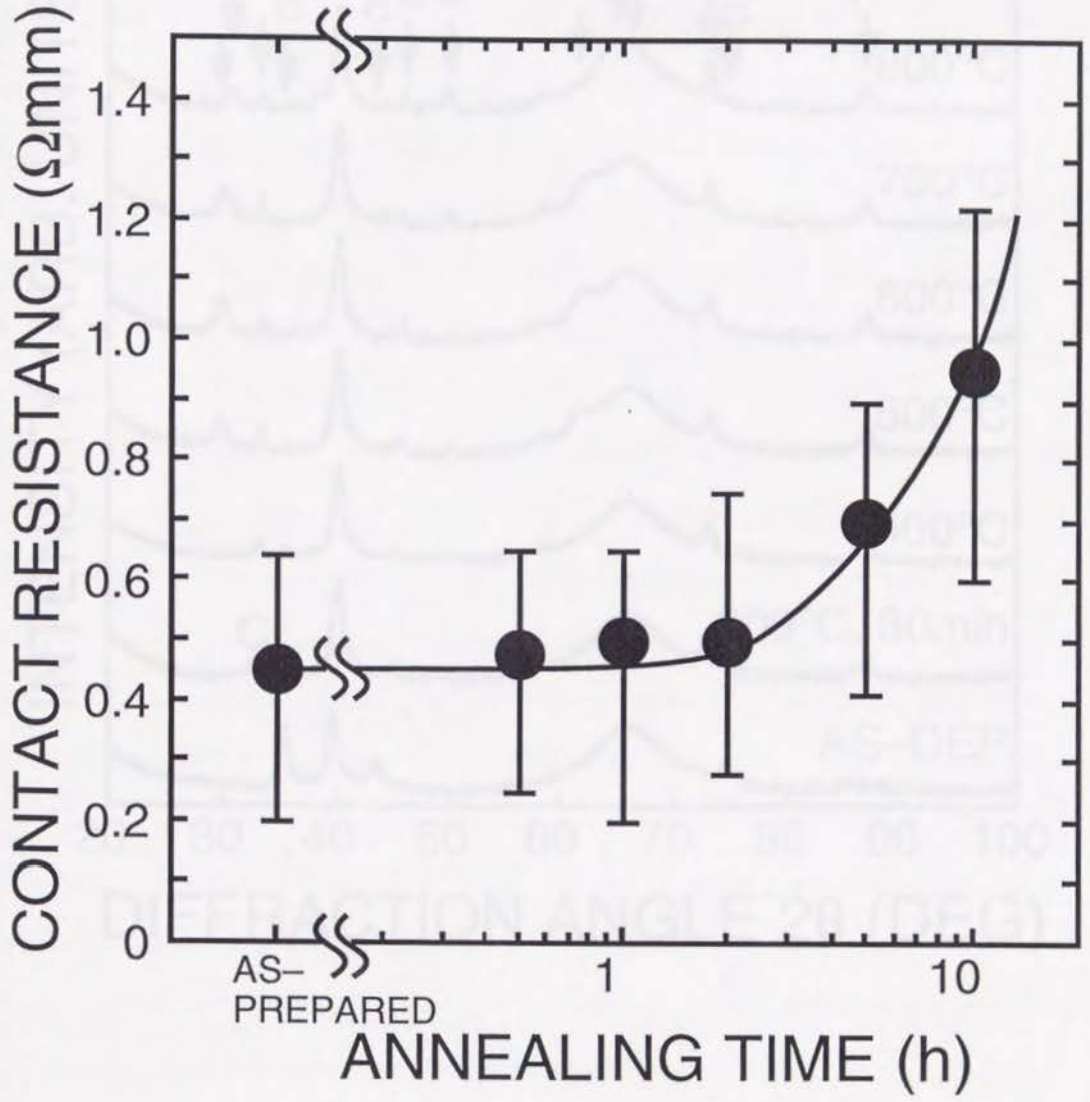


Fig. 3. 20 Contact resistances of Sample-A4 during isothermal annealing at 400 °C.

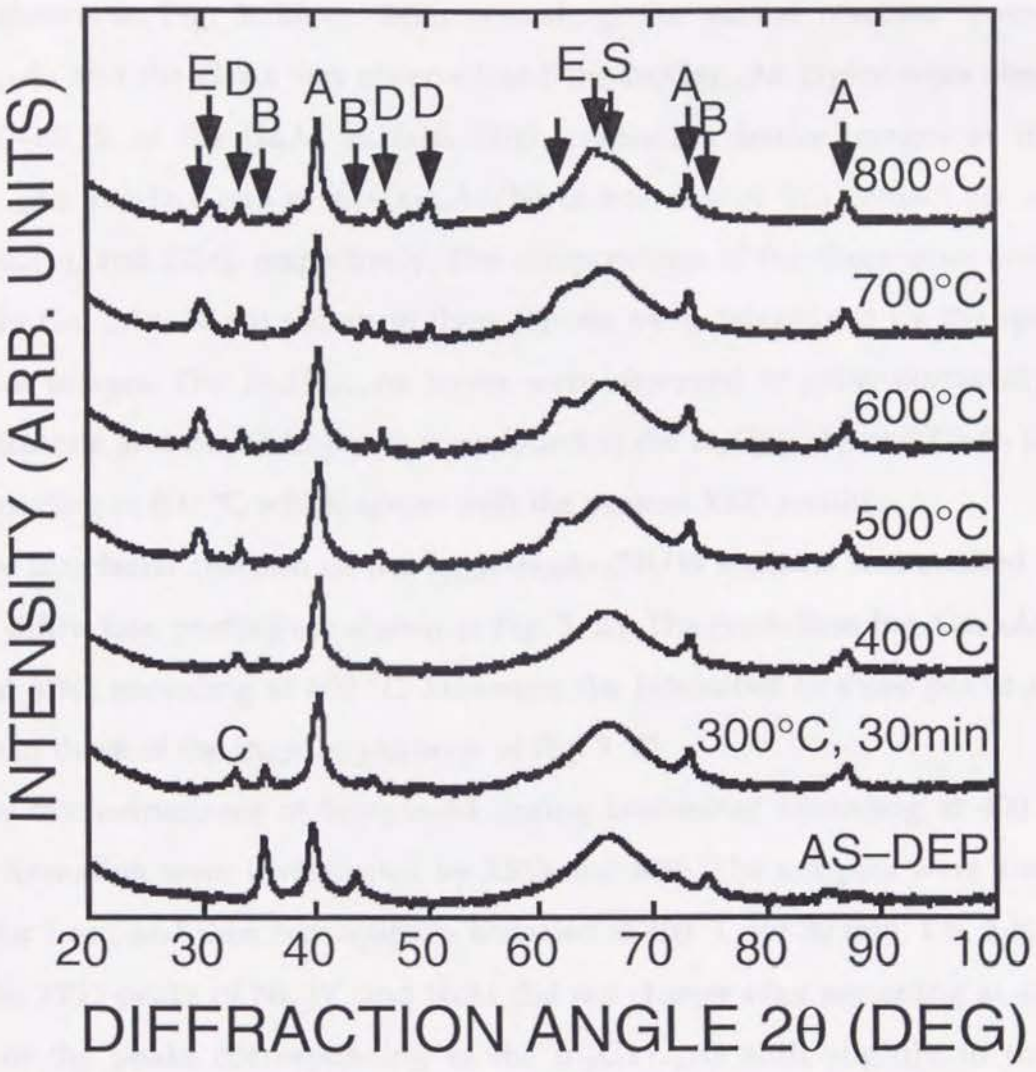


Fig. 3. 21 XRD profiles of Sample A–4 as–deposited, after annealing at 300 °C for 30 min, and after annealing at 400~800 °C for 1 s. (A: α-W; B: β-W; C:$NiAs_2$; D: NiAs; E: InGaAs; S: Substrate).

decreased to 0.5 at the temperatures above 600 °C. Note that the lowest contact resistance was obtained in the contact annealed at 600 °C.

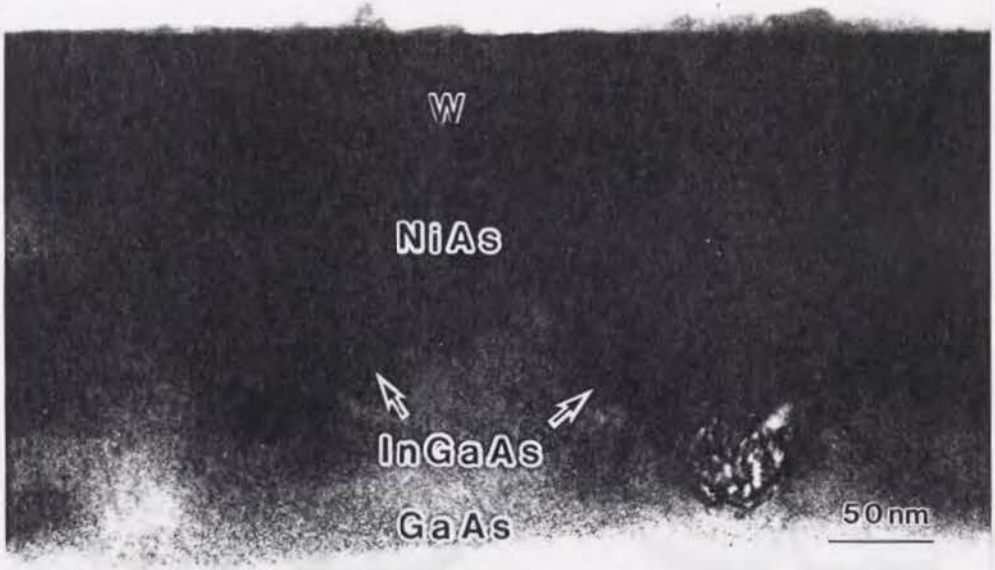
The XTEM micrographs of the $In_{0.7}Ga_{0.3}As$/Ni/W contacts after annealing at 600 °C are shown in Fig. 3. 22(a). After annealing, the partial reaction between the $In_{0.7}Ga_{0.3}As$ and the GaAs was observed and the $In_xGa_{1-x}As$ layers were observed to cover 30~60 % of the GaAs surface. High resolution lattice images at the GaAs /$In_xGa_{1-x}As$ interface and at $In_xGa_{1-x}As$/NiAs interface of this contact are shown in Figs. 3. 22(b), and 22(c), respectively. The compositions of the three compound layers (GaAs, $In_xGa_{1-x}As$, NiAs) shown in these figures were determined by the spacings of the lattice images. The $In_xGa_{1-x}As$ layers were observed to grow epitaxially on the GaAs substrate and the NiAs layers were found at the $In_xGa_{1-x}As$ and GaAs interfaces after annealing at 600 °C which agrees with the present XRD results.

The interfacial reaction of the $In_{0.4}Ga_{0.6}As$/Ni/W contacts was studied by XRD, and the diffraction profiles are shown in Fig. 3. 23. The crystalline $In_{0.4}Ga_{0.6}As$ layer is observed after annealing at 600 °C. However, the intensities of these peaks are much lower than those of the $In_{0.7}Ga_{0.3}As$ layer of Fig. 3. 21.

The microstructures of Sample-A4 during isothermal annealing at 400 °C after contact formation were investigated by XRD and RBS. The samples were annealed at 600 °C for 1 sec, and then subsequently annealed at 400 °C for 30 min, 1 h, 2 h, 4 h, and 10 h. The XRD peaks of Ni, W, and NiAs did not change after annealing at 400 °C for 10 h, but the peaks corresponding to the $In_xGa_{1-x}As$ shift slightly to the higher diffraction angle, which indicates that the In concentration (x) in the $In_xGa_{1-x}As$ phases decreases with increasing the annealing time.

The RBS spectra of Sample-A4 which was annealed at 600 °C for 1 s and then annealed at 400 °C for 10 h are shown in Fig. 3. 24. The spectra changed after annealing at 400 °C, indicating that the In in the $In_xGa_{1-x}As$ layer diffuses to the GaAs substrate during annealing at 400 °C, which could lead to the increase of the R_c value.

The surface morphology of the $In_{0.7}Ga_{0.3}As$/Ni/W contacts was observed by



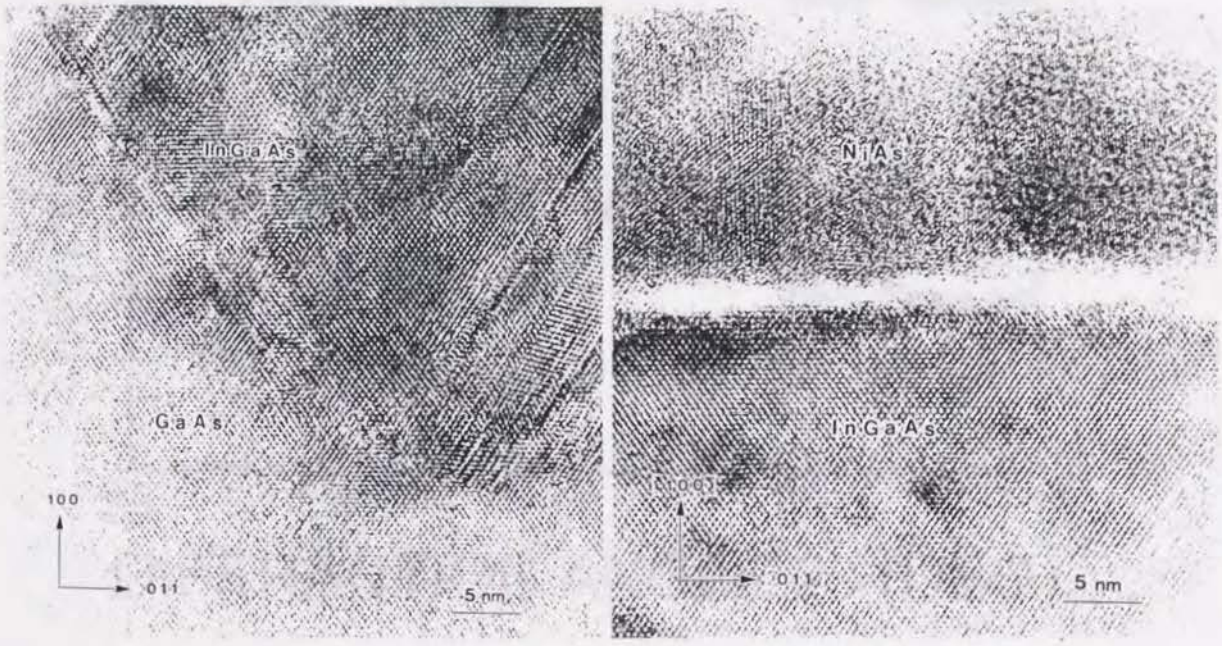


Fig. 3. 22 (a)The XTEM micrographs of Sample-A4 after annealing at 600 °C for 1 s, (b) high resolution lattice image at GaAs/InGaAs interface of Sample-A4 after annealing at 600 °C for 1 sec, and (c) high resolution lattice image at InGaAs/GaAs interface of Sample-A4 after annealing at 600 °C for 1 s.

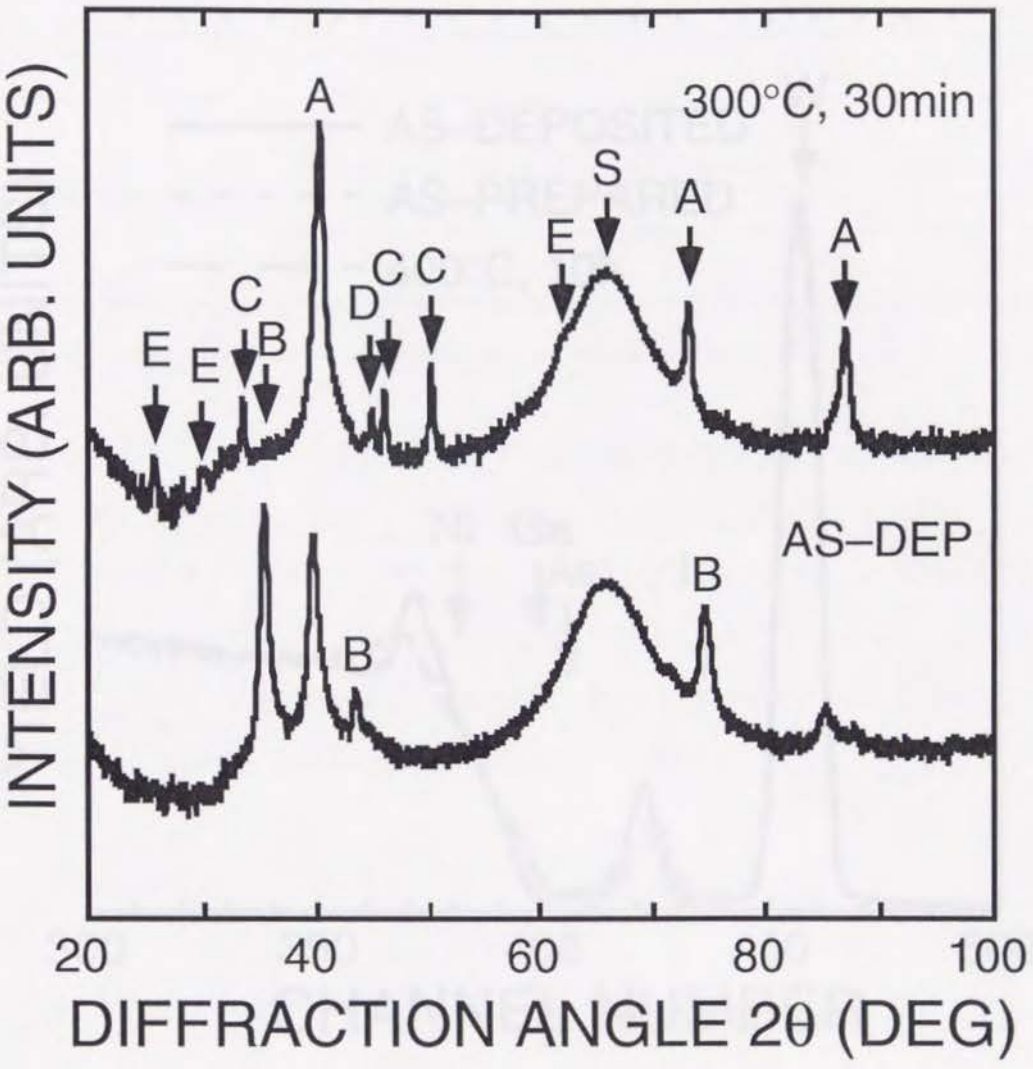


Fig. 3. 23 XRD profiles of the $In_{0.4}Ga_{0.6}As$ contacts as–deposited and after annealing at 300 °C for 30 min. (A: α-W; B: β-W; C:NiAs; D: Ni; E: InGaAs; S: Substrate).

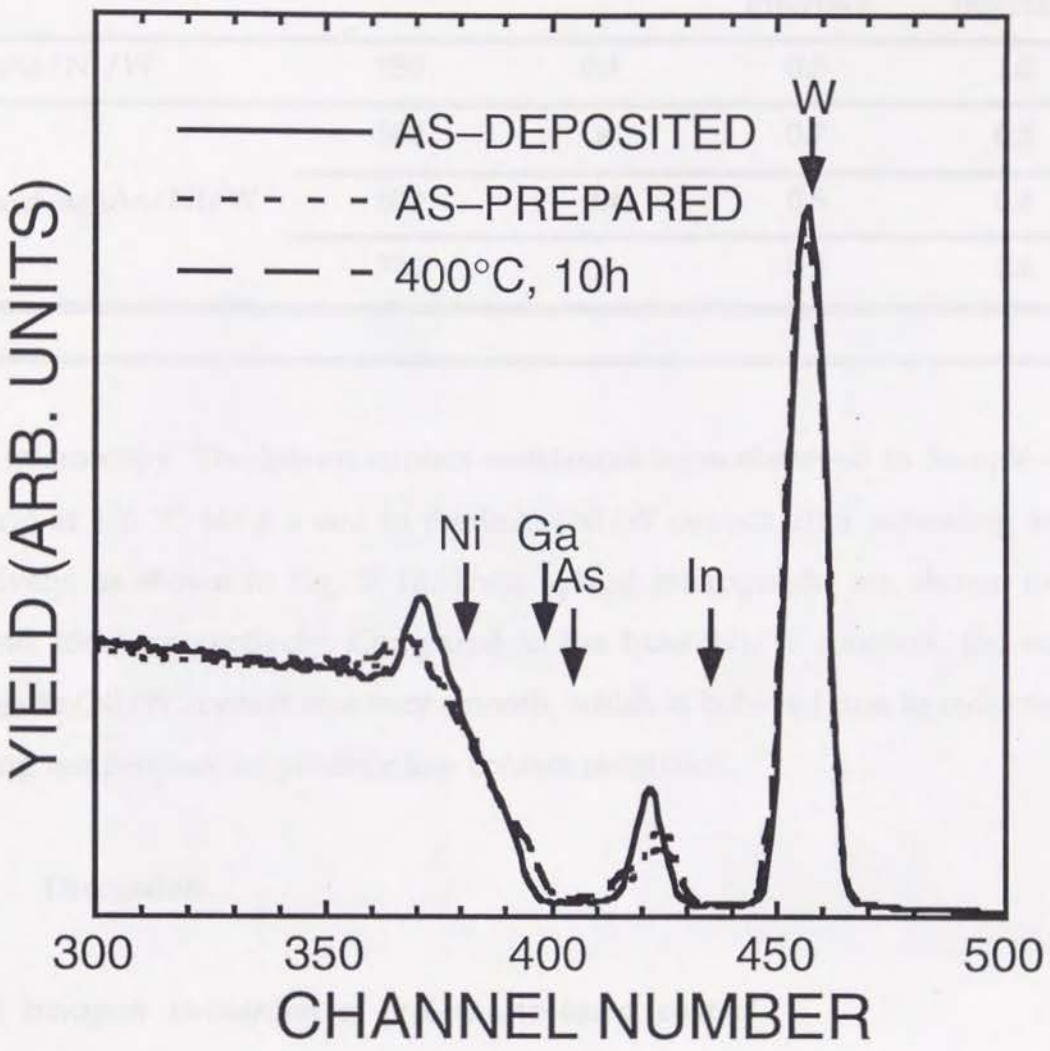


Fig. 3. 24 Rutherford backscattering spectra of Sample-A4 as–deposited, as–prepared, and after annealing at 400 °C for 10 h.

Table IV. Correlation between In concentrations (x) in the $In_xGa_{1-x}As$ layers and R_c values.

Sample	Annealing Temp. (°C)	R_c(Ωmm)	x($In_xGa_{1-x}As$) GaAs interface	x($In_xGa_{1-x}As$) Metal interface
InAs/Ni/W	750	0.4	0.5	1.0
$In_{0.7}Ga_{0.3}As$/Ni/W	500	×	0.7	0.8
	600	0.4	0.5	0.8
	700	×	0.5	0.6

optical microscopy. The lowest contact resistances were observed in Sample–A4 after annealing at 600 °C for 1 s and in the InAs/Ni/W contact after annealing at 750 °C, respectively, as shown in Fig. 3. 19. Their optical micrographs are shown in Figs. 3. 25(a) and 25(b), respectively. Compared to the InAs/Ni/W contacts, the surface of $In_{0.7}Ga_{0.3}As$/Ni/W contact was very smooth, which is believed due to reduction of the annealing temperature to produce low contact resistance.

3. 2. 4 Discussion

Current transport mechanism of $In_xGa_{1-x}As$–based contact

The epitaxial growth of the $In_xGa_{1-x}As$ layer on the GaAs substrate was found to be essential to convert the I–V characteristics of the metal/n–GaAs contacts from Schottky behavior to Ohmic behavior by previous studies. [4, 20] In such the contacts two barriers exist at the metal/$In_xGa_{1-x}As$ interface and at the $In_xGa_{1-x}As$/GaAs interface, and the R_c values are determined by the higher barrier between the two. Their barrier

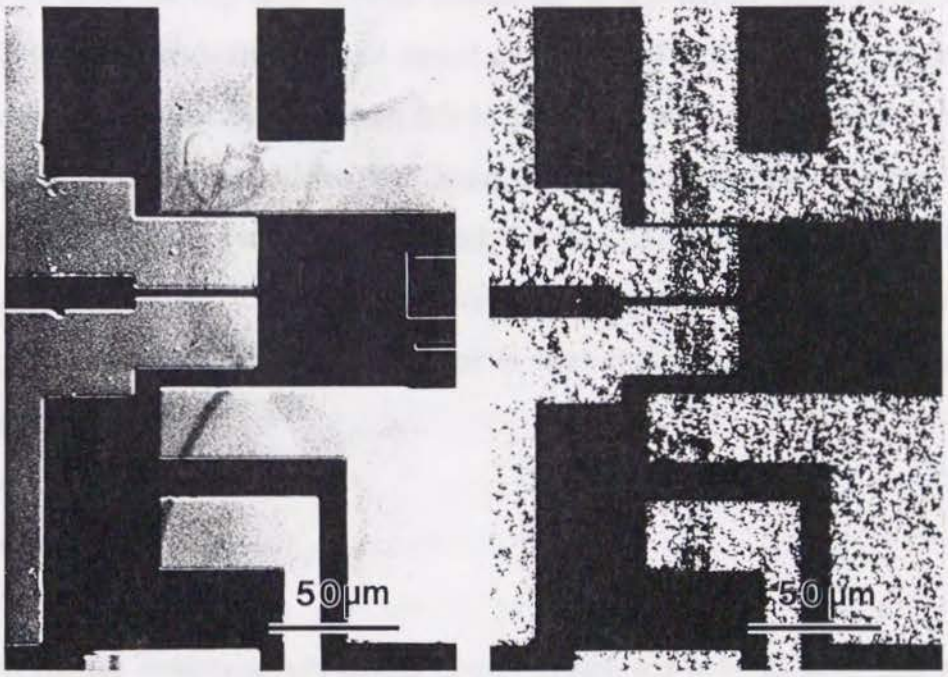


Fig. 3. 25 (a) Optical micrograph of the $In_{0.7}Ga_{0.3}As$/Ni/W contact after annealing at 300 °C for 30 min and 600 °C for 1 s and (b) optical micrograph of the InAs/Ni/W contact after annealing at 300 °C for 30 min and 750 °C for 1 s.

heights are determined by the In concentration (x) in the $In_xGa_{1-x}As$ layers and the percentage of the GaAs interface covered by the $In_xGa_{1-x}As$ layers. The correlation between the R_c values and the percentage of the GaAs interface covered by the $In_xGa_{1-x}As$ layers was extensively studied and it was found that the R_c values are almost constant when more than 50 % of the GaAs interface is covered by the $In_xGa_{1-x}As$ layers. [14]

In the present study, the distribution (normal to the contact surface) of the In concentrations (x) in the $In_xGa_{1-x}As$ layers was measured by TEM [Figs. 3. 22(b), 22(c)] and correlated with the R_c values in Table 3. IV. This table suggests us that the In concentrations at both the top and bottom interfaces of the $In_xGa_{1-x}As$ layer influence strongly the R_c values. From the present result of Table 3. IV, the x value at the $In_xGa_{1-x}As$/GaAs interface should be less than 0.5 to prepare low R_c. Therefore, the lattice mismatch at the interface should be less than 4% to prepare low R_c. On the other hand, it is concluded that x value at the metal/$In_xGa_{1-x}As$ interface should be larger than 0.7 to obtain low R_c values. A reason why the contacts prepared by the $In_{0.4}Ga_{0.6}As$ target showed Schottky behavior is that this contacts do not satisfy the above requirements.

3. 2. 5 Conclusion

Reduction of the optimum annealing temperature for low R_c and improvement of surface morphology of the previously developed InAs/Ni/W contacts were successfully achieved by using $In_{0.7}Ga_{0.3}As$ targets instead of InAs targets. However, the lowest R_c values of these contacts were almost same. It was found that there exists wide distribution of the In concentrations (x) inside the $In_xGa_{1-x}As$ layers along the direction normal to the contact surface. The R_c values were strongly influenced by the In concentrations (x) both at the metal/$In_xGa_{1-x}As$ interface and at the $In_xGa_{1-x}As$ /GaAs interface. The In concentrations (x) at the $In_xGa_{1-x}As$/GaAs interface of both the

InAs/Ni/W and $In_{0.7}Ga_{0.3}As$/Ni/W contacts were almost same which determine the R_c when the In concentration at the metal/$In_xGa_{1-x}As$ is higher than 0.7. This non-uniform In distribution also explained a reason why the Ohmic behavior were not obtained in the $In_{0.4}Ga_{0.6}As$/Ni/W contacts.

3.3 Development of $In_{0.7}Ga_{0.3}As$/Ni/W_2N/W contact

3.3.1 Introduction

In Section 3. 1, the InAs/Ni/W contact was prepared by the radio frequency (rf) sputtering technique and the best contact resistance (R_c) was about 0.3 Ω–mm. This contact provided low R_c values and excellent thermal stability at 400 °C for 10 h. However, reproducibility of the R_c values was poor, and the surface morphology was rough. These poor properties were found to be due to In out–diffusion through the W layer.

In Section 3. 2, in order to prevent the In out–diffusion, the contact formation temperature was reduced by using a $In_{0.7}Ga_{0.3}As$ target instead of the InAs target. The optimum formation temperature of $In_{0.7}Ga_{0.3}As$/Ni/W contact was reduced from 750 °C to 600 °C. The R_c value of this contact was 0.4 Ω–mm, and the contact surface was smooth. However, reproducibility of the R_c values was still poor because a small amount of the In diffused to the W layer. The best method to prevent the In out-diffusion is to deposit the barrier layer for the In diffusion. In addition, suppression of the In out–diffusion is expected to increase the contact area of the $In_xGa_{1-x}As$/GaAs interface, resulting the reduction of the R_c values. Various barrier layers have been investigated for electrode materials by depositing refractory metals, nitride, or silicide. However, the barrier layer for the In diffusion has not been reported.

The purposes of this section are twofold. The first is to study the effectiveness of W_2N layers as the In diffusion barrier for the $In_xGa_{1-x}As$–based Ohmic contacts by

preparing the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contacts using the rf sputtering technique. The second purpose is to understand the contact formation mechanism by analyzing the interfacial structure using x–ray diffraction (XRD) and cross sectional high-resolution electron microscopy (HREM).

3.3.2 Experimental Procedure

$In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ samples were sequentially deposited by the rf sputtering technique. Thicknesses of the W_2N and the W layer were 25nm, respectively. W_2N was sputter deposited from W target in a mixed gas of argon (Ar) and nitrogen (N_2). The composition of the W_2N was measured by Rutherford backscattering spectroscopy (RBS). The substrate temperature was kept at 100 °C during the W_2N deposition. The $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ samples were annealed at the temperatures in the range of 450 to 700 °C for 10 s by rapid thermal annealer (RTA) in a 5 % H_2/N_2 atmosphere. Isothermal annealing at 400 °C after contact formation was carried out in 5 % H_2/N_2 atmosphere to investigate the thermal stability.

The R_c values were measured by the transmission line method (TLM). [12] Microstructural analysis were carried out by XRD and HREM. The surface morphology of the contacts was observed by an optical microscope.

3.3.3 Experimental Results

Electrical properties

The current–voltages (I–V) of the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contacts were measured and the results are shown in Fig. 3. 28, where symbols ○ and × indicate Ohmic and non–ohmic behavior, respectively. The lowest R_c value was obtained by

depositing 14 nm thick $In_{0.7}Ga_{0.3}As$ and 10 nm thick Ni.

The R_c values of this sample are plotted in Fig. 3. 29 as a function of annealing temperatures, where the annealing time was ~10 sec. The error bars indicate the highest and the lowest R_c values among 20 TLM measurements. The metal sheet resistance (R_s) of this sample was 6 Ω/□. The contribution of the R_s value to the R_c value was subtracted using an equation given by Marlow and Das. [13] The R_c value of 0.1 Ω–mm was obtained after annealing at 550 °C.

The thermal stability during isothermal annealing at 400 °C was investigated after contact formation. The R_c values are plotted in Fig. 3. 30 as a function of the annealing times. The R_c value lower than 0.2 Ω–mm was obtained after annealing at 400 °C for 5 h and increased slightly to 0.3 Ω–mm after 10 h annealing.

Microstructural analysis

The interfacial reaction of the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contact after annealing at 550 °C for 10 s was investigated by XRD, and its profile is shown in Fig. 3. 29. In this sample, diffraction peaks corresponding to α–W, W_2N, NiAs and $In_xGa_{1-x}As$ are observed. The In composition (x) in the $In_xGa_{1-x}As$ was measured to be about 0.5 from the $In_xGa_{1-x}As$ (400) peak. Note that this x value is the same value of the $In_{0.7}Ga_{0.3}As/Ni/W$ contacts prepared previous by annealing at 300 °C for 30 min and 600 °C for 1 s, where the R_c value was 0.4 Ω–mm. [24]

Figure 3. 30 is a high–resolution image of the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contact. Epitaxialy grown $In_xGa_{1-x}As$ layers are observed between the W_2N and the GaAs substrate, and about 90 % of the GaAs surface is covered by the $In_xGa_{1-x}As$ layers. Also, NiAs phases are observed at the $In_xGa_{1-x}As/GaAs$ interface and in the $In_xGa_{1-x}As$ layers as indicated by arrows. The $In_xGa_{1-x}As$ phase and the NiAs phase were determined by the lattice spacings, and the results agree very well with the XRD observation.

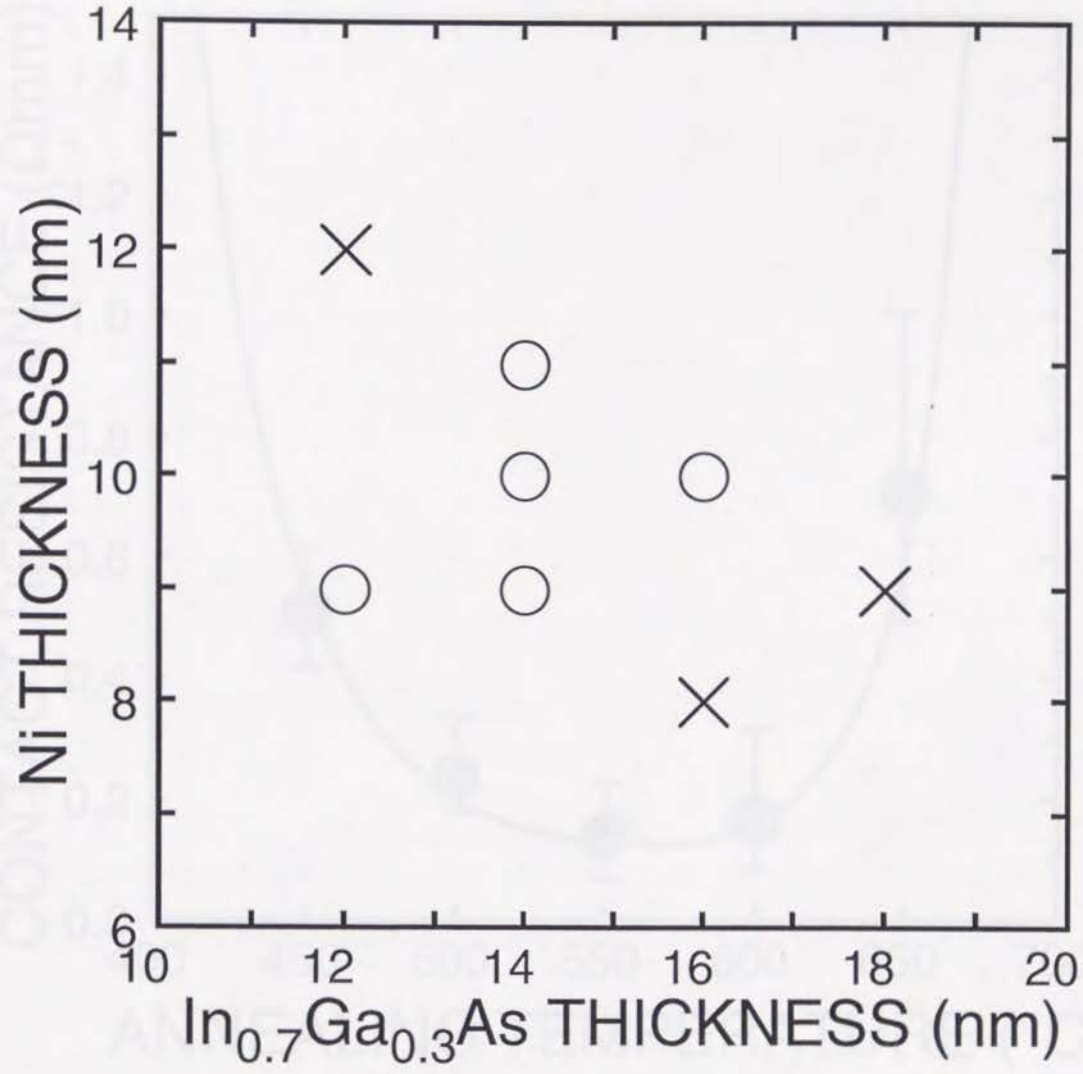


Fig. 3. 26 Current–voltages of the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contacts, where symbols ○ and × indicate Ohmic and non–Ohmic behavior, respectively.

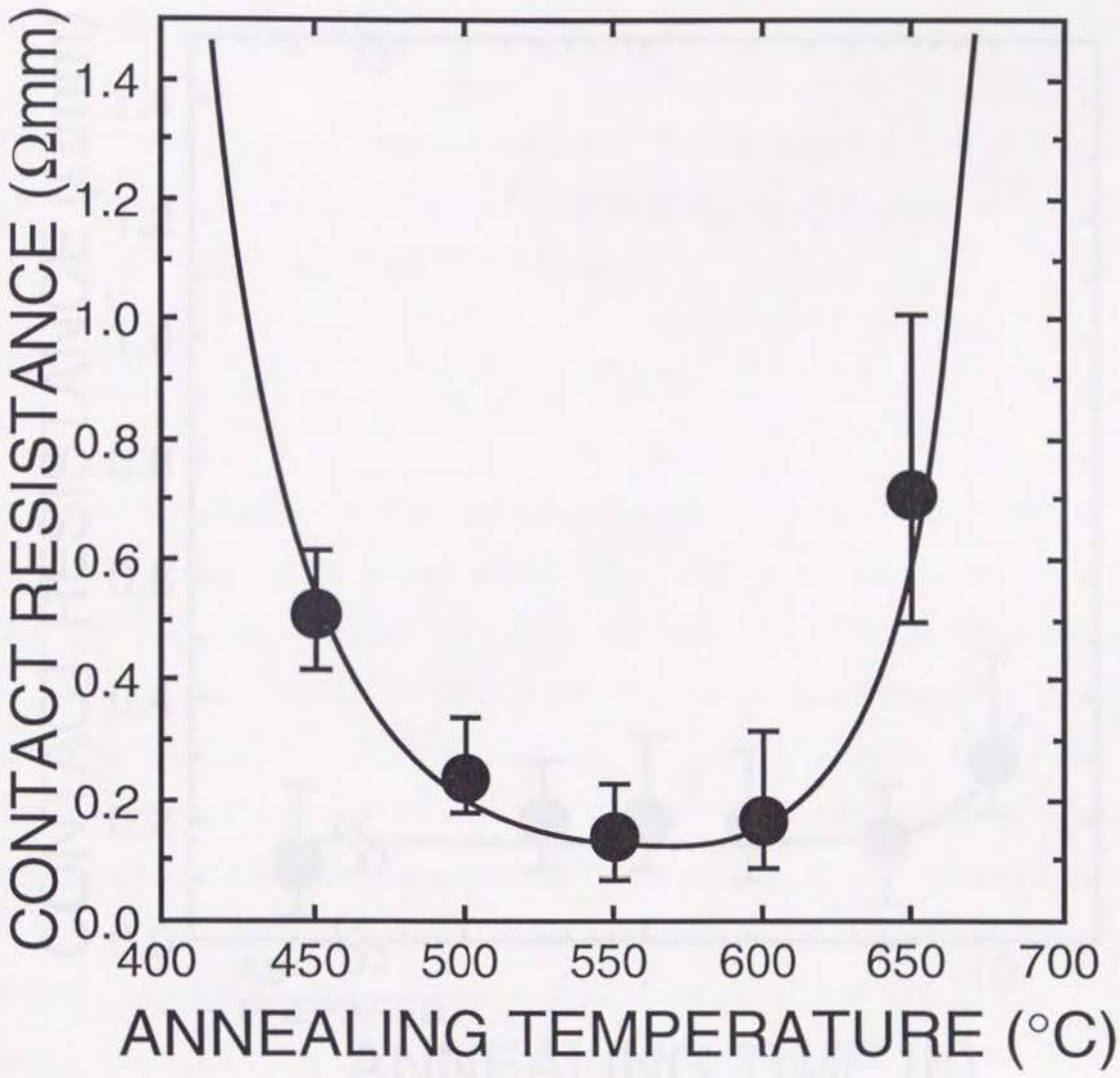


Fig. 3. 27 Contact resistances of $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contact annealed at various temperatures for 10 s.

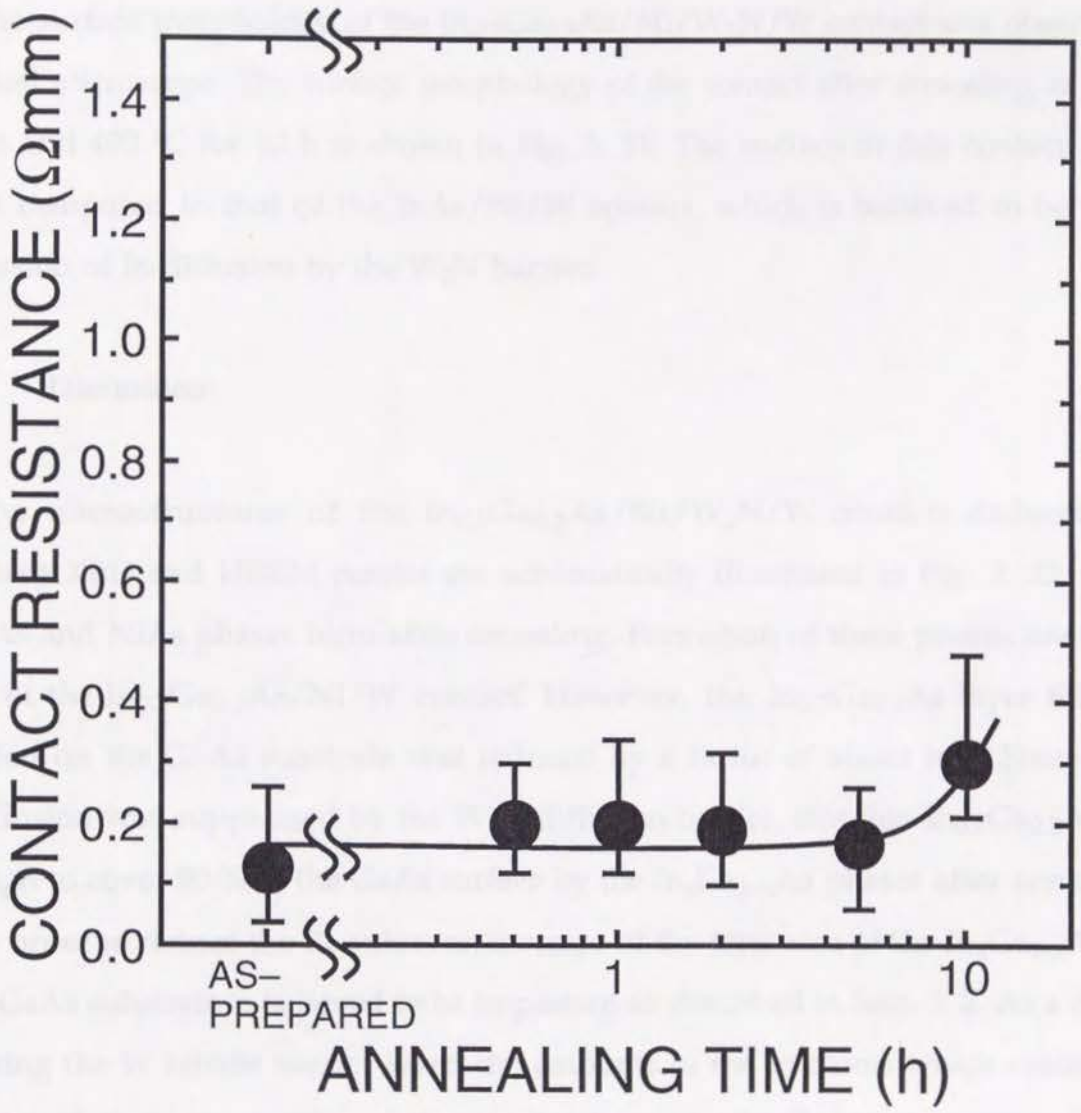


Fig. 3. 28 Contact resistances of $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contact during isothermal annealing at 400 °C.

The In concentrations x in the $In_xGa_{1-x}As$ layers were measured by the lattice spacings of the $In_xGa_{1-x}As$ layers. The In concentrations in the $In_xGa_{1-x}As$ phases at the $W_2N/In_xGa_{1-x}As$ interface was larger than 0.7 and was 0.5 at the $In_xGa_{1-x}As/GaAs$ interface. The In concentrations at these interfaces satisfy the condition to form Ohmic contact as discussed in Sec. 3. 2.

The surface morphology of the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contact was observed by an optical microscope. The surface morphology of the contact after annealing at 550 °C for 10 s and 400 °C for 10 h is shown in Fig. 3. 31. The surface of this contact is very smooth compared to that of the InAs/Ni/W contact, which is believed to be due to suppression of In diffusion by the W_2N barrier.

3. 3. 4 Discussion

The microstructures of the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contacts deduced from thepresent XRD and HREM results are schematically illustrated in Fig. 3. 32. The $In_xGa_{1-x}As$ and NiAs phases form after annealing. Formation of these phases are similar to that of the $In_{0.7}Ga_{0.3}As/Ni/W$ contact. However, the $In_{0.7}Ga_{0.3}As$ layer thickness deposited on the GaAs substrate was reduced by a factor of about two. Since the In out–diffusion was suppressed by the W_2N diffusion barrier, this thin $In_{0.7}Ga_{0.3}As$ layer is enough to cover 90 % of the GaAs surface by the $In_xGa_{1-x}As$ phases after annealing.

In order to reduce the R_c value, an increase of the total area of the $In_xGa_{1-x}As$ layer on the GaAs substrate is believed to be important as described in Sect. 3. 2. As a result of depositing the W nitride barrier layer, the amounts of the In atoms which reacted with the GaAs substrate increased, and thus the total area on the GaAs was increased. In this study, more than 90 % of the GaAs surface was covered by the $In_xGa_{1-x}As$ phases, and the R_c value of 0.1 Ω–mm was achieved. In addition, since the $In_xGa_{1-x}As$ layer was uniformly grown on the GaAs surface, the reproducibility of the R_c values was excellent. The relationship between the R_c values and the total areal

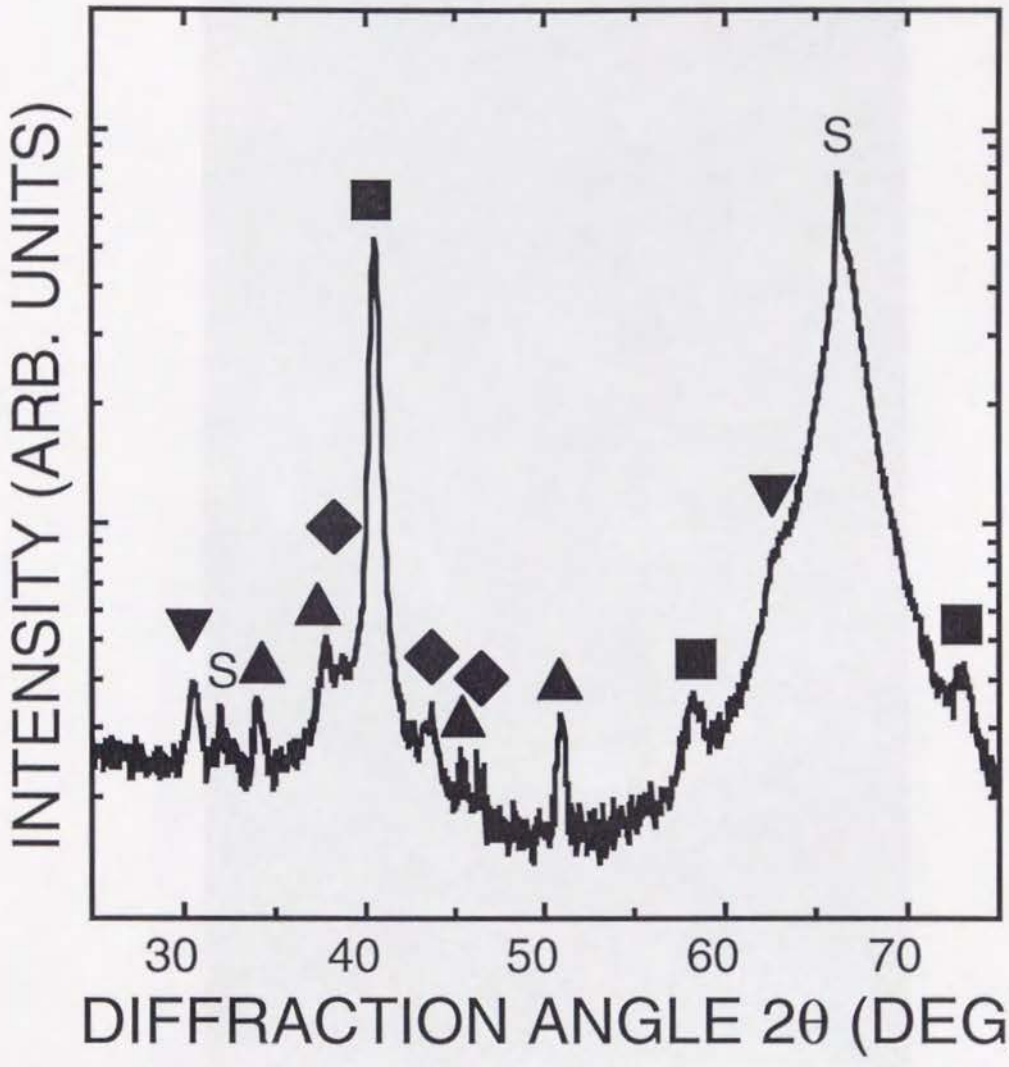


Fig. 3. 29 XRD profiles of $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contact after annealing at 550 °C for 10 s. (■: α–W; ▼: $In_xGa_{1-x}As$; ▲: NiAs; ◆: W_2N; S: GaAs substrate).

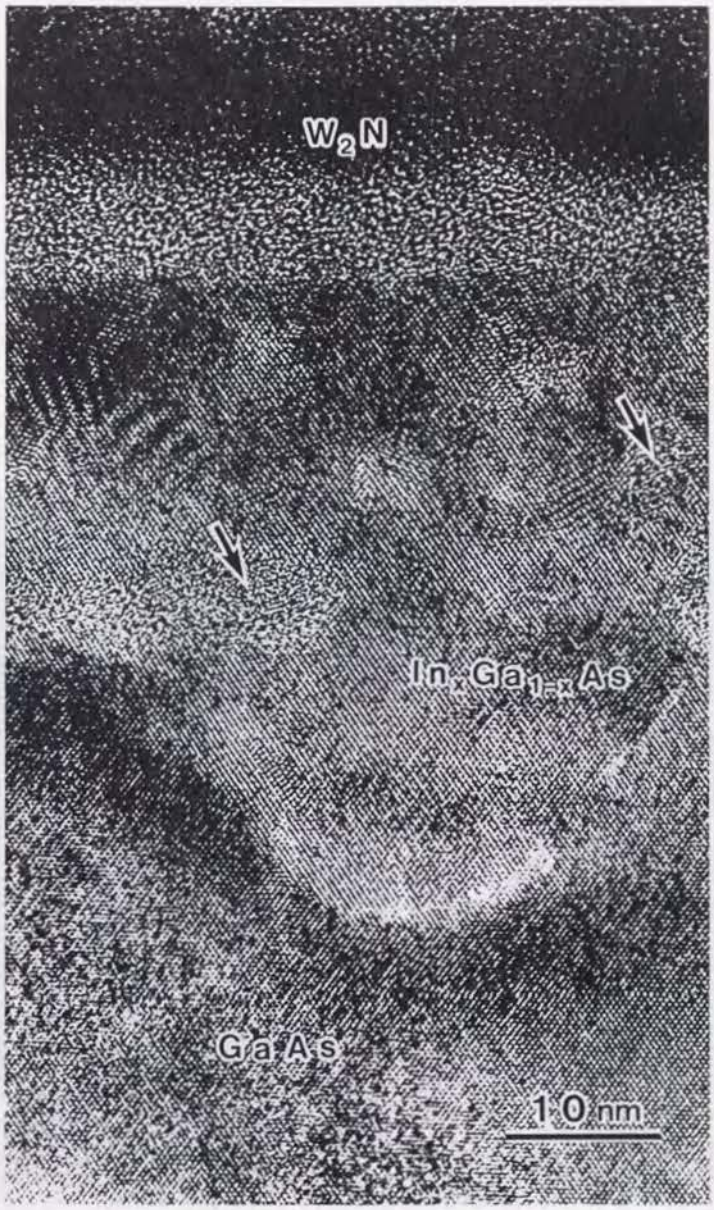


Fig. 3. 30 High resolution XTEM micrograph of $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contact after annealing at 550 °C for 10 s.

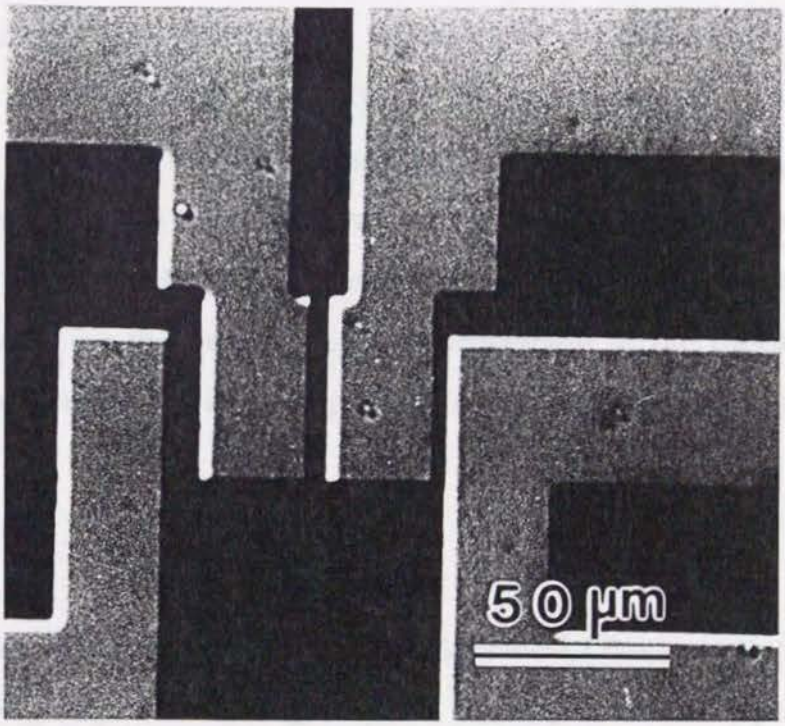


Fig. 3. 31 Optical micrograph of $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contact after annealing at 550 °C for 10 s and 400 °C for 10 h. of the $In_xGa_{1-x}As$

coverage of the $In_xGa_{1-x}As$ on the GaAs surface agree very well with that established previously by Murakami *et al.* [4]

In addition, the reduction of the $In_{0.7}Ga_{0.3}As$ layer thickness was found to simplify the thermal treatment process. In Sec. 3. 1, it was concluded that "pre–annealing" at 300 °C for 30 min prior to the high temperature annealing was necessary to prepare the low resistance contacts. During pre–annealing, Ni atoms were found to diffuse through the $In_{0.7}Ga_{0.3}As$ layer and remove the native oxide layer on the GaAs substrate by forming Ni_xGaAs. In this experiment, since the thickness of the $In_{0.7}Ga_{0.3}As$ was reduced, the Ni atoms diffuse to the GaAs substrate during heating to the elevated temperature.

The properties of the InAs/Ni/W (Sec. 3. 1), $In_{0.7}Ga_{0.3}As$/Ni/W (Sec. 3. 2) and $In_{0.7}Ga_{0.3}As/Ni/W/W_2N$ contacts are summarized in Table 3. V. The R_c values increased slightly after annealing at 400 °C for 10 h in the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contacts. The deterioration mechanism of the R_c value at 400 °C is not clear at the moment. However, since the annealing was carried out in H_2/N_2 atmosphere without cap layers such as Si_3N_4, contamination and decomposition of the contact edges would be the primary cause for the deterioration. Improvement of the thermal stabilities of this contacts are expected if the annealing is carried out with the cap layers.

3. 3. 5 Conclusion

Low resistance, thermally stable $In_xGa_{1-x}As$–based Ohmic contacts were developed by depositing sequentially $In_{0.7}Ga_{0.3}As$, Ni, W_2N, and W layer on the GaAs using rf sputtering. These contacts provided the excellent reproducibility and the smooth surface. The low R_c values were found to be due to the large total area of the $In_xGa_{1-x}As$ layer covering the GaAs substrate. These improvements of the Ohmic contact properties were found to be due to deposition of the W nitride

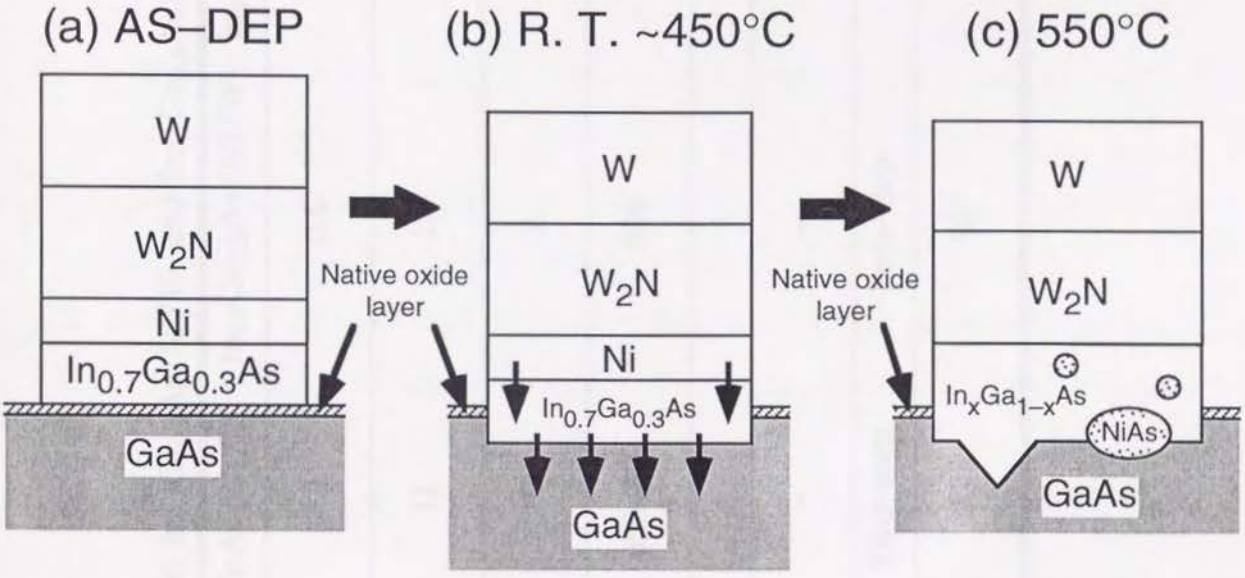


Fig. 3. 32 Schematic illustrations of $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contact (a) before annealing, (b) during annealing, and (c) after annealing.

Table 3. V.The properties of InAs/Ni/W, $In_{0.7}Ga_{0.3}As$/Ni/W, and $In_{0.7}Ga_{0.3}As$/Ni/W_2N/W contacts.

	Ideal contact	InAs/Ni/W	$In_{0.7}Ga_{0.3}As$/Ni/W	$In_{0.7}Ga_{0.3}As$/Ni/W_2N/W
Contact resistances (Ω–mm)	Low (<0.2 Ω–mm)	0.3	0.4	0.1
Sheet resistances (Ω/□)	Low (<2 Ω/□)	11	11	6
Thermal stability at 400°C (hr)	Stable (>10 hr)	10	2	5
Annealing temperature (°C)	Low (<550 °C)	650–800	600	550
Reproduciblity	Excellent	–	–	+
Surface morphology	Smooth	–	–	+
Annealing process	Simple	Two–step	Two–step	One–step
Total area of $In_xGa_{1-x}As$ (%)	100	50	50	90

barrier for the In diffusion. This low resistance, thermally stable Ohmic contacts prepared by only rf sputtering are desirable for the manufacturing GaAs devices.

3.4 References

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4. $In_xGa_{1-x}As$–based contacts with wiring metals

4.1 Introduction

As described in the previous section, development of the low resistance, thermally stable Ohmic contacts is necessary for improvement of the GaAs VLSI devices. In the actual integrated circuits, these contacts are connected by the wiring metals.

In the Si device technology, Al metallizations are extensively used, because Al has low resistivity (ρ=2.7 $\mu\Omega$cm at 20 °C) and adheres well to various materials. However, with increasing the integration level, the reliability of the Al wirings become in concern. Since the resistivity of Cu is lower (ρ=1.7 $\mu\Omega$cm at 20 °C) than that of Al and the reliability of the Cu–based metallization is expected to be higher than that of the Al–based metallization, Cu is a promising material for the wiring metal for the future Si device technology.

In the GaAs device technology, Au is extensively used. Therefore, in order to apply the current Si packaging process to the GaAs devices, the Ohmic contacts are desirable to be compatible with Al or Cu wirings instead of Au. However, Al interacts with Au and forms intermetallic compounds. Note that Au is one of the key elements in the AuGeNi Ohmic contacts, which is extensively used in the present GaAs device technology. Therefore, the Al wiring deteriorates the electrical properties of the AuGeNi contacts when it is used in the GaAs technology.

In Section 3. 3, low resistance Ohmic contacts which provide excellent reproducibility, smooth surface and excellent thermal stability have been developed by depositing $In_{0.7}Ga_{0.3}As$, Ni, W_2N, and W by rf sputtering. However, the compatibility of the Al wirings or the Cu wirings for the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contacts has not been studied.

The purpose of a present experiment is to study the compatibility of the Al or the Cu wirings for the InGaAs–based Ohmic contacts. The effect of the annealing temperatures on the R_c values of the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contacts with an Al or a Cu layer was investigated by using a transmission line method (TLM). The distributions of the In atoms before and after annealing were studied by Rutherford backscattering spectrometry (RBS).

4. 2. Experimental

The details of the experimental procedures to prepare the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contacts and to measure the contact resistance (R_c) by the transmission line method (TLM) [1] were described in Section 3. 3. The TLM channels were prepared by doping the selected areas of the semi–insulating (100)–oriented GaAs substrate with $^{29}Si^+$ ions at an energy of 38.5 keV with a dose level of 1.3×10^{14} cm^{-2} and by activating them at 850 °C for 20 min. The sheet resistance of the channels was measured to be about 200 Ω/□.

Prior to metal deposition, the substrates were chemically cleaned by rinsing in HCl for 3 min and then deionized water for 1 min. The vacuum chamber was evacuated to 3×10^{-5} Pa. $In_{0.7}Ga_{0.3}As$ (14 nm), Ni (10 nm), W_2N (25 nm), and W (25 nm) were sequentially deposited by the radio frequency (rf) sputtering technique, where W_2N was sputter–deposited from a W target in a mixed gas of argon and nitrogen. After contact metal deposition, the samples were re-loaded into the vacuum chamber. Before deposition, the vacuum chamber was evacuated to 3×10^{-5} Pa, and 200 nm thick Al or Cu were deposited by a resistance heater and an electron–beam, respectively. In order to improve the adhesion between the Cu layer and the contact metal, 10 nm thick Cr was deposited before the Cu deposition. After the metal deposition, the photo –resists were lifted–off. The samples were annealed at temperatures in the range of 450

to 650 °C for 10 s by a rapid thermal annealer (RTA) in a H_2/N_2 (5%) forming gas.

The thermal stability of the contact was evaluated by annealing the samples at 400 °C for 10 h in a H_2/N_2 (5%) gas atmosphere. The microstructures of the contacts were analyzed by Rutherford backscattering spectrometry (RBS) with 2 MeV $^4He^{2+}$ ions at an observed scattering angle of 170°. Surface morphology was observed by the optical microscope.

4. 3. Results and Discussion

The R_c values of the contacts (with the Al overlayer) are plotted in Fig. 4. 1 as a function of annealing temperatures. The R_c values lower than 0.2 Ωmm were obtained after annealing at 550 °C for 10 s. This dependence of the R_c values on the temperatures is similar to that of the contact without the Al overlayer. [2] This result indicates that the Al overlayer did not affect the formation mechanism of the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contacts. However, the temperatures range to provide the Ohmic behavior is narrower than that of the contact without the Al overlayer. The reason is not clear at the moment. The metal sheet resistance (R_s) of this contact was 0.28 Ω/□ and the contribution of the R_s value to the R_c values is negligibly small according to the theory developed by Marlow and Das. [3]

The optical micrograph of the contact after annealing at 550 °C is shown in Fig. 4. 2. The surface of this contact is rough, because the annealing temperature is close to the melting point of Al (T_m~660 °C). This poor surface morphology will be improved by depositing a refractory cap layer before annealing.

The thermal stability during isothermal annealing at 400 °C after contact formation was investigated for the contacts with the Al overlayer. The R_c values are plotted in Fig. 4. 3 as a function of the annealing times. The R_c values of 0.2 Ωmm did not change after annealing at 400 °C for 5 h and increased slightly to 0.3 Ωmm after 10 h annealing. The deterioration of the R_c values after annealing at 400 °C for 10 h was

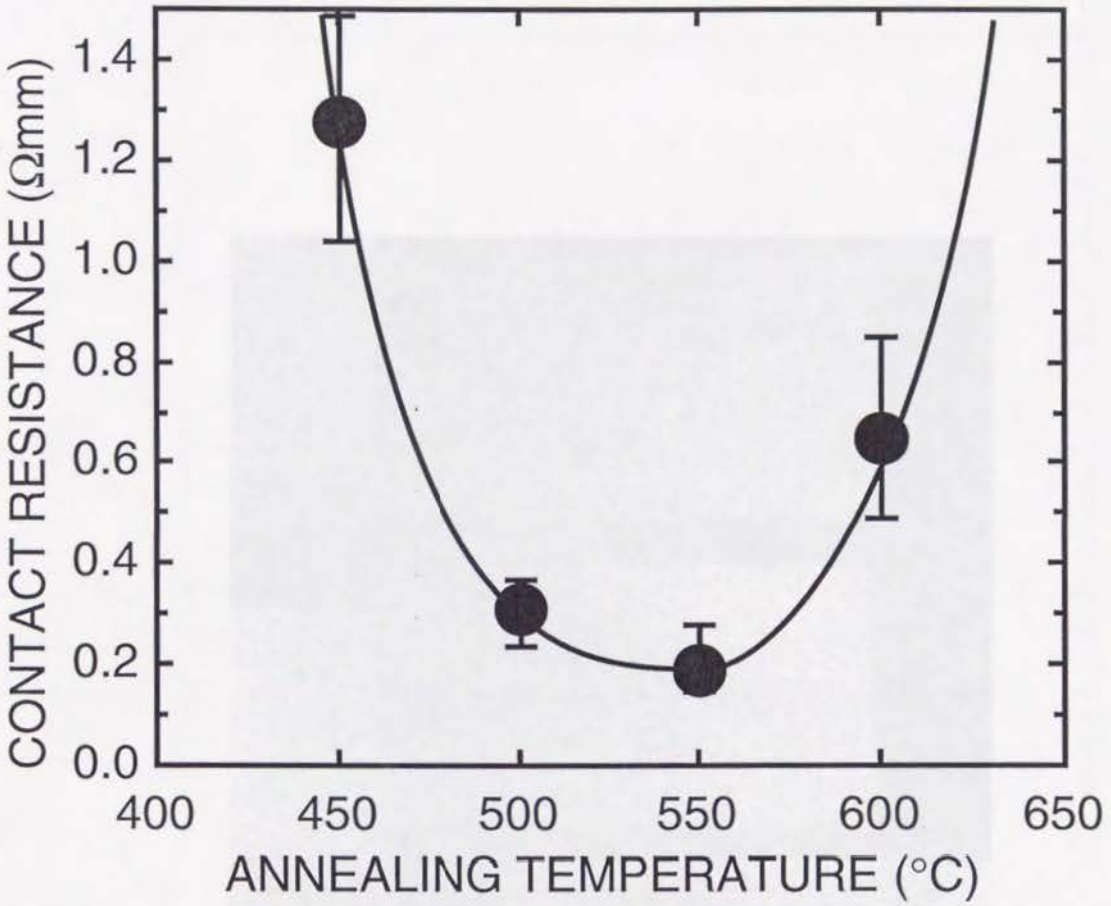

Fig. 4. 1 Contact resistances of $In_{0.7}Ga_{0.3}As/Ni/W_2N/W/Al$ contact annealed at various temperatures for 10 s.

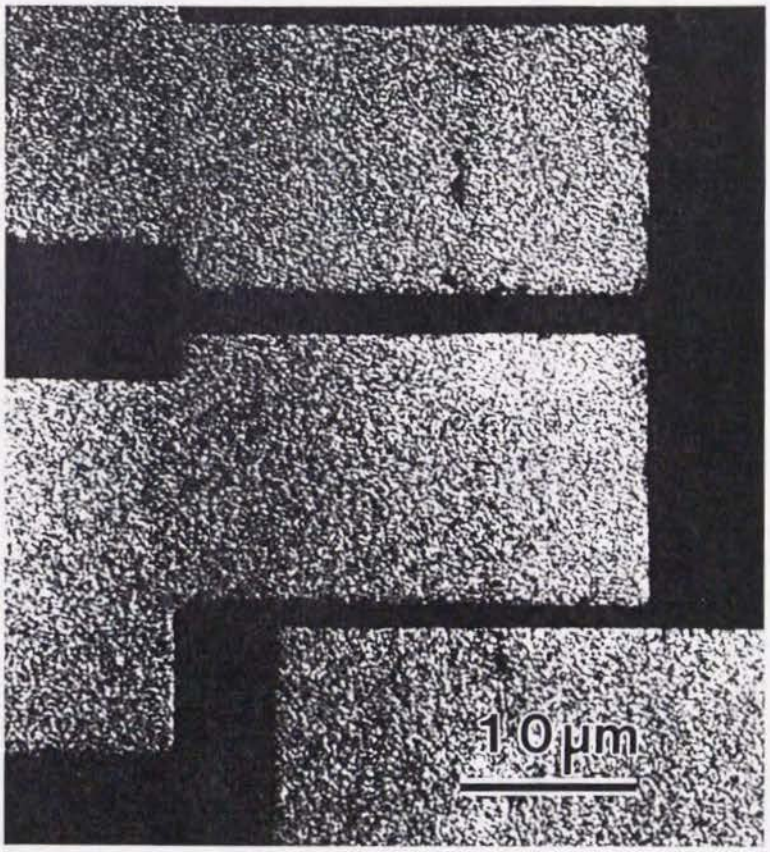

Fig. 4. 2 Optical micrograph of $In_{0.7}Ga_{0.3}As/Ni/W_2N/W/Al$ contact after annealing at 550 °C for 10 s.

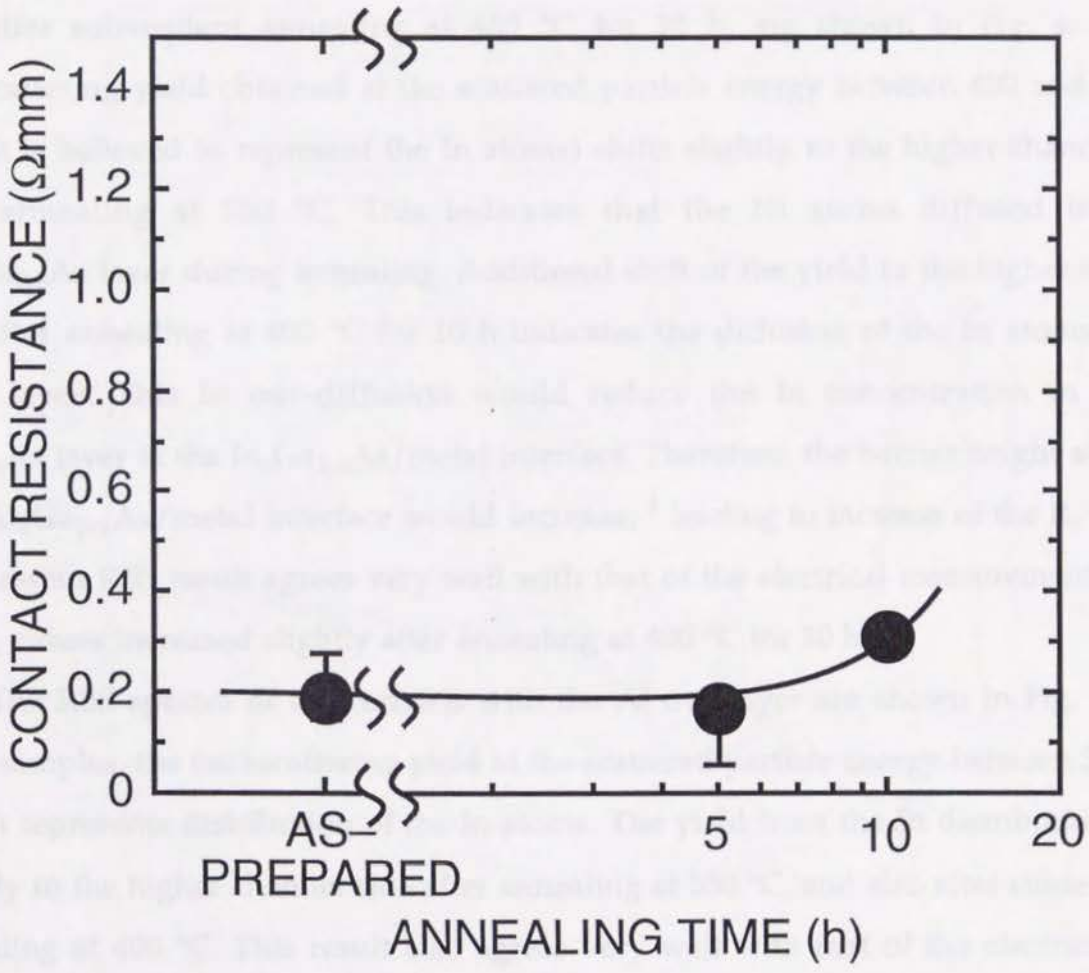

Fig. 4. 3 Contact resistances of $In_{0.7}Ga_{0.3}As/Ni/W_2N/W/Al$ contact during isothermal annealing at 400 °C.

also found in the contact without the Al overlayer. [2]

Since the electrical properties are sensitive to the In concentration in the $In_xGa_{1-x}As$ layer grown epitaxially on the GaAs surface after contact annealing, the In distribution at the metal/GaAs interface was analyzed by RBS. The RBS spectra of the contact without the Al overlayer before annealing, after annealing at 550 °C for 10 sec, and after subsequent annealing at 400 °C for 10 h, are shown in Fig. 4. 4. The backscattering yield obtained at the scattered particle energy between 400 and 420 ch (which is believed to represent the In atoms) shifts slightly to the higher channel side after annealing at 550 °C. This indicates that the Ni atoms diffused into the $In_{0.7}Ga_{0.3}As$ layer during annealing. Additional shift of the yield to the higher channel side after annealing at 400 °C for 10 h indicates the diffusion of the In atoms to the W_2N layer. This In out–diffusion would reduce the In concentration in the $In_xGa_{1-x}As$ layer at the $In_xGa_{1-x}As$/metal interface. Therefore, the barrier height at the n-type $In_xGa_{1-x}As$/metal interface would increase, [4] leading to increase of the R_c values. The present RBS result agrees very well with that of the electrical measurement where the R_c values increased slightly after annealing at 400 °C for 10 h. [2]

The RBS spectra of the contacts with the Al overlayer are shown in Fig. 4. 5. In these samples, the backscattering yield at the scattered particle energy between 380 and 400 ch represents distribution of the In atoms. The yield from the In distribution shifts slightly to the higher channel side after annealing at 550 °C, and also after subsequently annealing at 400 °C. This result also agrees very well with that of the electrical measurement. The present RBS results indicate that the formation mechanism of the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contact is not affected by the Al overlayer.

The RBS spectra of the contacts with the Cu layer are shown in Fig. 4. 6. Note that this contact did not show Ohmic behavior. The backscattering yield obtained at the scattered particle energy between 330 and 360 ch is believed to indicate the In distribution. The yield which indicates the In distribution shifts significantly to the higher channel after annealing at 550 °C. This result indicates that the In out–diffusion

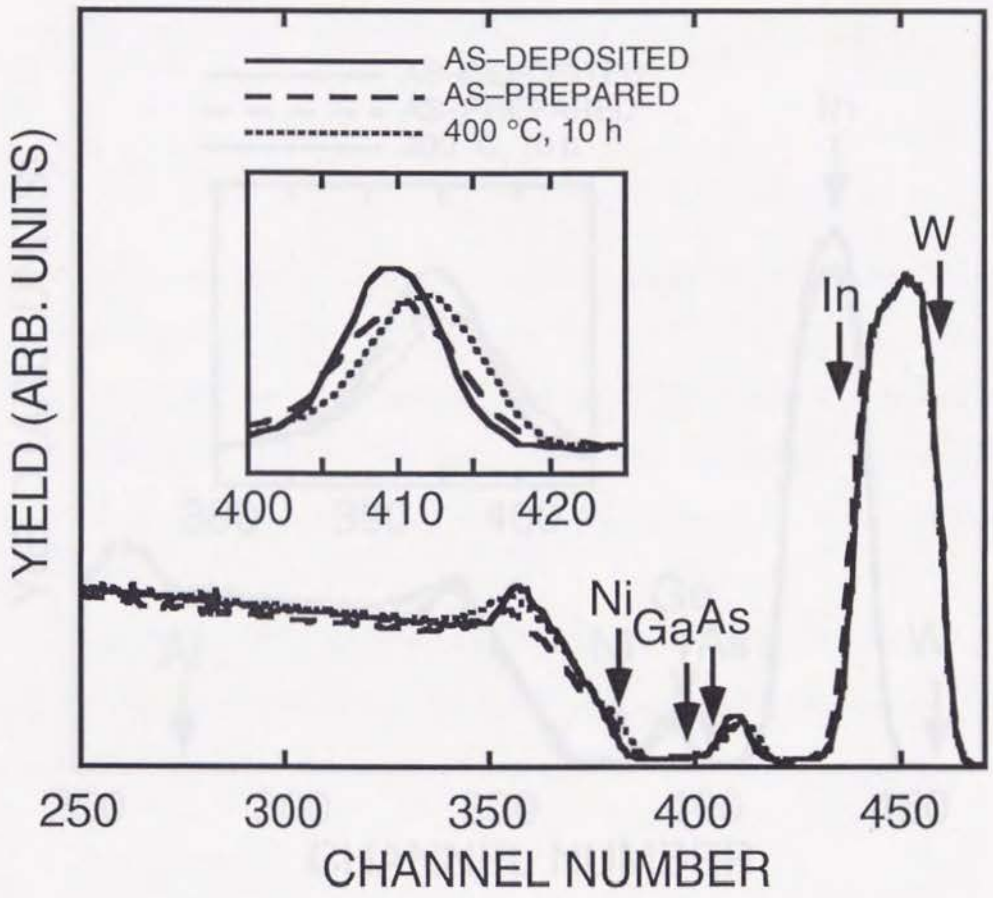

Fig. 4. 4 Rutherford backscattering spectra of $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contact as–deposited, as–prepared, and after annealing at 400 °C for 10 h.

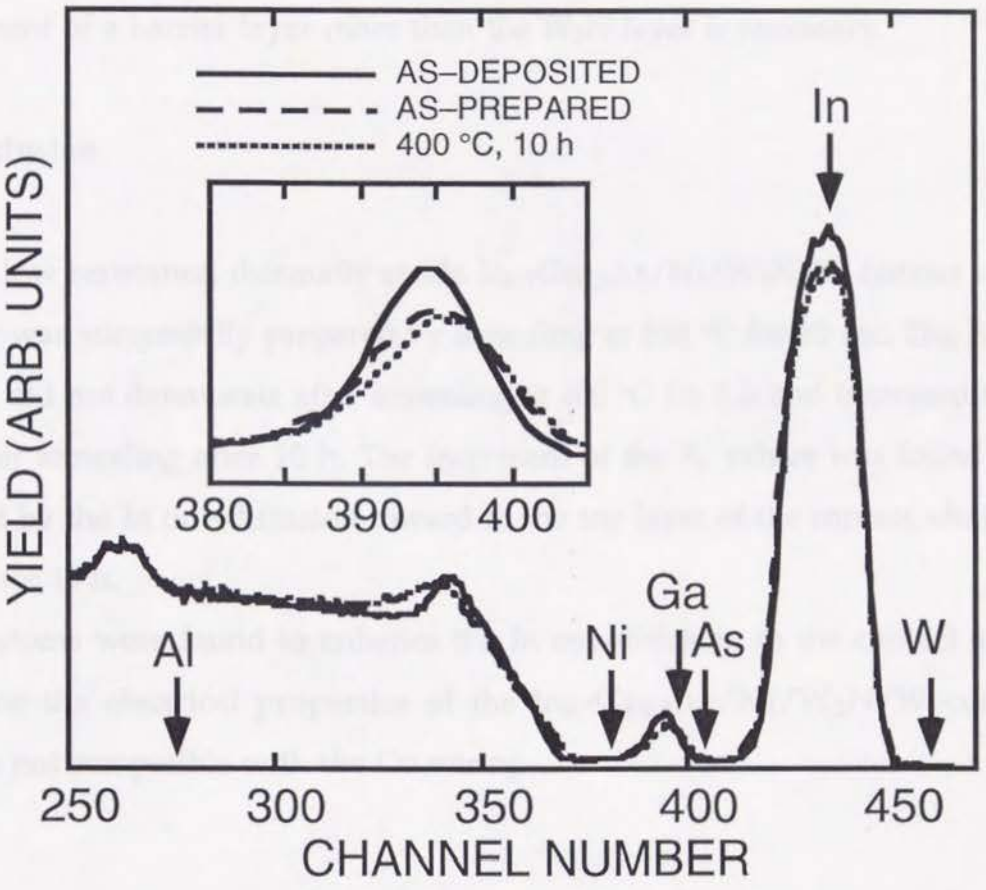

Fig. 4. 5 Rutherford backscattering spectra of $In_{0.7}Ga_{0.3}As/Ni/W_2N/W/Al$ contact as–deposited, as–prepared, and after annealing at 400 °C for 10 h.

through the W_2N layer was enhanced by the Cu atoms, because Cu and In are chemically reactive and form In–Cu compounds. (Note that the Cu–In compounds were not detected in the present study.) The out–diffusion of the In atoms to the metal surface reduces the total area of the $In_xGa_{1-x}As/GaAs$ interface, [2] leading to the increase of the R_c values. In order to reduce the In out–diffusion of the contacts with the Cu layer, development of a barrier layer other than the W_2N layer is necessary.

4. 4. Conclusion

The low resistance, thermally stable $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contact with the Al overlayer was successfully prepared by annealing at 550 °C for 10 sec. The R_c values of 0.2 Ωmm did not deteriorate after annealing at 400 °C for 5 h and increased by only 0.1 Ωmm after annealing after 10 h. The increment of the R_c values was found by RBS to be caused by the In out–diffusion toward to the top layer of the contact after annealing at 400 °C for 10 h.

Cu atoms were found to enhance the In out–diffusion to the contact surface and deteriorate the electrical properties of the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contact. This contact is not compatible with the Cu wiring.

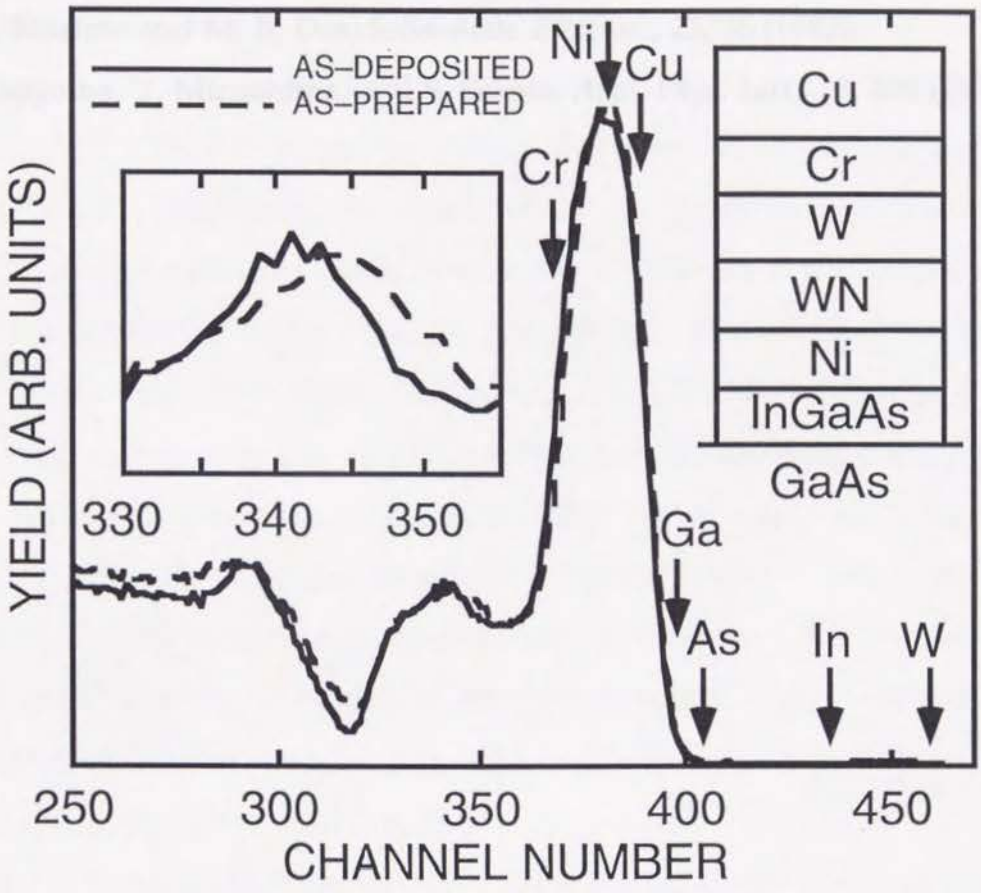

Fig. 4. 6 Rutherford backscattering spectra of $In_{0.7}Ga_{0.3}As/Ni/W_2N/W/Cr/Cu$ contact as–deposited and after annealing at 550 °C for 10 s.

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5. Summary of The Thesis

The low resistance, thermally stable $In_xGa_{1-x}As$–based Ohmic contacts were successfully developed by depositing an InGaAs and contact metals by using the radio frequency (rf) sputtering technique and by annealing in rapid thermal annealer (RTA).

In order to develop the $In_xGa_{1-x}As$–based Ohmic contacts, details of the formation mechanism of the previously developed InAs–based contacts were investigated. As a result of the microstructural analysis of the InAs/Ni/W contacts prepared with various deposition sequences, the effects of the Ni atoms on the formation mechanism were understood. The Ni atoms in the second Ni layer enlarged the $In_xGa_{1-x}As$/GaAs contact area by breaking the stoichiometry of the InAs compounds, resulting in low contact resistances. After the contact formation, the $In_xGa_{1-x}As$ layer was epitaxially grown on the GaAs substrate and the In composition x in the $In_xGa_{1-x}As$ layer at the metal/$In_xGa_{1-x}As$ interface was about 1.0 and about 0.5 at the $In_xGa_{1-x}As$/GaAs interface. The InAs/Ni/W contact provided the contact resistance (Rc) values of ~0.3 Ω–mm and excellent thermal stability. The contact resistance reduction was believed to be due to the increasement of the total area of the $In_xGa_{1-x}As$/GaAs interface and the reduction in the density of the crystal line defects formed at the $In_xGa_{1-x}As$/GaAs interface.

In order to understand the carrier transport mechanism of the InAs/Ni/W, the Rc values were measured at a various temperatures. Since the lowest R_c values were measured when the x values at the metal/$In_xGa_{1-x}As$ interface were about 1.0, the effective barrier to control the current flow was found to be the barrier at the $In_xGa_{1-x}As$/GaAs interface. The barrier height at the $In_xGa_{1-x}As$/GaAs interface of the InAs/Ni/W contact was evaluated to be 0.13 eV and the carrier transport mechanism was believed to be a thermionic field emission. This barrier would be formed due to about 4 % lattice mismatch between the $In_xGa_{1-x}As$ and the GaAs substrate.

Although the InAs/Ni/W contact provided low R_c values and excellent thermal

stability, the surface of this contact was rough and the reproducibility of the R_c values was poor. These deteriorations were found to be due to diffusion of large amounts of In atoms to the top W layer. In addition, formation temperatures of the InAs/Ni/W contacts were relatively high.

Reduction of the optimum annealing temperature for low Rc values and improvement of the surface morphology were achieved by depositing an $In_{0.7}Ga_{0.3}As$ layer instead of InAs. Formation temperatures of the $In_{0.7}Ga_{0.3}As/Ni/W$ contacts were reduced, resulting in smooth contact surface. However, the lowest Rc values of these contacts were almost same and the reproducibility of the Rc values was still poor, because the large amounts of the In diffused to the W surface.

The deterioration of the previous $In_xGa_{1-x}As$–based contacts developed in this study was improved after developing the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contacts, where the W_2N layer was expected to prevent the In out–diffusion and increase the contact area of the $In_xGa_{1-x}As/GaAs$ interface, resulting in reduction of the R_c values. This contact provided the lowest R_c values of 0.1 Ω–mm after annealing at 550 °C, the excellent reproducibility and the smooth surface. This R_c values did not change even after annealing at 400 °C for 5 h. The low Rc values were found to be due to the large total area of the $In_xGa_{1-x}As/GaAs$ interface. These improvements of the Ohmic contact properties were found to be due to deposition of the W_2N barrier layer for the In out–diffusion.

In addition, the low Rc values were measured and the excellent thermal stability was obtained in the $In_{0.7}Ga_{0.3}As/Ni/W_2N/W$ contacts with an Al overlayer, which indicates that this contacts are compatible with an Al wiring process. This low resistance, thermally stable Ohmic contacts prepared by only rf sputtering are desirable for the manufacturing GaAs devices and would be able to apply the current Si packaging process.

Appendix

In this section, the basic dvice characterisitcs of the GaAs MESFET will be explained first and then two device parameters g_m and f_{max}, which indicate the device performances, will be explained.

The schematic illustration of the GaAs MESFET and the equivalent circuits of the MESFET are shown in Figs. A. 1 (a) and 1 (b), respectively. When a positive voltage (V_D) is applied to the drain with respect to the source, a current (I_D) flows from the source to the drain. The current I_D is limited by the gate electrode with respect to the source. The basic current–voltage characteristics of the GaAs MESFET for variousdrain voltage for various gate voltages. These characteristics are divided to three regiion: the linear region, the saturation region, and the breakdown region. In the linear region, I_D increases as V_D increases. In the saturation region, I_D saturates at Idsat and is independent of V_D. Note that the slope of the I_D vs. V_D in the liear region, I_D increases rapidly with a slight increase of V_D.

In order to evaluate the device performance, the variation of the I_D value to the V_G value is defined as a transconductance g_m, where

$$g_m \equiv \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=\text{const}}$$

Since a large variation of the I_D value should be controlled by the small V_G value, a large g_m value is desirable for the high performance MESFET. When the current I_D flows from the drain to the source, and voltage drop is measured at the metal/semiconductor interface ($V_{contact}=I_DR_c$) and at the channel latyer ($V_{channel}=I_DR_c$), where R_c and R_{ch} is a contact resistnace and a chammel resistance, respectively. Therefore, the actually applied voltage to the gate electrode ($V_{G,\,appl}$) is expressed as

$V_{G,\,appl}=V_G-(V_{contact}+V_{channel})$.

Then the extrinsic g_m^{ext} value is expressed by the equation

$$g_m^{ext}=\frac{\partial I_D}{\partial V_G}=\frac{1}{\frac{\partial V_{G,appl}}{\partial I_D}+\frac{1}{\partial I_D}(\partial V_{contact}+\partial V_{channel})}=\frac{g_m^{int}}{1+(R_c+R_{ch})g_m^{int}},$$

where $g_m{}^{int}$ us an intrinsic value. In order to close the $g_m{}^{ext}$ value to the $g_m{}^{int}$ value, R_c and R_{ch} should be sufficiently low.

In order to operate a MESFET as a microwave device, the frequency response of the device is important. The frequency responce of the MESFET is limited by thte transit time of carriers to travel from source to drain and the RC time constant. The frequency f_T, corresponding to the transit time is expressed as

$$f_T=\frac{v_s}{2\pi L},$$

where v_s is a saturation velocity of the carrier and L is a gate length. The maximum frequency of ascillation f_{max} is given by

$$f_{max}\simeq\frac{f_T}{2\sqrt{r_1+f_T\tau_3}},$$

where r_1 is the input–to–output resistance ratio,

$r_1=(R_G+R_i+R_c+R_{ch})/R_{DS}$

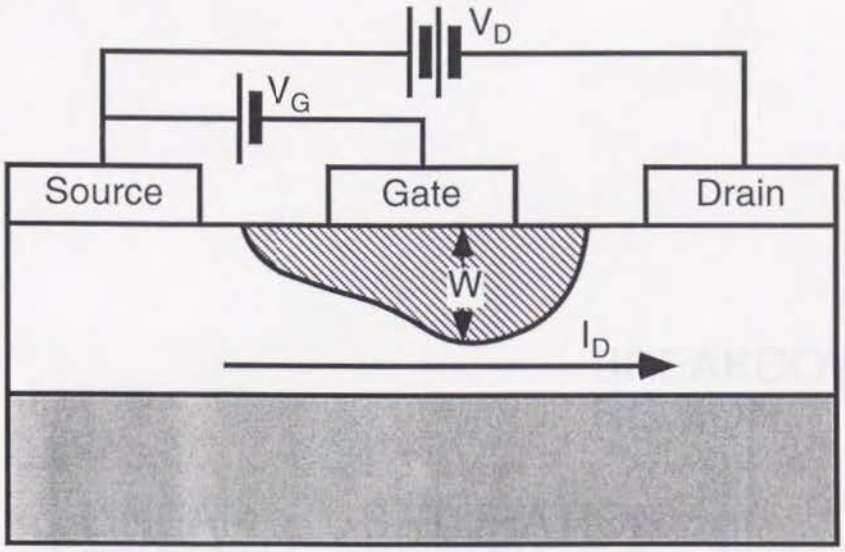
and τ_3 is a time constant

$\tau_3\equiv 2\pi R_G C_{DG}$.

In order to maximize f_{max}, reduction of the R_c and R_{ch} values is one of the effective approaches.

Based on the equation of g_m and f_{max}, reduction of the R_c value and the R_{ch} value was found to be necessary to improve the device performance. The T_{ch} value will be reduced with shrinking the devuce dimension, however, the R_c value increases with shrinking the device dimension. Therefore, development of the Ohmic contacts, which provide low contact resistance, is necessary.

A.1(a)



A.1(b)

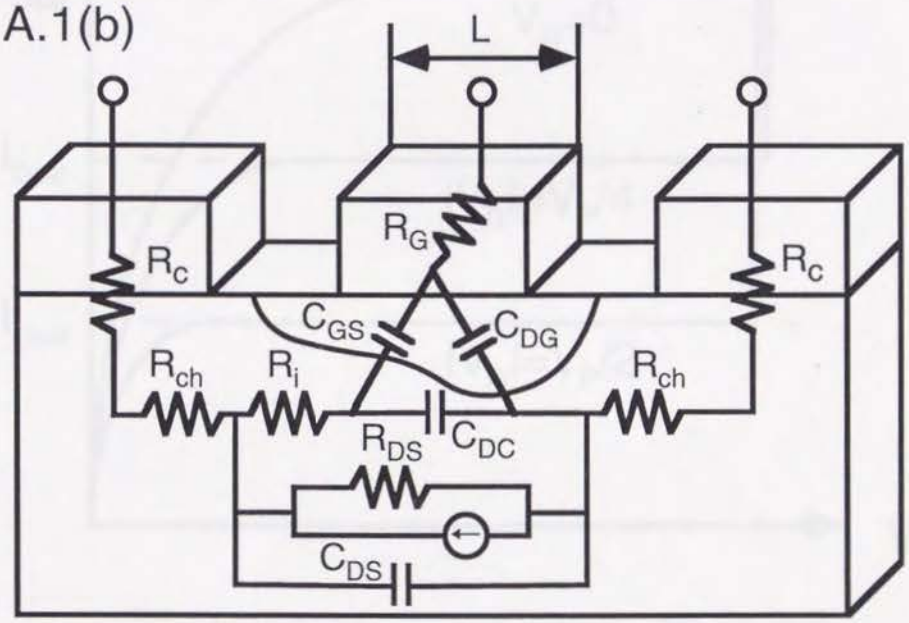


Fig. A. 1 (a) Schematic illustration of GaAs MESFET and (b) the equivalent circuits of the MESFET.

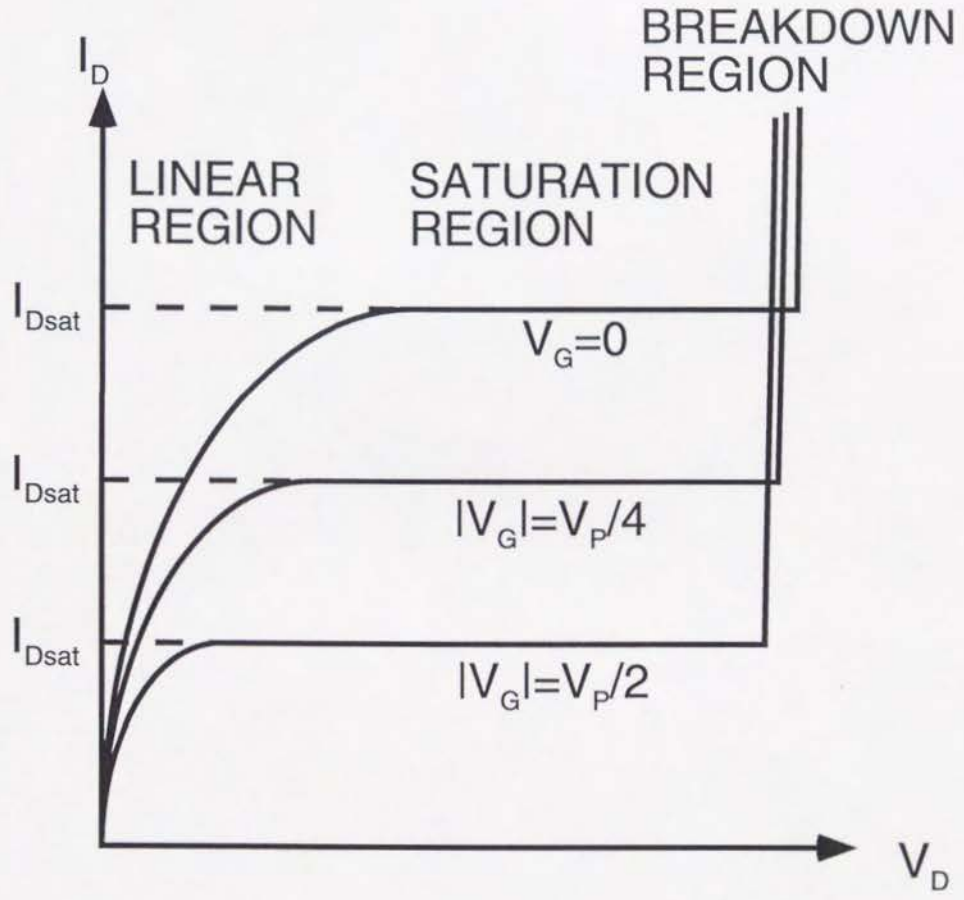


Fig. A. 2 Basic I–V characteristics of a MESFET, where V_P is a pinch–off voltage.