

Impact of Bias Temperature Instability and Random Telegraph Noise on CMOS Logic Circuits

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March 7, 2015

Acknowledgement

I would like to express my sincere gratitude to Professor Hidetoshi Onodera in Kyoto University for his appropriate guidance and valuable advices throughout this research. I would like to express my deepest gratitude to him for providing me a precious opportunity and an excellent environment to study as a doctoral student in his laboratory. I would like to thank Professor Takashi Sato, and Professor Naofumi Takagi in Kyoto University for their profitable advice on writing this thesis.

I would like to thank Professor Kazutoshi Kobayashi in Kyoto Institute of Technology for his valuable advices. I would like to thank Associate Professor Tohru Ishihara, and Assistant Professor Akira Tsuchiya in Onodera laboratory for their supports on this research. I would like to thank Ms. Seiko Jinno for her kind supports throughout my student life in Onodera laboratory. I would like to express my appreciation of active discussions from co-authors in Onodera laboratory; Mr. Hiroaki Makino, Mr. Kyosuke Ito, Mr. Atsushi Miki and Mr. Shohei Nishimura. I would like to express my appreciation to all students in Onodera laboratory.

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo, in collaboration with Semiconductor Technology Academic Research Center (STARC), e-shuttle. Inc., Fujitsu Ltd, and Renesas Electronics Ltd. This study is supported by VDEC, the University of Tokyo, in collaboration with Cadence Corporation, Mentor Graphics Corporation, and Synopsys Corporation. I would like to express my appreciation to all members of “Dependable VLSI Platform Using Robust Fabrics” research project in Japan Science and Technology Agency (JST), Core Research od Evolutional Science and Technology (CREST).

I would like to thank all of my friends for spending good time with me.

Finally, I give my thank to my family for their kind supports all the time.

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Chapter 1

Introduction

In this chapter, backgrounds and contributions of this thesis are described. In the first part of the chapter, modern LSI design issues are briefly described. Then, the scaling of LSI manufacturing process and various problems recently caused by the scaling are explained. In the third part of the chapter, reliability wearout in modern CMOS technology is described. Then objective and contributions of this thesis are summarized. The final part of this chapter describes the overview of this thesis.

1.1 Modern CMOS LSI Design Issues

Physical feature size of a transistor has been reduced continually over time. Leading edge products have a feature size of 14 nm in 2014. Due to the device miniaturization, the number of transistors in one processor exceeds several billion in 2014. On the other hand, designing reliable systems has become a big challenge in recent years. One of the dominant issues is a transistor performance variation. It can be classified into *static* variation and *dynamic* variation. Static variation is caused by Large Scale Integration (LSI) manufacturing process variation. Dynamic variation is caused by an environmental noise and an intrinsic device performance fluctuation. As a well-known example of dynamic variation, jitter in oscillators can be caused by both environmental and intrinsic device noise. Another example of dynamic variation is a gradual LSI performance degradation or a temporal LSI performance fluctuation. They are known as LSI reliability problems. Transistor reliability has a great impact on modern CMOS circuits. The quality of the interface between gate oxide and silicon substrate is one of the key factors for highly-reliable circuit operations. This thesis deals with LSI reliability issues caused by a gradual performance degradation in transistor and a temporal noise in transistor.

1.2 Scaling of LSI Manufacturing Process

It has been more than fifty years since the invention of the Integrated Circuit (IC) technology. Metal Oxide Semiconductor Field Effect Transistor (MOS-FET) is a key device of modern LSI technology. After the invention of the first planar IC by Fairchild in 1960, IC technology has been scaled by Moore's law and now the complexity is doubling every 18 months[1]. Transistor performance factors can be increased by miniaturization and it is called scaling law[2, 3]. Physical feature size of a transistor has been reduced continually over time.

Table 1.1 shows the device and circuit parameter change by two ideal scaling methods. The electric potential inside the transistor is the same after device parameters in Table 1.1 are changed by these scaling methods. Lateral sizes of a transistor such as the gate length (L), the gate width (W) and vertical sizes of a transistor such as the gate oxide thickness (t_{ox}), the junction depth (x_j) are reduced by $1/k$ times ($k > 1$). Constant field scaling is done by keeping the electric field inside the transistor constant. The substrate doping concentration (N_A) is increased by k times and the operating voltage (V) is reduced by $1/k$ times for the constant field scaling. As a result, the circuit delay (d) and the power dissipation (P) decrease $1/k$ and $1/k^2$ times respectively. The number of transistors (the integration density) increases by k^2 times. As for the constant voltage scaling, N_A is increased by k^2 times and V is kept constant. As a result, d decreases by $1/k$ times and P is kept constant. The number of transistors increases by k^2 times. The transconductance (G_m) that represents the driving capability of a transistor is kept constant for both scaling methods. Owing to the scaling, the logic circuit becomes k times faster and its integration density

Table 1.1: Device and circuit parameter change by scaling

Device or Circuit Parameter	Constant Field Scaling	Constant Voltage Scaling
Gate length L , Gate width W	$1/k$	$1/k$
Gate oxide thickness t_{ox}	$1/k$	$1/k$
Junction depth x_j	$1/k$	$1/k$
Substrate doping concentration N_A	k	k^2
Voltage V	$1/k$	1
Current I	$1/k$	1
Transconductance $G_m = I/V$	1	1
Gate capacitance C	$1/k$	$1/k$
Delay $d = CV/I$	$1/k$	$1/k$
Power dissipation $P = VI$	$1/k^2$	1
Power density P/LW	1	k^2
Number of transistors	k^2	k^2

becomes k^2 times larger. When the value of $1/k$ is kept 0.7, the density is doubled for every generation and IC technology actually has been developed exponentially. The exponential growth of IC technology has great impact on our lifestyle and the research and development of Very Large Scale Integration (VLSI) technology is intensively done in the world.

As already described in the previous section, several problems have recently appeared in VLSI technology developments because more than a billion transistors have been integrated in one chip. Transistors function as switching elements in logic circuits even under a manufacturing process variation. But the whole circuit may fail to operate due to a timing violation. The process variation problems are briefly discussed in Section 2.1. We deal with a reliability problem caused by intrinsic noise in transistor. A whole LSI may randomly fail to operate in a short time due to a temporal transistor performance fluctuation, although it operates correctly most of the time. As another case, a whole LSI may fail to operate suddenly after several years of operation due to transistor performance degradations. It is well known today that Hot Carrier Injection (HCI)[4, 5], Bias Temperature Instability (BTI)[6, 7, 8], Time Dependent Dielectric Breakdown (TDDB)[9], and Random Telegraph Noise (RTN)[10, 11] are main issues in transistor gate oxide reliability. Transistor reliability has a great impact on modern CMOS circuits and the quality of the interface between gate oxide and silicon substrate is one of the key factors for highly-reliable circuit operations.

In the next section, reliability wearout problems in modern CMOS technology are briefly summarized.

1.3 Reliability Wearout in Modern CMOS Technology

Due to the recent aggressive technology scaling, it becomes difficult to guarantee the quality of billions of transistors in one chip. A great deal of effort has been made to realize reliable products from a device level to a circuit and a system levels. In a reliable product, the system can operate correctly even though there are some unreliable components. The system performance is kept to be more than an acceptable level all the time. There are several reliability problems that still remain unresolved for realizing a reliable LSI. In this section, MOSFET reliability problems related to the transistor-gate-oxide-insulator are briefly described. HCI, BTI, and RTN are main reliability issues related to the property of the interface between gate oxide insulator and silicon substrate. Figure 1.1 shows how these factors have appeared as CMOS technology scales. CMOS technology scaling causes new gate oxide reliability issues. Before 180 nm technology, gate oxide is SiO_2 and main reliability issue is HCI. In 90 to 65 nm technology, nitridation of gate oxide is introduced. As a result, Negative Bias Temperature Instability (NBTI) becomes the main issue. It is reported that the increase of the nitrogen content at the SiO_2/Si interface promotes the NBTI[12,

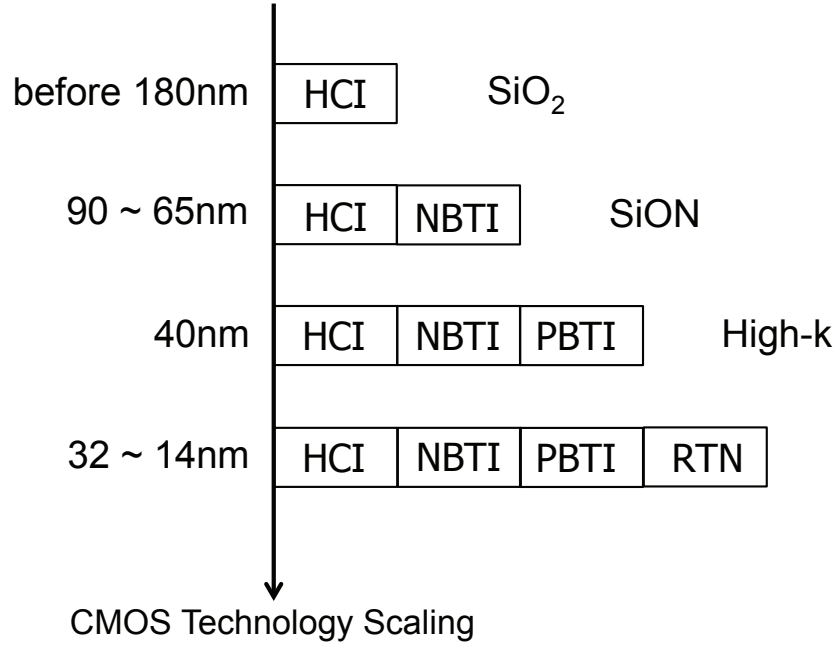


Figure 1.1: Various gate oxide reliability issues in CMOS technology scaling.

13]. When High-k material is introduced in 40 nm technology, Positive Bias Temperature Instability (PBTI) also becomes an issue. As technology further scales to 32 to 14 nm generation, RTN appears as a new issue. BTI and RTN have a big impact on modern CMOS technology.

The values of critical transistor parameters such as the drain current (I_{ds}) and the threshold voltage (V_{th}) gradually shift with time by HCI and BTI. It is reported that V_{th} -shift, ΔV_{th} , follows power-law with stress time, t , in a moderate NBTI-stressed condition

$$\Delta V_{th} \propto t^n \quad (1.1)$$

as shown in Fig. 1.2(left). By RTN, V_{th} discretely fluctuates temporary as shown in Fig. 1.2(right). All these phenomena can be caused by charge trapping into the gate oxide insulator. When billions of transistors are integrated in one chip, the probability that a transistor is not reliable increases. If the size of transistor and the thickness of a gate oxide can be increased, HCI, BTI, RTN, and TDDB have less impact on the circuit operation. This is because the electric field in a gate oxide is relaxed by thicker gate oxide and the impact of one charge trapped in the oxide becomes less by larger gate area. On the other hand, there is a strong demand for high performance transistor. There is a severe trade-off between high-reliability and high-performance. Due to this trade-off, a great effort has been made to clarify the gate oxide wearout mechanisms at the device

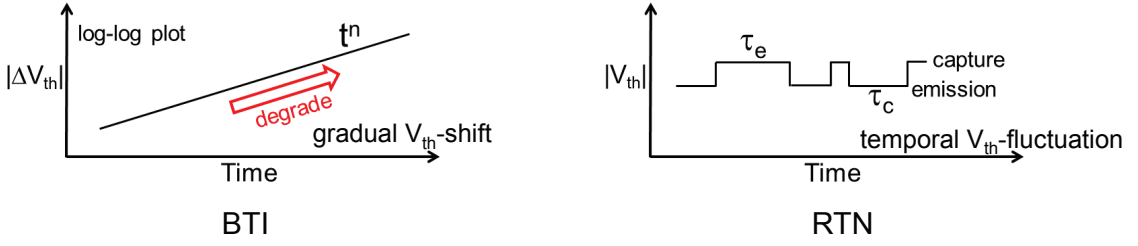


Figure 1.2: (left) Gradual threshold voltage shift by BTI. (right) Temporal threshold voltage fluctuation by RTN.

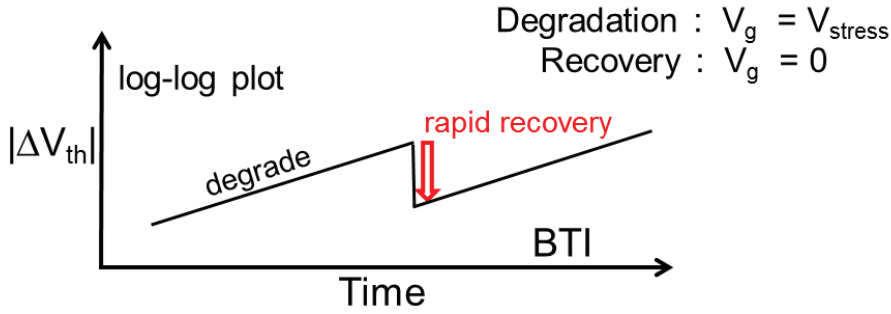


Figure 1.3: Threshold voltage degradation by NBTI with rapid recovery phase.

level, to achieve both high reliability and high performance.

BTI and RTN have been intensively investigated topics in recent years. As for NBTI, NBTI recovery phenomenon has been investigated thoroughly in recent ten years[14, 15, 16, 17, 18, 19]. When NBTI stress is removed or relaxed, degraded V_{th} rapidly starts to recover. As shown in Fig. 1.3, recovered V_{th} starts to degrade again after NBTI stress is resumed. V_{th} -shift with stress time becomes complex curve due to NBTI recovery after several stress-relax-stress cycles. Until now, there is still a controversy over the NBTI mechanism due to its recovery phenomenon[18, 19]. Measuring rapid NBTI recovery and predicting how NBTI recovers have been big challenges. As a result, it is also difficult to predict V_{th} -shift after complex stress-relax-stress cycles. On the other hand, the impact of RTN fluctuation with respect to within-die process variation is considered to be larger for further scaled technologies in the future. It was predicted in the past that the impact of RTN-induced fluctuation might exceed manufacturing process variation in 22 nm technology[20].

The impact of the gate oxide insulator reliability on the circuit level has attracted much attention these days inspired by intensive researches on device level reliability. The impact of BTI and RTN has been widely investigated for circuits that have a great number of small size transistors in one chip. As for

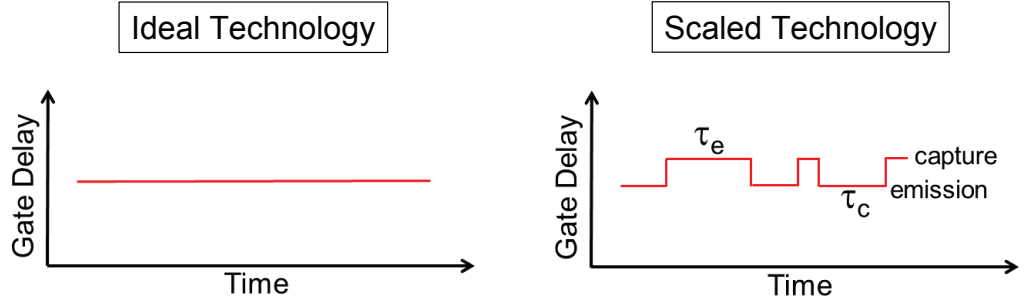


Figure 1.4: V_{th} versus gate delay. (left) in an ideal technology. (right) in a scaled technology.

BTI, there is a strong demand for a degradation model of circuit simulation that includes recovery phenomenon based on the high-speed BTI characterization. As for RTN, the impact of RTN on a logic circuit has not been well known. In an ideal technology, V_{th} does not fluctuate with time. It is a constant value. Thus the gate delay does not fluctuate with time. But in a scaled technology, the gate delay fluctuates discretely with time as shown in Fig. 1.4. Further discussions are made in Sections 2.2 (BTI), and 2.3 (RTN).

In this thesis, fast NBTI characterization results towards circuit simulation are described. Then, we propose an LSI lifetime extension method based on the self-healing of the NBTI-induced degradation. Finally, for the first time, the impact of RTN on a logic circuit is clarified based on measurement data. The impact of RTN fluctuation with respect to within-die process variation is discussed in the final part.

1.4 Objective and Contribution of This Thesis

The objective of this thesis is to clarify the impact of recent CMOS transistor reliability issues on a CMOS circuit operation. This thesis focuses on BTI and RTN as recent transistor reliability issues because they have appeared as threats in modern scaled CMOS technologies. Circuit designers who try to make their circuits more reliable can find fruitful results in this thesis. The objective is divided into the following two topics.

- To clarify how NBTI recovery occurs at transistor level and how an LSI operation is affected by NBTI recovery.
- To clarify whether a CMOS logic circuit operation is seriously affected by RTN.

The contribution of this thesis is as follows, corresponding to the objective described above.

- NBTI recoveries under various recovery conditions are found to follow one simple curve. Considerable recovery is found to be realized in a few hours under some condition in our test chip. Making the most of NBTI recovery, the concept of a multi-core LSI lifetime extension method is proposed.
- Even for a combinational circuit, its operation under a low supply voltage is for the first time found to be affected seriously by RTN. How circuit designers can decrease the impact of RTN on a combinational circuit is shown.

All discussions are based on measurement data fabricated in a commercial 65 nm and 40 nm CMOS technologies. This thesis greatly contributes to realize a reliable LSI even under various threats in present and future CMOS technologies.

1.5 Overview of This Thesis

In the following chapters, the impact of NBTI and RTN on a CMOS circuit operation is clarified. It helps circuit designers to consider how an LSI operation is affected by NBTI recovery. Also, it greatly helps circuit designers to consider how to suppress the impact of RTN at a circuit level. Discussions are based on measurement results from 65 nm and 40 nm test chips.

Process variation has been a dominant cause to prevent VLSI dependability until now. But the impact of transistor reliability has become larger and larger in these fifteen years. Chapter 2 describes transistor performance fluctuation in CMOS technology. An overview on transistor performance fluctuation with respect to process variation and reliability is given in Section 2.1. It is described that HCI, BTI, TDDB, and RTN are main issues related to the gate oxide reliability in modern CMOS technology. These four issues are caused by carriers trapped into the gate oxide. Sections 2.2 and 2.3 include discussions about transistor reliability and its impact on circuits with respect to NBTI and RTN.

Chapters 3 and 4 deal with NBTI. Chapter 3 describes NBTI degradation and recovery characterization at a transistor level. Results are summarized based on fast NBTI characterization methods. Section 3.1 describes issues on NBTI characterization. Section 3.2 describes NBTI characterization by Measure-Stress-Measure (MSM) method. By using the fast MSM method, NBTI recoveries under various recovery conditions are found to follow one simple curve. More than 80% of NBTI degradation is found to recover in a few hours under zero gate bias condition. But 10 to 20% of the degradation remains as a slowly recoverable or a permanently unrecoverable component. A transistor degrades during a recovery measurement in the MSM method. Thus the fast Leakage Current (LC) method is proposed in this thesis. Section 3.3 shows that the LC method has the highest fidelity to NBTI recovery measurement. The LC method has no degradation during the recovery measurement. NBTI recovery measurement results by the fast LC method with 400 ns measurement delay are shown. NBTI recovery monitored by the leakage current is found to follow $\log t_{\text{recovery}}$ where t_{recovery} is the recovery time. It is confirmed for the

first time in the region of $400 \text{ ns} \leq t_{\text{recovery}} \leq 30 \text{ ms}$. Chapter 3 gives the information of the recoverable and the permanent component in NBTI degradation. Making the most of NBTI recovery, Chapter 4 describes a multicore LSI lifetime extension method. Section 4.1 describes the concept of LSI lifetime extension by NBTI recovery based self-healing. It is applied to a multicore LSI lifetime extension in Section 4.2. Combined with NBTI recovery, circuit parallelization plays an important role for the lifetime extension. It is shown that transforming silicon area into LSI lifetime is a promising and realistic concept.

Chapters 5 and 6 deal with RTN. Chapter 5 describes RTN characterization of CMOS transistors. It is shown that RTN-induced transistor current fluctuation can be strongly influenced by both the gate bias and the substrate bias. Chapter 6 describes the impact of RTN on CMOS logic circuit performance. The impact of RTN on CMOS logic circuit reliability is described based on our results from 40 nm test chips. Section 6.1 describes the test structure for RTN evaluation. In Section 6.2, it is shown for the first time that the impact of RTN can be a serious problem even for combinational circuits when they are densely integrated and operated under low supply voltage. But the impact of RTN fluctuation can be drastically reduced when supply voltage, gate area, and number of stages are increased. By this Section 6.2, circuit designers can know quantitatively how the RTN impact on combinational circuits can be decreased by choosing proper circuit parameters.

Chapter 2

Transistor Performance Fluctuation in CMOS Technology

In this chapter, transistor performance fluctuation in CMOS technology is described. Section 2.1 starts with an overview on transistor performance due to process variation. Recent fruitful research results on NBTI and RTN owe to previous HCI and TDDB researches. A brief overview on HCI and TDDB is given in the final part of Section 2.1. The last two sections describe transistor reliability and their impact on circuit with respect to NBTI and RTN.

2.1 Transistor Performance Fluctuation: Variability and Reliability

Designing reliable systems has become more difficult in recent years. Besides conventional problems such as transistor leakage, reliability and variation of transistor performance have a severe impact on the dependability of VLSI systems[21, 22, 23, 24, 25]. Process variation has been a dominant cause to prevent VLSI dependability until now. In the first part of this section, various problems on manufacturing process variation are introduced. The impact of transistor reliability with respect to gate oxide has become larger and larger in these fifteen years. Thus clarifying the impact of reliability with respect to manufacturing process variation has much attraction in recent LSI developments[26]. It is because circuit designers can obtain a useful information when they try to suppress various reliability problems. Reliability problem such as RTN is considered to have larger impact on future scaled technologies. As one of the main results of this thesis, the impact of RTN on logic circuits with respect to that of process variation is clarified in Chapter 6. How the impact of RTN is suppressed is shown in this thesis. In the previous chapter, it is described that HCI, BTI,

TDDDB, and RTN are main issues related to the gate oxide reliability in modern CMOS technology. HCI is an old problem and some problems still remain to be unsolved. Although HCI degradation still remains an issue in transistor reliability, its impact has become smaller than that of NBTI in recent lower supply voltage CMOS technologies[27]. In this section, a brief introduction is made about HCI. Previously, intensive HCI researches were made on how a charged carrier is trapped to the defect in the SiO₂ gate oxide[28]. BTI and RTN are also induced by a charged carrier that is trapped into a gate oxide. Detailed studies on the physical property of defects in the SiO₂ oxide help to investigate defects in modern SiON and High-k gate oxides[29]. Researches on BTI and RTN are done when the gate oxide works as insulator. When the gate oxide loses its property as insulator, TDDDB dominates the gate oxide reliability. TDDDB is triggered by a carrier trap into the gate oxide. This thesis deals with BTI and RTN where TDDDB does not become a dominant issue. A brief introduction of TDDDB is made in the final part of this section. As main topics of this thesis, detailed discussions on Negative Bias Temperature Instability (NBTI) and RTN are made in Sections 2.3 and 2.4 respectively.

First, process variation problems are described. The manufacturing variability is not a new problem and it has been always an issue in circuit design. Transistor variation can be categorized into two cases. One is the global variation such as lot-to-lot, wafer-to-wafer, and die-to-die variation. The other is the local, Within-Die (WID) variation. In an old CMOS technology, only global variations matter and they can be handled by corner-based circuit design.

The global variation is mainly caused by uncontrollabilities in manufacturing equipments. As the technology scales, these uncontrollabilities also should be suppressed because the impact of process variation becomes larger in a small size device.

On the other hand, WID variation has been major concerns in recent CMOS technologies due to the aggressive miniaturization and the introduction of various new technologies. Suppressing the impact of WID variation remains to be a very difficult task but statistical design methodologies such as statistical timing analysis have been intensively researched[30, 31, 32, 33] from the circuit designer side. WID variation consists of a layout-dependent variation and a random variation. The layout-dependent variation is caused by a lithography and etching patterning process, temperature variation during rapid thermal annealing[34, 35, 36], and stress variation in strained silicon technology[37, 38, 39, 40, 41, 42]. The random variation is caused by process uncertainties that vary in a smaller scale compared to the transistor size. Such a small scale process uncertainty is called intrinsic parameter fluctuation[43]. The gate length varies by the gate Line-Edge-Roughness (LER)[44, 45] and its impact becomes larger in small size devices. Gate poly-silicon granularity[46] and interface state fluctuation[47] also induce transistor performance variation. Variation in number and position of dopant atoms in MOSFETs induces threshold voltage fluctuation from device to device[48, 49, 50]. It is called Random Dopant Fluctuations (RDF). The impact of transistor mismatches becomes increasing due to RDF. The standard

deviation of a threshold voltage, $\sigma(V_{th})$, usually satisfies the relationship

$$\sigma(V_{th}) = \frac{A_{VT}}{\sqrt{LW}}, \quad (2.1)$$

where L is the gate length and W is the gate width and A_{VT} represents the slope normalized with respect to the square root of the transistor gate area LW [51]. To further take into account the effects of different transistor designs,

$$\sigma(V_{th}) = B_{VT} \sqrt{\frac{t_{oxe}(V_{th} - V_{FB} - 2\phi_F)}{LW}}, \quad (2.2)$$

is reported[52] where a coefficient B_{VT} is introduced. Here t_{oxe} is electrical gate oxide thickness and V_{FB} is flat band voltage and ϕ_F is Fermi potential. If the random variation, $\sigma(V_{th})$, is dominated solely by the dopant fluctuation, B_{VT} is constant regardless of t_{oxe} and V_{th} . If the random variation is affected by other reasons in addition to the dopant fluctuation, B_{VT} takes different values from fab to fab.

In the design of analog circuits, the matching of transistors often plays an important role[53, 54, 55, 56]. If $\sigma(V_{th})$ is large, it becomes difficult to guarantee the threshold voltage difference of pair transistors within an acceptable level. The random variation of a transistor performance also has a severe impact on SRAM design. Integrating transistors as much as possible is important for SRAM design, and smaller size transistor compared to a logic circuit is used for an SRAM memory cell. To measure the stability of an SRAM cell against an external or an internal noise, static noise margin (SNM) is often used[57, 58]. When the supply voltage decreases and the random variation increases, SNM becomes smaller and it becomes difficult to guarantee the stability of SRAM cells in a whole chip. In the design of digital circuits, the propagation delay of a logic circuit varies by the random variation. It is necessary to set some timing margin for a synchronous circuit to guarantee the circuit function under the delay variation.

Next, reliability problems are described. HCI occurs when electrons or holes in a channel are accelerated by the electric field and get the energy enough to go into the gate oxide[4, 5]. By HCI, critical transistor parameters, such as the drain current (I_{ds}) and the threshold voltage (V_{th}), shift with time gradually. HCI is observed in both nMOSFET and pMOSFET. The degradation by HCI becomes worst in nMOSFET because the mobility of electron is higher than hole in MOSFETs. In a longer channel transistor, the degradation becomes larger in a lower temperature because the mean free path and the mobility of a carrier are increased due to the reduction of phonon scattering. In a shorter channel transistor such as $L = 0.25\mu\text{m}$, however, larger degradation is observed at low V_{ds} when temperature becomes higher[59]. HCI is pronounced during the signal transition in a logic circuit due to the short-circuit current between power supply rails and ground rails. To suppress HCI, too slow signal transition is usually prohibited and checked in a logic design phase. It is very important to predict HCI-induced circuit degraded behavior by a circuit simulation. The

first attempt to such simulator was developed at UC Berkeley and it is called Berkeley Reliability Tools (BERT)[60, 61, 62]. The methodologies incorporated in BERT became the de facto standard for circuit-level reliability simulations and widely used in EDA vendors[63, 64]. In a modern CMOS technology, the operation voltage of a core logic circuit is around 1 V and the impact of HCI is larger in I/O transistors that use higher voltages such as 3.3V, 2.5V, and 1.8V. In recent fifteen years, much of the active work on HCI has turned to BTI. Detailed discussion on NBTI is done in Section 2.2.

In the following, TDDB is discussed as the final topic in this section. Defects inside the gate oxide insulator are generated by the electric field in the oxide. Small amount of current can flow in the gate insulator by the electric field. It is considered that the defects generated by the current trigger the oxide breakdown. The relation between the generated defects and the oxide breakdown is usually explained statistically by the percolation model[9, 65]. In [65], the defects are modeled by conductive spheres that are generated randomly in the oxide insulator. The breakdown is triggered when a path of overlapping spheres connects the two electrodes. The percolation model predicts that the time necessary to breakdown the oxide follows Weibull distribution

$$F = 1 - \exp \left[- \left(\frac{t_{BD}}{\eta} \right)^\beta \right] \quad (2.3)$$

or

$$\ln [-\ln (1 - F)] = \beta(\ln t_{BD} - \ln \eta). \quad (2.4)$$

F is the cumulative distribution function and means the probability that an gate oxide breaks within the time of t_{BD} . β is called Weibull slope and usually $\ln [-\ln (1 - F)]$ is plotted as a function of $\ln t_{BD}$. It is called Weibull plot. The percolation model predicts the Weibull slope, β , lineally decreases with decreasing oxide thickness and it is in agreement with the experimental data[66]. In a scaled device, the probability that a transistor has a shorter lifetime increases because of a small β value.

2.2 NBTI and its Impact on Circuits

In this section, gate oxide reliability with relation to NBTI is described. NBTI is one of the strongest reliability concerns in recent CMOS technology that is related to a physical property of a very thin gate oxide insulator[7, 8]. NBTI occurs mainly in pMOSFET. The application of negative bias on pMOSFET causes a shift of its threshold voltage V_{th} . Figure 2.1 shows the typical bias configuration during NBTI stress. V_g is set to a negative bias below V_{th} (inversion mode) and V_s, V_d, V_{sub} are 0 V. Since NBTI is driven by the presence of holes in the channel, V_{th} shift also occurs in an nMOSFET in accumulation mode ($V_g < 0$). It is reported that the magnitude of V_{th} shift due to NBTI is much larger in the case of pMOSFET than that of nMOSFET under the same V_g at

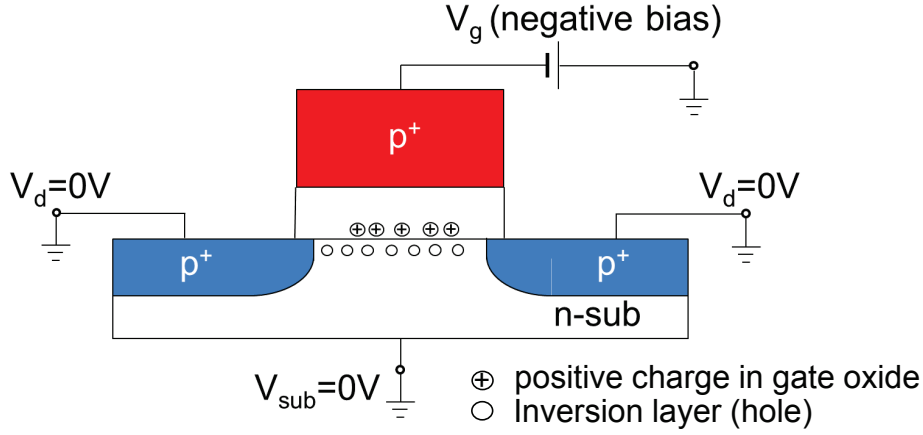


Figure 2.1: Typical bias configuration during NBTI stress.

stress[67, 68]. NBTI is worst in pMOSFET in inversion mode for modern CMOS technology under the same V_g at stress. NBTI is accelerated by the oxide electric field E_{ox} (5 – 8 MV/cm) and elevated temperature (100 – 200 °C). NBTI was observed since the early phases of MOSFET development. For example, Dr. B. E. Deal *et al.* in Fairchild reported NBTI of thermally oxidized silicon in 1967[6]. It was seven years after the invention of first planar IC. Although NBTI was not considered of any reliability concern until 1990s, the impact of NBTI becomes larger since 2000 due to the aggressive CMOS scaling.

The slower scaling of operating voltage compared to more aggressive scaling of gate oxide thickness has increased the E_{ox} . The magnitude of E_{ox} is more than 5 MV/cm after the year of 2000[7]. NBTI is accelerated during normal IC operation. Due to the excessive power dissipation of modern CMOS chips, there are hotspots on a chip that reflect the power distribution on the chip. The hotspot temperature reaches as high as 100 °C in a modern chip[69]. NBTI is also accelerated in a usual chip operation around the hotspot.

The introduction of the nitridation processes into the gate oxide in 90 nm CMOS node is another reason for enhancing the impact of NBTI. It can reduce both the gate leakage current and boron penetration from the p^+ -polycrystalline-silicon gate into the underlying silicon substrate of pMOSFET. Nitridation processes of gate insulator have been developed since 1970s[70, 71, 72] and widely used after 65 nm CMOS technologies. The impact of NBTI becomes larger by the increase of the nitrogen content at the SiO_2/Si interface[12, 13].

A remarkable phenomenon regarding NBTI is that the degraded performance of a pMOSFET transistor recovers when the bias temperature stress applied to the gate oxide is removed or relaxed[14, 15, 16, 17]. Despite the extensive research on NBTI, there is still a controversy over the NBTI mechanism due to the recovery phenomena[18, 19]. There is a strong demand for the practical

compact model that can treat NBTI and other reliability issues in the circuit simulation[62, 73, 74]. Compact model extracts parameters from experimental data. Monitoring NBTI at a circuit level helps to check the quality of the compact model. When a logic path suffers from NBTI, its delay increases gradually. A ring oscillator frequency degradation by NBTI is measured by using the beat frequency of two oscillators where one of them is under degradation[75, 76]. A ring oscillator based NBTI monitor circuit is proposed that uses the pulse-width-change depending on the difference between the rise and fall propagation delays[77]. Another circuit uses a delay-locked loop to monitor a logic path delay degradation[78]. It detects the control voltage of a voltage-controlled delay line that varies with respect to the monitored path delay variation[79, 80]. It has enough resolution to measure a fan-out one logic gate delay.

2.3 RTN and its Impact on Circuits

Figure 2.2 shows the drain current noise in large and small MOSFET. Figure 2.2(a) shows the conceptual figure for a large MOSFET case. Drain currents of three transistors are continuously measured. The drain current fluctuates with time but their amplitude is small. The power spectral density becomes $1/f$ type[81]. It is called low-frequency noise or $1/f$ -noise. When MOSFET becomes smaller, the drain current fluctuates discretely with time as shown in Fig. 2.2(b)[10]. The fluctuation amplitude and the time constant differ so

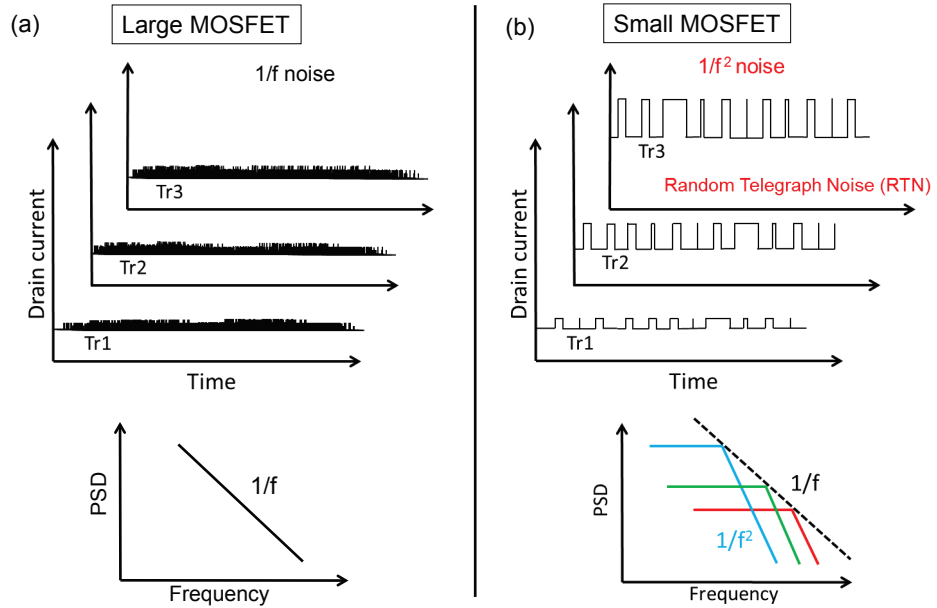


Figure 2.2: Drain current noise in (a) large and (b) small MOSFET.

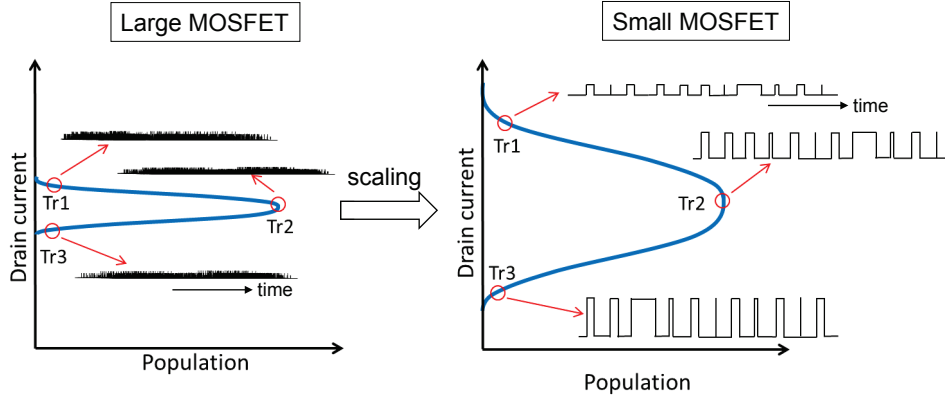


Figure 2.3: WID process variation and RTN fluctuation for a large and a small MOSFET.

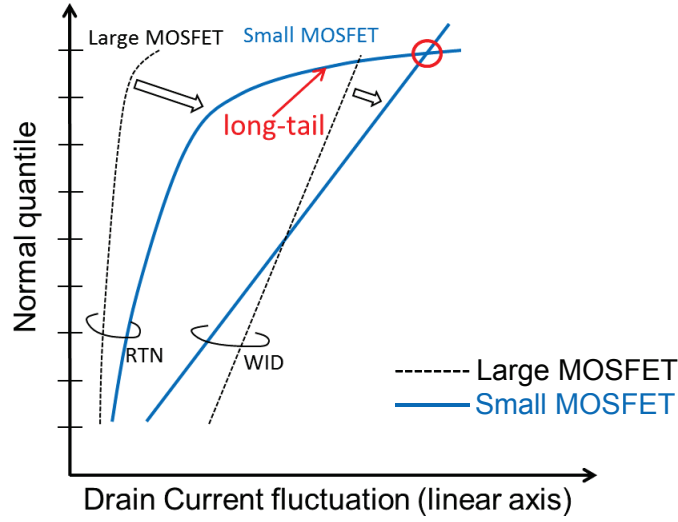


Figure 2.4: WID versus RTN as for statistical distribution.

much between different transistors. The power spectral density becomes $1/f^2$ type. RTN is characterized by a $1/f^2$ spectrum that is called Lorentzian power spectrum. It is considered that the superposition of many different $1/f^2$ noise generates $1/f$ noise[10].

Figure 2.3 shows WID process variation and RTN fluctuation. The left figure shows a large MOSFET case and the right figure shows a small MOSFET case. The blue line is drain current distribution due to WID process variation. Drain current fluctuations with time for three transistors are also shown. When

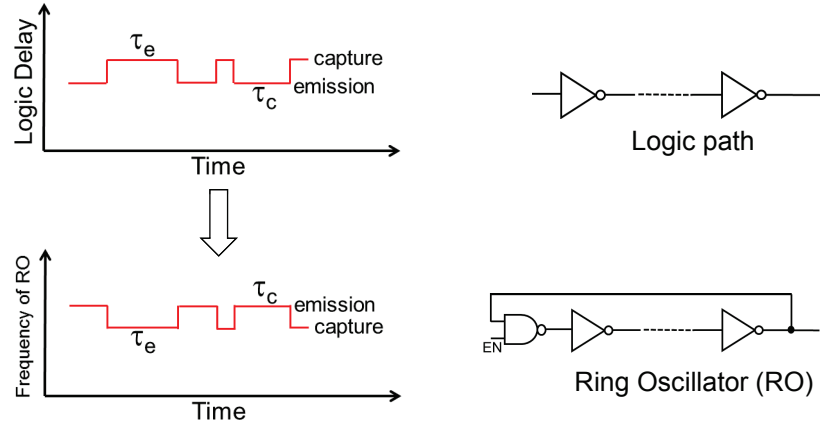


Figure 2.5: (upper) A logic path delay fluctuation by RTN. (lower) A ring oscillator (RO) oscillation frequency fluctuation by RTN.

technology scales as shown in the right figure of Fig. 2.3, WID variation becomes larger. RTN fluctuations differ by transistors in a small MOSFET. Thus statistical characterization is also necessary for RTN. Figure 2.4 shows WID versus RTN as for statistical distribution. The horizontal axis is the drain current fluctuation in linear scale. The vertical axis is the normal quantile. The dotted black line is a large MOSFET case and the blue line is a small MOSFET case. WID variation usually follows a normal distribution for both the large and the small MOSFETs. But the variation becomes larger for the small MOSFET case. RTN does not follow normal distribution. RTN distribution has a long-tail part. The long-tail part becomes much longer for the smaller MOSFET as shown in Fig. 2.4[82]. Due to the long-tail for smaller MOSFET, the drain current fluctuation by RTN can exceed WID variation at some σ value[83]. The impact of RTN and WID becomes comparable at the cross point shown as red circle in Fig. 2.4. In a scaled technologies, the impact of RTN fluctuation can be comparable to process variation in a dense circuit such as SRAM.

When a logic path delay is continuously monitored, the delay fluctuates with time if RTN occurs in some logic gates. Figure 2.5 shows that a logic path delay or a ring oscillator (RO) oscillation frequency fluctuates with time due to RTN. If the fluctuation is small, RTN has no impact on circuit operation. From measurement data shown in Chapter 6, RTN-induced delay fluctuation can be an issue. But it is shown that proper circuit design and proper operating condition can reduce the impact.

Low frequency noise or $1/f$ noise is observed in various systems[84]. As for LSI systems, $1/f$ noise can be observed as a drain current fluctuation in a transistor with moderately large gate area. On the other hand, RTN is observed in a small transistor with a few oxide traps. As already described, one possible interpretation is that the superposition of various RTN with a broad distribution

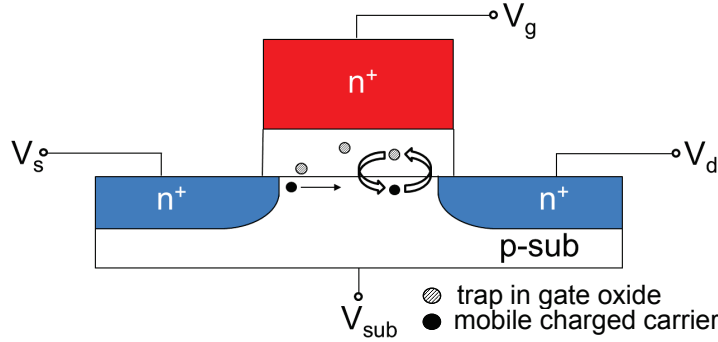


Figure 2.6: Capture and emission of carriers by gate oxide traps (nMOSFET).

of activation energies in RTN process yields $1/f$ noise[10]. Figure 2.6 shows a conceptual process of RTN in an nMOSFET where an electron traveling in the channel is trapped into or detrapped from oxide traps randomly. The capture and emission of one carrier induces two-state RTN. Figure 2.7 is a typical example of a measured drain current fluctuation in a commercial 40 nm pMOSFET in our test chip that has a large two-state RTN. Time constants τ_c and τ_e are defined as the time when the drain current stays at high-current state (H-state) and low-current state (L-state) respectively. The fluctuation amplitude is defined as ΔI_{ds} . RTN is an intrinsically random phenomenon. The parameter such as τ_c , τ_e and ΔI_{ds} differ by transistors. Thus statistical characterization is necessary for the correct RTN modeling[85, 86, 87]. When a two-state RTN is measured for some period, distributions of τ_c and τ_e are obtained. The average of τ_c and τ_e is denoted as $\langle \tau_c \rangle$ and $\langle \tau_e \rangle$ respectively. We assume that the probability of a transition from H-state to L-state per unit time is given by $1/\langle \tau_c \rangle$ and from L-state to H-state per unit time is given by $1/\langle \tau_e \rangle$. $A(t)$ is defined as the probability that a transition from H-state to L-state does not happen after time t . Then,

$$A(t + dt) = A(t) \left(1 - \frac{dt}{\langle \tau_c \rangle} \right) \quad (2.5)$$

is obtained. Integrating Eq. (2.5) with $A(0) = 1$,

$$A(t) = \exp(-t/\langle \tau_c \rangle). \quad (2.6)$$

As a result, the probability, $P_H(t)$, that the transition from H-state to L-state does not happen for time t , and then happens between time t and $t + dt$ is given by

$$P_H(t) = \frac{1}{\langle \tau_c \rangle} \exp(-t/\langle \tau_c \rangle). \quad (2.7)$$

The time constant, τ_c and τ_e , follows exponential distribution by Eq. (2.7). It is experimentally shown later that time constants actually follow exponential

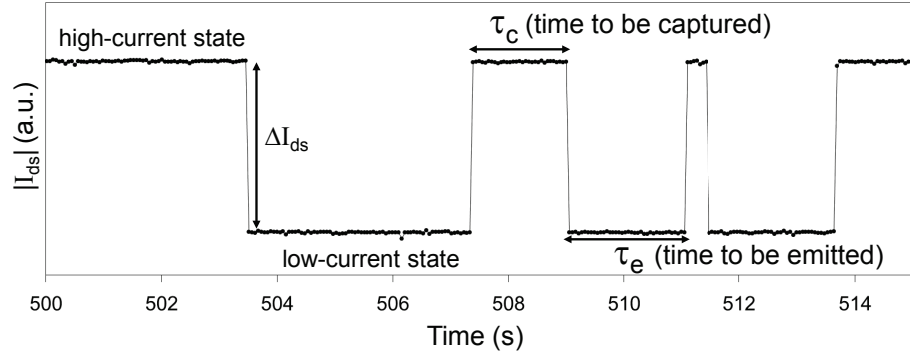


Figure 2.7: RTN-induced drain current fluctuation in a pMOSFET.

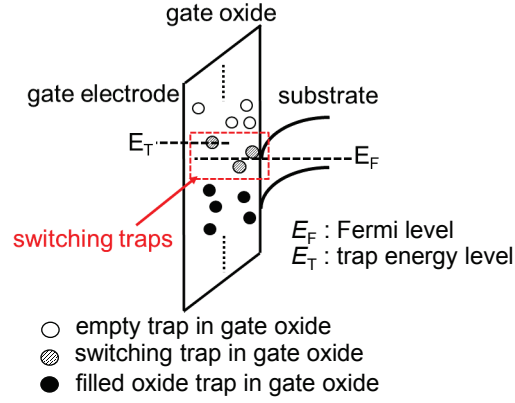


Figure 2.8: Energy band diagram of an nMOSFET transistor.

distribution both for a two-state drain current fluctuation (Section 5.1) and for a two-state logic delay fluctuation (Section 6.2).

The capture and emission of a carrier also induces the threshold voltage fluctuation, ΔV_{th} , and it is approximately expressed as

$$\Delta V_{th} = \frac{e}{LWC_{ox}}, \quad (2.8)$$

where L is the gate length, W is the gate width, C_{ox} is the gate capacitance per unit area, and e is the elementary charge. Equation (2.8) shows the impact of one charged carrier on ΔV_{th} becomes larger as the gate area shrinks. When the operating voltage of a circuit decreases, the impact of ΔV_{th} also becomes larger. Recent studies show that ΔV_{th} caused by RTN grows more rapidly than the threshold variation caused by random dopant fluctuation[20]. Figure 2.8 shows the energy band diagram of an nMOSFET transistor. The Fermi level is denoted by E_F and the trap energy level is denoted by E_T . Traps below E_F

(filled circle) is filled and above E_F (open circle) is empty. Several traps close to E_F can act as switching traps. The $\langle\tau_c\rangle/\langle\tau_e\rangle$ ratio follows

$$\frac{\langle\tau_c\rangle}{\langle\tau_e\rangle} = \exp\left(\frac{E_T - E_F}{k_B T}\right), \quad (2.9)$$

where k_B is Boltzmann constant and T is temperature. When one switching trap exists, a 2-state discrete drain current fluctuation is observed. If there are n switching traps, a 2^n -state discrete fluctuation can be observed.

RTN in transistors is a critical issue not only for analog/RF circuits but also for digital circuits. RTN already has a serious impact on CMOS image sensors[88], flash memories[89], and SRAMs[90, 91, 92].

Recently it is reported that RTN also induces performance fluctuation to logic circuits[93]. The impact of RTN can be a serious problem even for logic circuits when they are operated under low supply voltage[94, 95, 96]. Circuit designers can change various parameters such as operating voltage, transistor size, logic stage number, logic gate type, and substrate bias. However, the impact of such parameters on RTN is not well understood at the circuit level. This impact is clarified based on measurement results in Chapters 5 and 6. It is shown in Chapter 6 that the impact of RTN-induced logic delay fluctuation grows log-normally. It is also confirmed that the logic delay variation due to process variation follows normal distribution. It is experimentally shown that although process variation still dominates, the impact of RTN grows rapidly than process variation in combinational circuits. Circuit designers can obtain a useful information from Chapter 6 when they try to suppress various reliability problems.

Fully depleted SOI (FD-SOI) MOSFETs are one of the attractive devices for the present and the future planar CMOS technology[97]. As one of the FD-SOI devices, the Silicon On Thin Buried oxide (SOTB) is developed because of the superior device characteristics for ultra-low voltage operations and the suppression of device variability caused by dopant fluctuation[98]. Some paper predicted that RTN amplitude is also suppressed by FD-SOI MOSFETs when it is compared to bulk MOSFETs[99]. It is because large channel potential fluctuation in the bulk device is suppressed in the FD-SOI device[99]. Multi-gate transistors such as tri-gate device are also attractive devices and have already been applied to the advanced SoC in 22 nm technology[100]. RTN in multi-gate device and its impact on circuit becomes an important issue in recent CMOS technologies[101, 102]. Although 65 nm and 40 nm technologies are considered in this thesis, the property of the interface between the gate oxide and the substrate has some common features with multi-gate technologies. Thus various results with respect to gate oxide reliability in this thesis are expected to contribute to future multi-gate technologies. Chapter 5 and 6 describe the impact of RTN on CMOS logic circuit reliability based on our measurement results from 65 nm and 40 nm test chips.

2.4 Chapter Summary

This chapter briefly describes transistor performance fluctuation in CMOS technology with respect to variability and reliability. The local or WID variation has been a major concerns in recent CMOS technologies due to the aggressive miniaturization and the introduction of various new technologies. Various causes of WID variation are summarized. As an important example of WID variation, the transistor mismatch due to RDF has severe influence on various circuits such as SRAM and analog circuit. Previously it is considered that process variation dominates the impact of transistor reliability. But transistor reliability problems such as NBTI and RTN have become issues that already can not be ignored. Recent researches of NBTI and RTN owe to previous researches on HCI and TDDB so much. A brief overview on HCI and TDDB is described. Although HCI degradation still remains an issue in transistor reliability, it is described that its impact has become smaller than that of NBTI in a recent lower voltage CMOS technology. Final two sections overviews NBTI, RTN and their impacts on circuits. As for the impact of RTN on combinational circuits, some main results that will be obtained in Chapter 6 are briefly described. The impact of RTN can be a serious problem even for logic circuits when they are operated under low supply voltage. Although process variation still dominates, the impact of RTN grows rapidly than process variation in combinational circuits. Various results with respect to gate oxide reliability in this thesis are expected to contribute to future CMOS technologies such as multi-gate transistor.

Chapter 3

NBTI Degradation and Recovery Characterization

This chapter describes NBTI degradation and recovery characterization at a transistor-level. All results are based on fast NBTI characterization methods. Section 3.1 describes issues in NBTI characterization. In Section 3.2, NBTI characterization by measure-stress-measure (MSM) method is described. Section 3.3 deals with NBTI characterization by Leakage Current (LC) method. An NBTI recovery sensor with a 400 ns measurement delay based on LC method is proposed[103, 104]. For the first time, the leakage current recovery in the region of $400 \text{ ns} \leq t_{\text{recovery}} \leq 30 \text{ ms}$ is clarified.

3.1 Issues in NBTI Characterization

The recent slower scaling of operating voltage and widely-used nitridation processes of gate insulator after 65 nm CMOS technologies are two main reasons that promote NBTI. Several NBTI characterization methods have already been proposed[105, 106, 107, 108, 109, 110, 103]. The complex recovery may contain very fast process less than $1 \mu\text{s}$ [109]. It is the reason why there are no direct measurement methods to characterize full recovery process. Thus there is no perfect NBTI model. How to combine several characterization methods for the purpose of clarifying NBTI is still an ongoing research topic. Developing a new characterization method is also an ongoing research topic[111].

One of the popular characterization methods is a measure-stress-measure (MSM) method[105]. It involves application of a stress voltage to the gate to accelerate degradation. The stress is periodically interrupted and the device characterization by $I_{\text{ds}}-V_{\text{gs}}$ sweep or one-spot I_{ds} measurement is done. In Section 3.2, all characterizations with the MSM method are done by measuring one I_{ds} at the same bias condition. The key factor when the MSM is applied is that its measurement delay should be kept as short as possible. In this thesis, the measurement delay is kept as short as $1 \mu\text{s}$. $1 \mu\text{s}$ is a comparably short

measurement delay when it is compared with other papers[18, 106]. One paper reports that the recovery seems to start before $1\mu s$ after the stress is relaxed[18]. Another paper reports that the recovery starts around $1\mu s$ after the stress is relaxed[106].

When a dynamic or an AC stress is applied to the gate, it is known that the degradation becomes smaller than that of a constant gate stress case[14, 16]. Here the gate stress voltage takes the value of 0 V or the gate stress voltage, $V_{gs_AC}(< 0)$, for the dynamic stress. The gate stress voltage takes constant value, $V_{gs_DC}(< 0)$, for the constant stress. The source, the drain, and the substrate terminal voltages are set to 0 V. Even though

$$V_{gs_AC} = V_{gs_DC}, \quad (3.1)$$

the degradation for the AC stress case becomes smaller than that of the DC stress case. It is because NBTI recovery occurs for the AC stress case when the gate bias takes the value of 0 V. When a pulse signal propagates in a digital circuit, its logic gate suffers from AC NBTI. Estimating the lifetime of the logic gate by DC NBTI becomes pessimistic. How its lifetime is prolonged by considering the AC NBTI effect is very important. The switching frequency dependence in AC NBTI is also important for the digital circuit lifetime prediction. One paper reports that no frequency dependency is observed between 1 Hz and 2 GHz[112]. Another paper reports that some frequency dependency is observed between 1 Hz and 1 kHz[113, 114].

Sections 3.2 and 3.3 focuses on an averaged behavior of NBTI degradation and NBTI recovery at a transistor level. In a small transistor, NBTI-induced V_{th} shifts with respect to a stress time and a recovery time differ by transistors[115, 116, 117, 118, 119]. BTI variation is especially important in a circuit that uses a large number of small transistors. Considering NBTI variability into SRAM circuit design has already been proposed[115]. One paper on 6-transistor SRAM reports improved write access time, degraded read static noise margin and increased hold failure with increased NBTI stress[120]. Another paper reports that a read failure probability in a 100-k SRAM array in a 28 nm technology is not so influenced by BTI-induced variability even after 10 years operation[121].

When NBTI recovery is used for an LSI lifetime extension, it is necessary to know how much degradation can be recovered[122, 123]. Various important results of recovery behavior as well as degradation behavior are obtained by the MSM method. At the same time, the limitation of the MSM method is experimentally confirmed in the next section. To compensate the MSM method, the leakage current (LC) method that has the highest fidelity to NBTI recovery measurement is developed in Section 3.3[103, 104].

3.2 NBTI Characterization by Measure-Stress-Measure (MSM) Method

In this section, NBTI characterization at transistor level is described. As already described in the previous section, one popular characterization method is a MSM method[105]. The drain current degradation by NBTI is characterized in this section. Figure 3.1 shows the gate bias condition of the MSM NBTI characterization method used in this section for a pMOSFET characterization. $V_{g\text{stress}}$ and $V_{g\text{meas}}$ represents the gate bias under the stress phase and the measurement phase, respectively. The gate bias under the recovery phase is set to 0 V. The initial measurement is done before the stress phase. The recovery phase follows the stress phase. Short time measurement interrupts the stress phase or the recovery phase. The source, the drain and the substrate bias are usually kept to 0 V. The drain bias is set to some finite negative value only in the measurement duration. All measurements are done in the same bias condition in the MSM method. It is generally believed that the measurement delay is set to as short as $1\ \mu\text{s}$ to prevent NBTI recovery for a correct NBTI characterization[106]. Figure 3.2 shows the test structure schematic of 3×5 pMOSFET array and its layout with 10 pads. Five transistors out of the 15 transistors are selected at one time for NBTI measurement to average the NBTI degradation variation for each transistor. This transistor is fabricated in a commercial 65 nm CMOS technology. We use the standard size pMOSFET in the technology. The physical gate oxide thickness is 1.7 nm and the minimum L is 50 nm (physical).

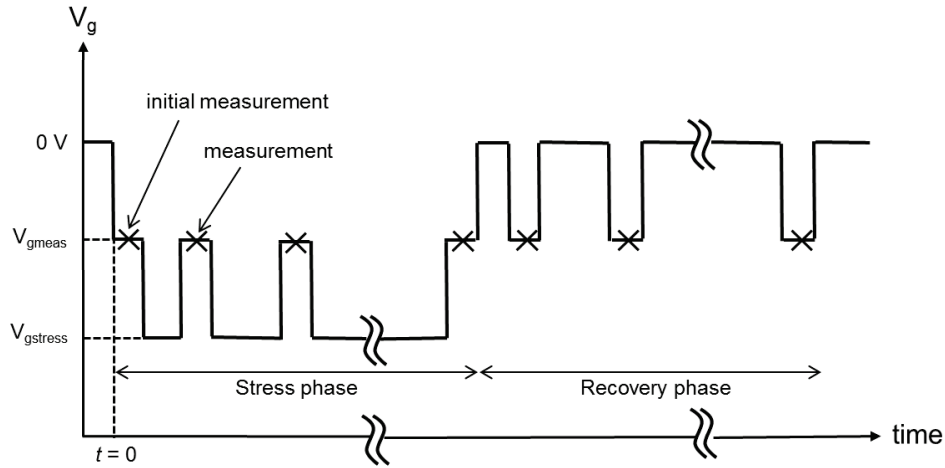


Figure 3.1: Gate bias condition of Measure-Stress-Measure NBTI characterization method.

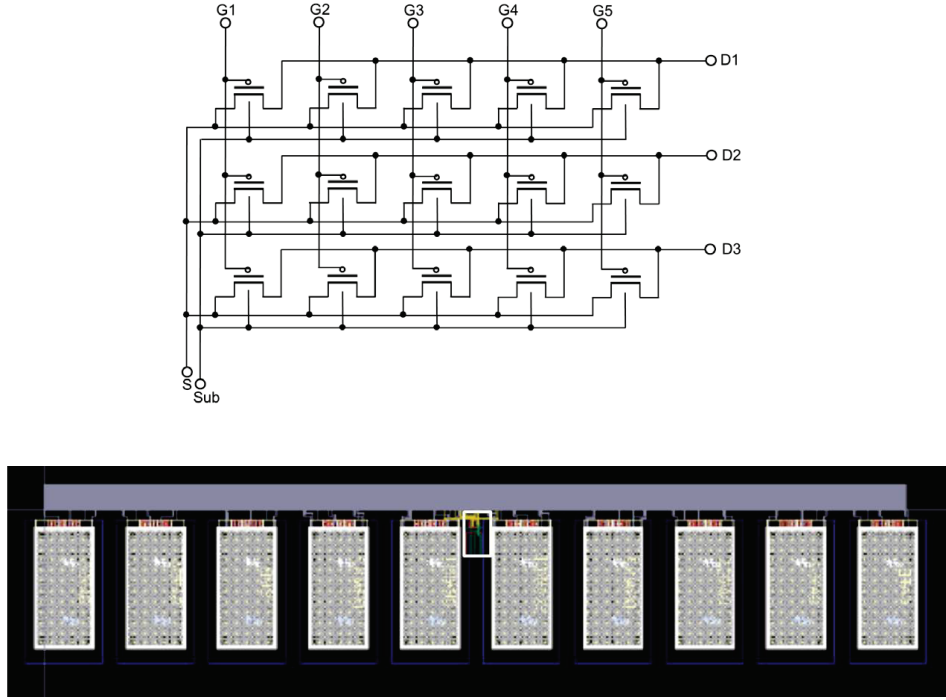


Figure 3.2: Test structure schematic of 3×5 pMOSFET array and its layout with 10 pads.

In the following, the impact of a measurement delay on NBTI characterization is described. Figure 3.3 shows an example of the drain current degradation measurement result. The vertical axis is the drain current degradation ratio normalized by the initial drain current ($\Delta I_d / I_{d_init}$). The horizontal axis is the stress time. Both axes are plotted in log-scale. The measurement delay is changed as 500 ns, 1 ms and 100 ms. When the measurement delay is changed as 500 ns, 1 ms and 100 ms, $\Delta I_d / I_{d_init}$ follows t^n where $n = 0.11, 0.16$ and 0.20 , respectively. Due to the NBTI recovery, $\Delta I_d / I_{d_init}$ becomes smaller than true degradation. As a result, the slope n becomes larger than the true value. How to predict the true n is one of the difficult problems because it depends on the recovery behavior within $1 \mu\text{s}$ time scale that is hard to access experimentally. Even for the data of 500 ns measurement delay, degradation begins to be away from the $t^{0.11}$ line for stress time shorter than 10^{-2} s. It may be due to recovery during measurement. Figure 3.4 shows the drain current degradation with various measurement delays at 15 s stress time in Fig. 3.3. The degradation becomes smaller due to NBTI recovery during characterization and it follows $\log t_{\text{meas.delay}}$. From Figs. 3.3 and 3.4, it is confirmed that the key factor when

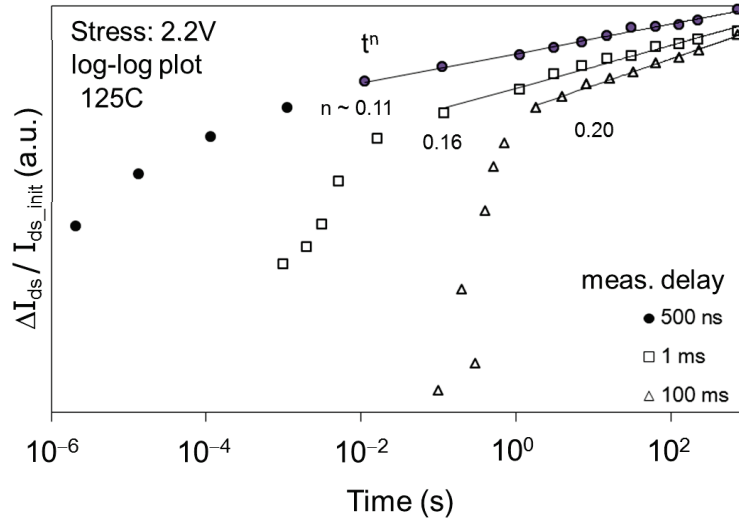


Figure 3.3: The drain current degradation measurement with various measurement delays.

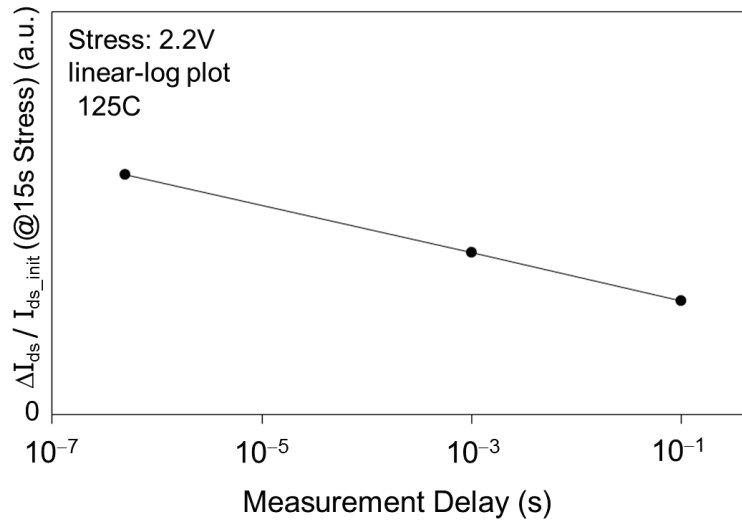


Figure 3.4: The drain current degradation with various measurement delays at 15 s stress time in Fig. 3.3.

the MSM is applied is that its measurement delay should be kept as short as possible. In this section, the measurement duration is set to 500 ns $\sim$ 1 μ s.

It is generally considered that V_{th} -shift by NBTI consists of a recoverable and an unrecoverable component. NBTI recovery is used for an LSI lifetime extension in Chapter 4. In the following, it is clarified how much degradation can be recovered. Figure 3.5 shows an example of the generated voltage waveform of stress phase captured by an oscilloscope. V_g , V_d , V_s , and V_{sub} mean gate bias, drain bias, source bias, and substrate bias, respectively. The gate bias under the stress phase is -2.2 V and under the recovery phase is 0 V. The drain bias is set to -0.6 V only in the measurement duration. The measurement delay is set to 300 ns and the measurement duration is set to 500 ns $\sim$ 1 μ s. Followed by the initial measurement, first 10 μ s stress is applied in Fig. 3.5. Then the measurement with 500 ns duration appears followed by second stress. All measurements are done by a commercial semiconductor parameter analyser[124, 125].

Figure 3.6 shows the two cycle degradation and recovery measurement result plotted in a linear scale. It is obtained by using the MSM method. Five standard size transistors out of the 15 transistors are selected at one time as already shown in Fig. 3.2. The vertical axis is $\Delta I_d/I_{d_init}$ and the horizontal axis is the measurement time. The stress time for one cycle is 727 s and the recovery time

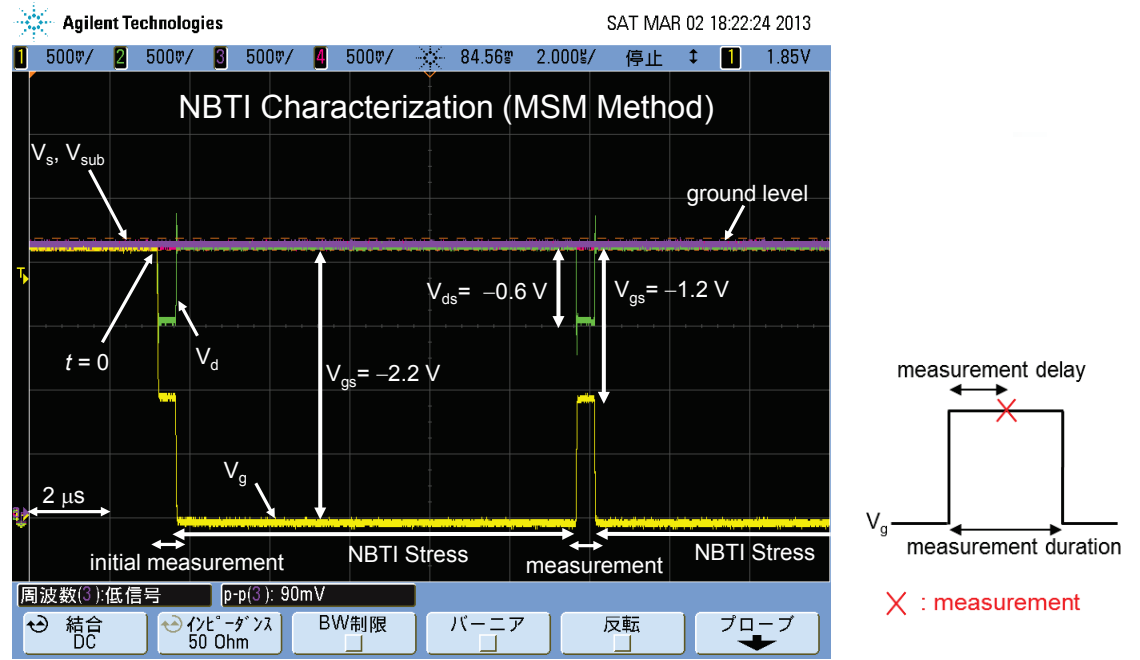


Figure 3.5: Generated voltage waveform of the stress phase.

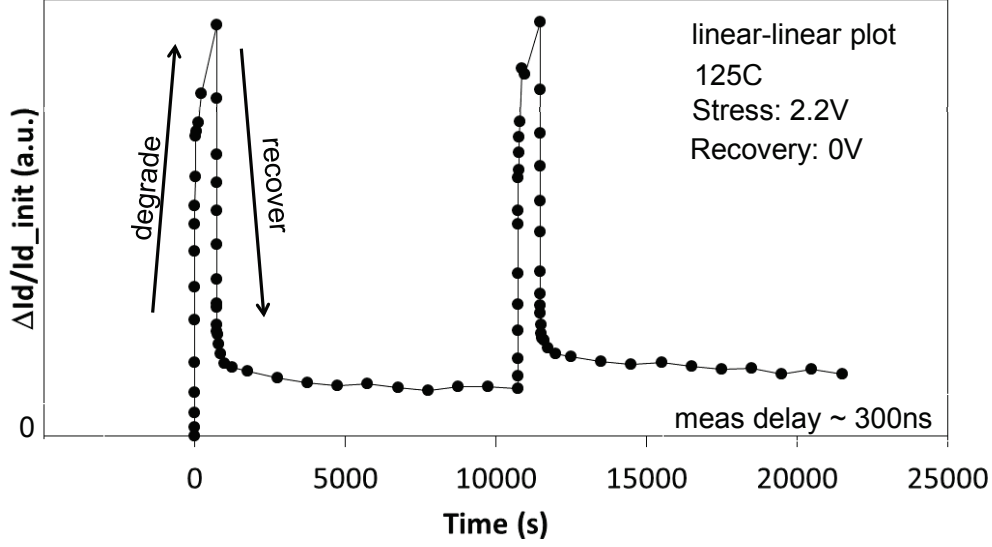


Figure 3.6: Two cycle degradation and recovery measurement result.

for the same cycle is 10,023 s. One cycle measurement is completed in 10,800 s. The gate stress voltage is -2.2 V and the gate recovery voltage is 0 V. The stress temperature is 125°C . The measurement starts at $t = 0$. The device degrades rapidly in the early phase of the degradation and degrades slower in the final phase of the degradation. Recovery starts rapidly and becomes slower in the final phase of the recovery. The recovery seems to saturate after several thousand seconds of the recovery time but the saturation level slightly increases in the recovery phase of the second cycle. It is considered that the recovery saturation represents the permanent degradation component or very slowly recoverable component of NBTI. It is considered that the increase of the saturation level in the second cycle is due to the permanent component accumulation. NBTI degradation is accelerated by the stress voltage and V_{gs} is set to -1.8 V, -2.0 V or -2.2 V. The stress voltage dependence of NBTI degradation at the first cycle is shown in Fig. 3.7. The degradation becomes larger as V_{gs} increases. The degradation follows t^n after 10 ms stress but the degradation departs from the t^n behavior in the early degradation phase before 10 ms stress time as shown in Fig. 3.7(left). In the early degradation phase, $\log t$ behavior well describes the degradation as shown in Fig. 3.7(right). When the degradation follows t^n , the index n does not strongly depend on the stress voltage and the value is around 0.12. Figure 3.8 shows the stress voltage dependence of NBTI recovery at the 1st cycle. Just after the last point of degradation measurement at the 1st cycle, V_{gs} is set to be 0 V for the recovery as already described in Fig. 3.1. The initial time ($t = 0$) of the recovery is the last degradation measurement point in

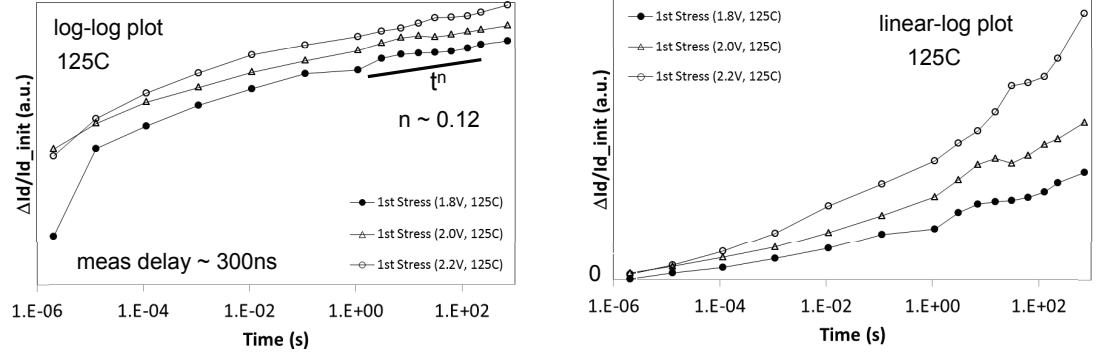


Figure 3.7: Stress voltage dependence of NBTI degradation at 1st cycle. (left) log-log plot. (right) linear-log plot.

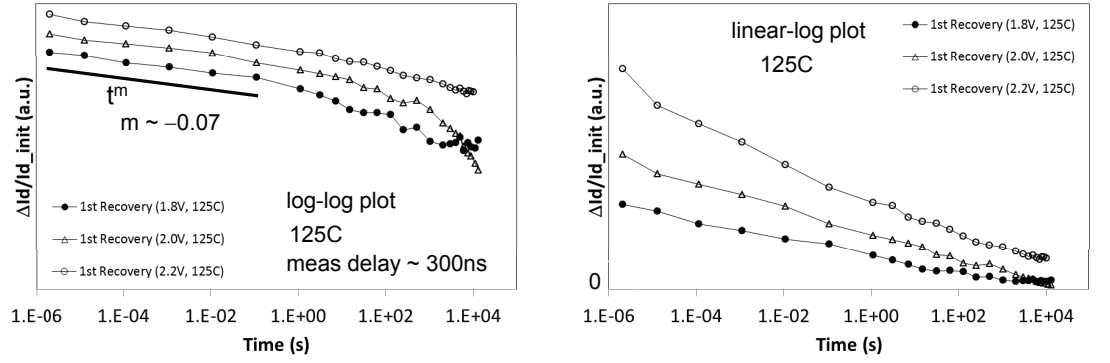


Figure 3.8: Stress voltage dependence of NBTI recovery at 1st cycle. (left) log-log plot. (right) linear-log plot.

the 1st cycle. The NBTI recovery begins to be measured only $2 \mu\text{s}$ after the last degradation point. As shown in Fig. 3.8, the recovery does not have a tendency to saturate at $2 \mu\text{s}$. It is clarified that the recovery has already begun within $2 \mu\text{s}$ after the last degradation in this sample. Although MSM method suffers from NBTI recovery during NBTI characterization, these results are obtained with a comparably short measurement delay when it is compared with other papers. The recovery is well described by both t^m and $\log t$ behavior after $t = 2 \mu\text{s}$. The index m for t^m does not strongly depend on the stress voltage and the value is around -0.07 as shown in Fig. 3.8(left). From Fig. 3.6 to Fig. 3.8, it is clarified in this device that 10–20% of NBTI degradation becomes unrecoverable and

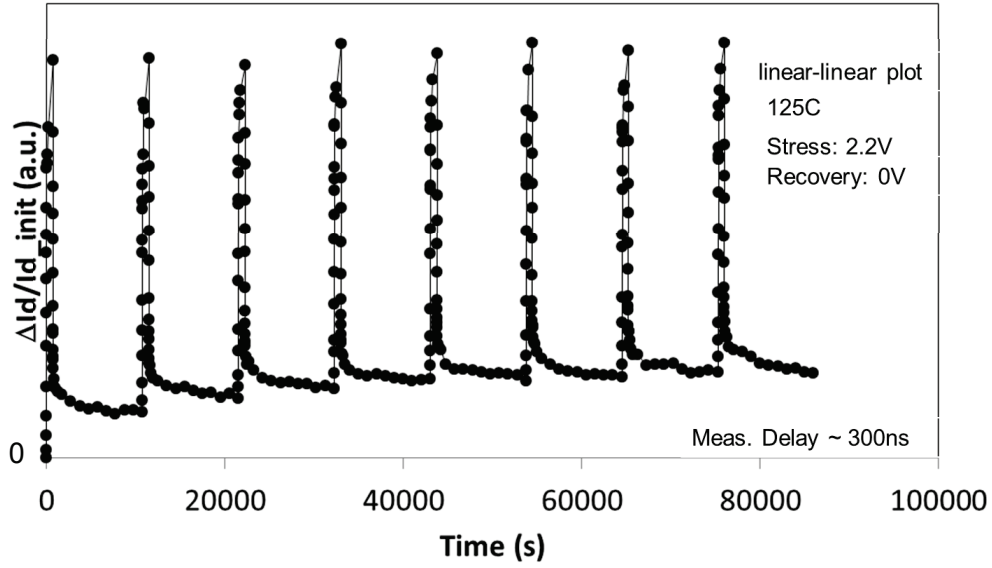


Figure 3.9: Eight cycle degradation and recovery measurement result.

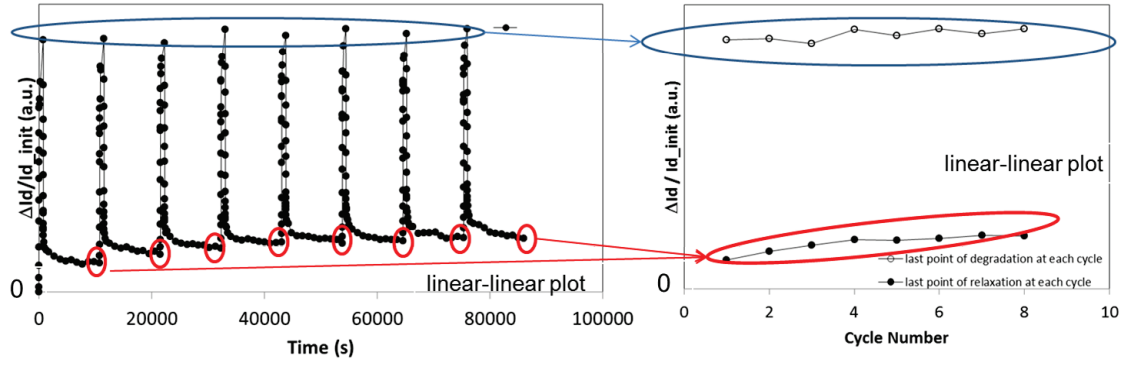


Figure 3.10: The last point of degradation at each cycle and the last point of relaxation at each cycle of Fig. 3.9 are plotted.

80–90% of that becomes recoverable.

In the following, how the unrecoverable component of NBTI is accumulated is shown. For this purpose, the degradation and recovery cycle is further repeated. Figure 3.9 shows the eight cycle degradation and recovery measurement result plotted in a linear scale. The stress time for one cycle is 727 s and the recovery time for the same cycle is 10,023 s. Although most of the final degradation

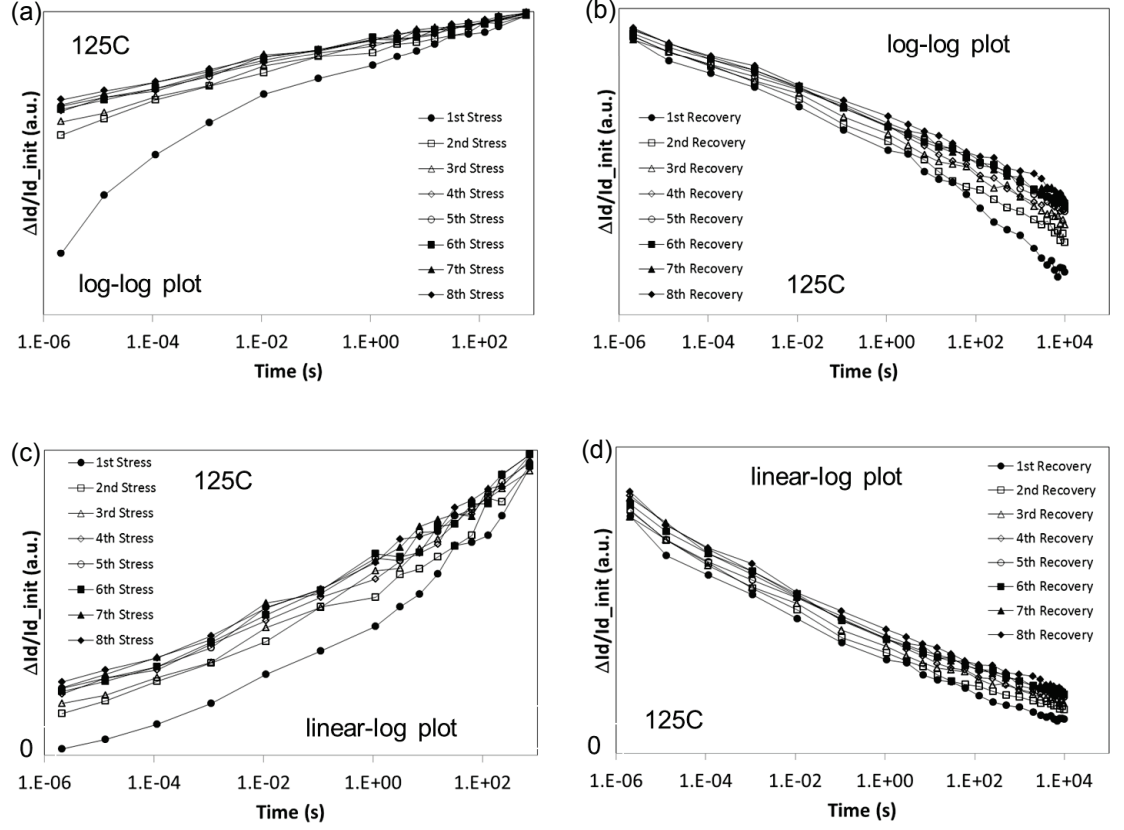


Figure 3.11: Degradation and recovery measurement results for each cycle.

(a) Degradation in log-log scale. (b) Recovery in log-log scale. (c) Degradation in linear-log scale. (d) Recovery in linear-log scale.

amount at each degradation cycle recovers in each recovery phase, the saturation level of each recovery phase slightly increases towards the last eighth cycle. It is considered that the monotonic increase of the saturation level is due to the permanent component accumulation. Next, the last point of degradation at each cycle and the last point of relaxation at each cycle are plotted in Fig. 3.10 (right). Almost the same degradation is observed for every cycle but the last point of relaxation at each cycle slightly increases. Figure 3.11 shows the degradation and the recovery results for each cycle and the data is taken from Fig. 3.9. The upper half two figures (Fig. 3.11(a), (b)) are plotted in a log-log scale and the lower half two figures (Fig. 3.11(c), (d)) are plotted in a linear-log scale. The upper left and the lower left figures (Fig. 3.11(a), (c)) show the

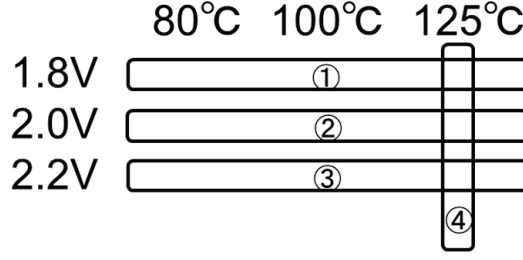


Figure 3.12: Combination of stress voltage and temperature for NBTI recovery modeling.

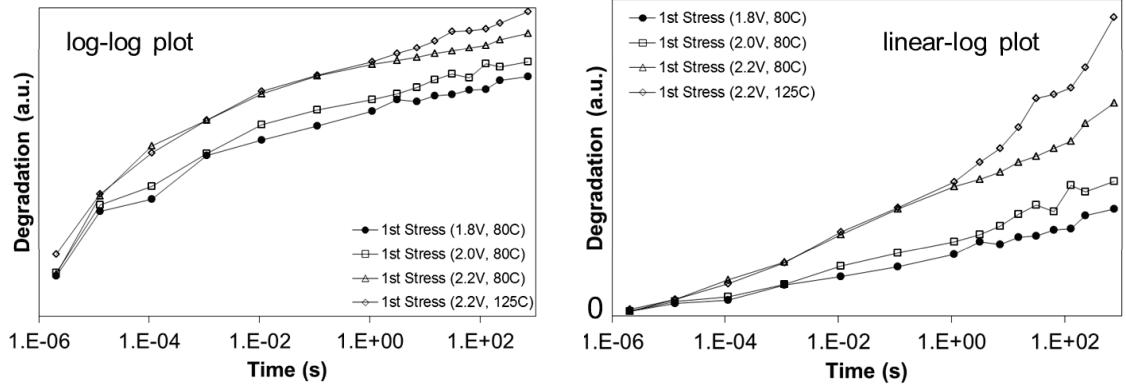


Figure 3.13: Pre-stressed samples for various degradation conditions.

degradation data for each cycle. The upper right and the lower right figures (Fig. 3.11(b), (d)) show the recovery data for each cycle. Due to the slowly recoverable or permanent component, the first point of the degradation after 2nd cycle slightly increase and the degradation follows t^n behavior all the time after the 2nd cycle as shown in Fig. 3.11(a). The last points of the degradation for each cycle are almost same after 727s stress. Just after the last point of the degradation at each cycle, NBTI recovery starts. Because vertical axes for the degradation and the recovery are plotted in a same scale, the recovery has already started $2 \mu\text{s}$ after the beginning of the recovery. It is found that about 20% recovery is observed at $t = 2 \mu\text{s}$ for the each recovery cycle. It indicates that the measurement delay should be shorter than $1 \mu\text{s}$ in this device. The recovery around $2 \mu\text{s}$ in Fig. 3.11(b) or (d) is contrast to Ref. [106] that shows a recovery saturation around $t = 1 \mu\text{s}$. It seems to be different from Ref. [18] because the recovery around $t = 2 \mu\text{s}$ in Fig. 3.11 (d) is downward-convex

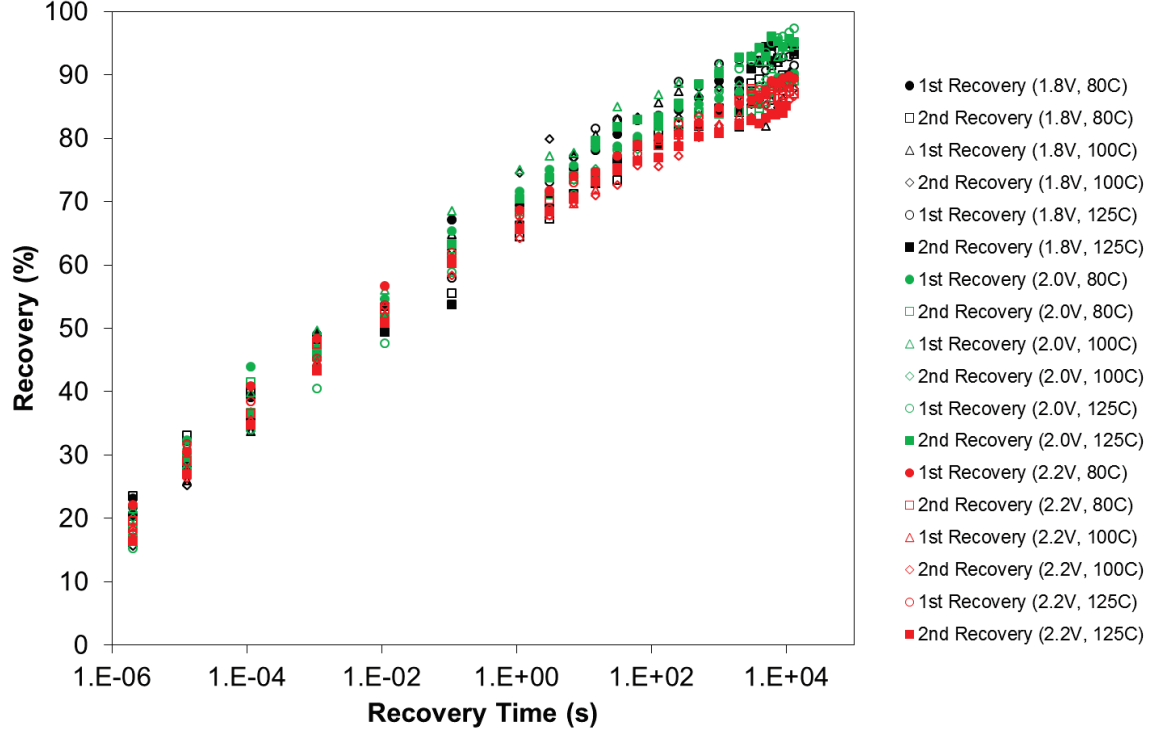


Figure 3.14: NBTI recovery from various degradation levels.

function. Ref. [18] seems to show upward-convex function around $t = 2 \mu\text{s}$ recovery time. The recovery is well described by both t^m and $\log t$ behavior as shown in Fig. 3.11(b), (d). From Fig. 3.9 to Fig. 3.11, it is clarified that the permanent component accumulation becomes monotonic as the stress time increased. The increasing speed of the permanent component is slow and it is at most 20% after eight cycle measurement. LSI performance can also be recovered by NBTI recovery. Its lifetime can be further extended by repeatedly recovering degraded circuits. This concept is further described in Chapter 4.

Some papers describe that NBTI recovery has a universal behavior independent of stress voltage, stress time and temperatures[126]. It may help to remove the recovery effect by a calibration during NBTI characterization[127]. Thus, it is very useful if such a universal behavior can be found in the device used in this thesis. In the following, a universal NBTI recovery behavior is explored through the measurement. Figure 3.12 shows the combination of stress voltage and temperature for NBTI recovery modeling. The gate stress voltage is set to -1.8 V , -2.0 V , or -2.2 V . The stress temperature is set to 80°C , 100°C , or 125°C . Nine sets of experiments are done and these experiments are categorized

into four groups (Case I ~ Case IV). Case I is $(-1.8 \text{ V}, 80^\circ\text{C})$, $(-1.8 \text{ V}, 100^\circ\text{C})$, and $(-1.8 \text{ V}, 125^\circ\text{C})$. Case II is $(-2.0 \text{ V}, 80^\circ\text{C})$, $(-2.0 \text{ V}, 100^\circ\text{C})$, and $(-2.0 \text{ V}, 125^\circ\text{C})$. Case III is $(-2.2 \text{ V}, 80^\circ\text{C})$, $(-2.2 \text{ V}, 100^\circ\text{C})$, and $(-2.2 \text{ V}, 125^\circ\text{C})$. Case IV is $(-1.8 \text{ V}, 125^\circ\text{C})$, $(-2.0 \text{ V}, 125^\circ\text{C})$, and $(-2.2 \text{ V}, 125^\circ\text{C})$. Before starting NBTI recovery, nine samples that have different degradation levels are prepared under 727 s stress condition as described above (Fig. 3.13). Figure. 3.13 shows only four samples of $(-1.8 \text{ V}, 80^\circ\text{C})$, $(-2.0 \text{ V}, 80^\circ\text{C})$, $(-2.2 \text{ V}, 80^\circ\text{C})$, and $(-2.2 \text{ V}, 125^\circ\text{C})$. In the strongest stress experiment of $(-2.2 \text{ V}, 125^\circ\text{C})$, the degradation after 727s stress corresponds to several years order degradation under nominal operating condition.

Figure. 3.14 shows NBTI recovery data from various degradation levels. The vertical axis is defined as the recovery rate normalized at the last degradation level (of 727 s stress time) in each cycle. Although each recovery starts from various degradation levels, all data recover in a similar way. By using the fast MSM method, NBTI recoveries under various recovery conditions are found to follow one simple curve when they are averaged over five transistors. From Fig. 3.14, it is clarified that NBTI recoveries studied in this thesis also show a universal behavior. The weak dependence of the recovery on degradation level suggests that constructing a recovery model becomes much simpler. How to include observed recovery results into a circuit simulation model is a future work.

3.3 High-Fidelity NBTI Recovery Characterization by Leakage Current (LC) Method

The measurement results of MSM characterization method is discussed in the previous section. This section describes a sensor circuit design that has high fidelity to NBTI recovery monitoring. This circuit monitors a pMOSFET leakage current variation by NBTI. The leakage current decreases gradually under NBTI degradation.

First, on-the-fly (OTF) method is briefly discussed as a high-fidelity NBTI degradation characterization method. Then leakage current (LC) method is proposed as high-fidelity NBTI recovery characterization method. OTF method is one of the popular methods in NBTI characterization originally proposed in 2004[107]. Figure 3.15 shows the gate bias condition of OTF NBTI characterization method for pMOS transistor. By keeping the gate bias to the stress bias during the measurement, OTF can avoid NBTI recovery during the measurement. The source, the drain and the substrate bias are usually kept to 0 V but the drain bias is set to some small negative value only in the measurement duration. Typically, V_{ds} is set to be between several tens mV and 100 mV during the measurement. The disturbance by the measurement is kept to be as small as possible. As a recovery-free method, OTF has a great advantage but there are two main problems in this method. One problem is the degradation of the

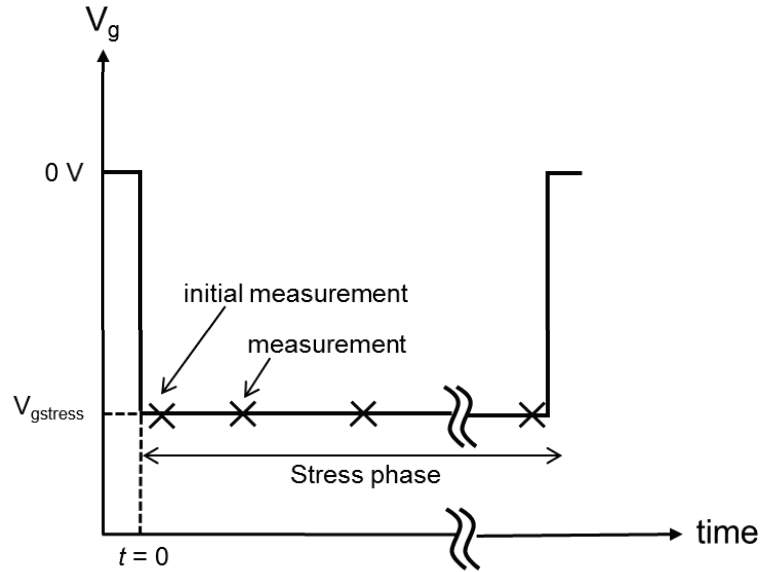


Figure 3.15: Gate bias condition of on-the-fly (OTF) NBTI characterization method.

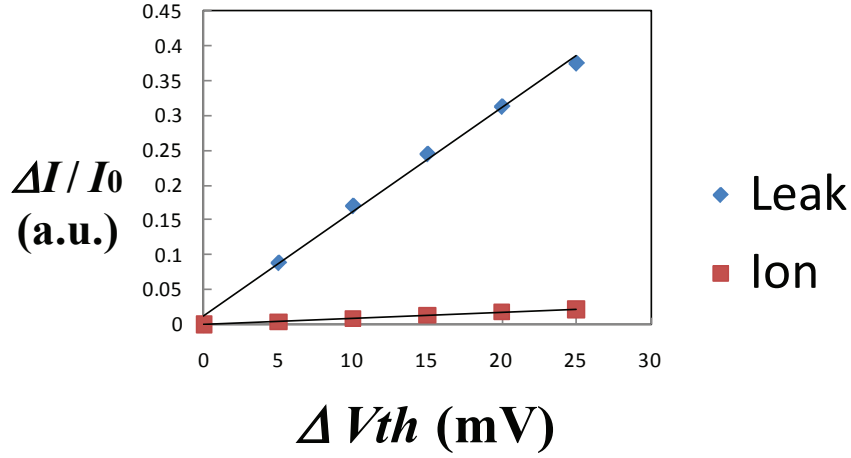


Figure 3.16: Drain to source off-leak current (Leak) has a much higher (16 times higher) sensitivity than the saturation current (Ion) under the same amount of deviation in the threshold voltage ΔV_{th} according to a circuit-level simulation. (© 2011 Japan Soc. App. Phys.)

drain current is characterized at the stress bias condition. Some calibration is necessary to get the threshold shift under nominal operating voltage. It is possible that the calibration procedure includes some errors. The other problem is the initial measurement is also done under a stressed bias condition. To avoid the fast NBTI degradation at the initial measurement, it is necessary to use a fast-OTF method[109].

In the following, leakage current (LC) NBTI characterization method is discussed. The characterization under the stress phase and the recovery phase is performed at off-leak ($V_{gs} = 0$) condition. The advantage of LC method is that a device under measurement in a recovery phase does not degrade at all because the gate bias is set to 0 V. MSM or OTF method usually uses some finite gate bias over the threshold voltage and it is difficult to avoid some degradation during the measurement. The disadvantage of LC method is that a device under measurement in a stress phase recovers much more than MSM or OTF method. Thus it is necessary to complete the measurement as short as possible to suppress the recovery as much as possible for LC method. This section starts to clarify the limitation of NBTI recovery measurement by a single pMOS transistor when LC method is applied. Then, it is described that an NBTI-recovery sensor with a minimum assist circuit achieving a 400 ns measurement delay[103, 104].

Figure 3.16 shows that the drain-to-source off-leak current (Leak) has 16 times higher sensitivity than the saturation current (Ion) under the same amount of deviation in the threshold voltage ΔV_{th} according to a circuit-level simulation.

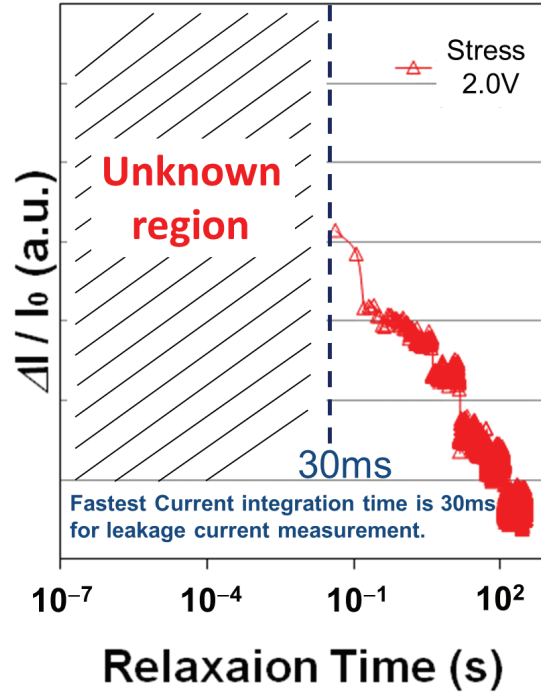


Figure 3.17: NBTI recovery measurement result by off-leak current of a single pMOS transistor for gate stress bias of 2.0 V. The fastest measurement delay is 30 ms. (© 2011 Japan Soc. App. Phys.)

Therefore, the off-leak current is used to characterize NBTI recovery with high resolution. Figure 3.17 shows the typical NBTI recovery measurement result obtained by the off-leak current of a single pMOS transistor. The transistor size used in Figs. 3.16 and 3.17 is identical and a small device is used. The bias during the stress phase is $V_{gs} = -2.0$ V, $V_{ds} = 0$ V, and $V_{sub} = V_s$. The bias during the measurement phase is $V_{gs} = 0$ V, $V_{ds} = -1.2$ V, and $V_{sub} = V_s$. This measurement is done using a commercial semiconductor parameter analyzer[124] and 30 ms is the fastest initial measurement time in the case of off-leak current measurement. The current integration time is about 30 ms and this limits the measurement delay of 30 ms. A triaxial cable of 3 m length is used to connect the analyzer and the probe card.

Clear step-like recovery behavior is observed. Such step-like behavior is due to the individual recovery of positively charged defects[128]. Recovery starts immediately (generally, at least $1 \mu s$) after stress is removed or relaxed[106]. Thus, the minimum measurement delay of 30 ms is too slow to measure NBTI recovery just after stress is released. As a result, there is an unknown region,

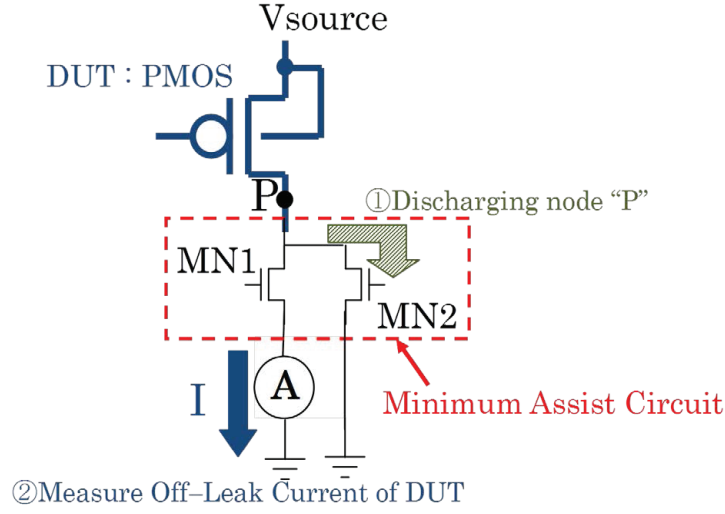
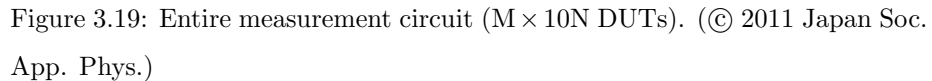


Figure 3.18: Concept of unit cell circuit design is shown. Unit cell circuit is constructed from a pMOS DUT and two assist nMOSFETs. Unit cell contains 10 DUTs in parallel in the real circuit. (© 2011 Japan Soc. App. Phys.)

as shown in Fig. 3.17, and clarifying the recovery behavior in this region is very important for NBTI recovery modeling. Next, this thesis proposes for the first time an NBTI-recovery measurement circuit that can measure the recovery behavior with as short as a 400 ns delay.

Parallelizing many pMOS transistors can amplify the off-leak current while achieving high resolution. However, a large amount of charge is stored at the drain node of a DUT pMOSFET during the NBTI stress phase. As a result, the measurement range of the analyzer changes owing to this large injection current, which makes the measurement speed slower. To avoid this problem, a circuit is proposed that has two assist nMOS devices (MN1 and MN2 in Fig. 3.18), added to the pMOS DUT. Figure 3.18 shows the concept of the proposed circuit. This unit cell contains 10 DUTs in parallel and the transistor size of one DUT pMOSFET is identical to the case in Figs. 3.16 and 3.17. Immediately after the NBTI stress is removed, the charge at node P (drain of DUT) is discharged by MN2 for about 30 ns. Then, the off-leak current of the DUT is measured by opening MN1. These two nMOS devices achieves a 400 ns measurement delay as shown in the next section. Figure 3.19 shows the top structure of the proposed circuit. $M \times N$ cells in Fig. 3.18 are connected and the sum of the off-leak current of all these cells is measured. Because there are buffers between unit cells, the time when the leakage current begins to be measured in each cell is delayed slightly. As a result, the peak current that rushes to the ammeter immediately after MN1 is turned on becomes smaller and the measurement



VST2 determines the pMOSFET leakage measurement duration. As shown in Fig. 3.20, the measurement delay of the circuit depends on the time until the circuit stays in a stable state after VST1 becomes “high”. Figure 3.21 shows the simulation result of the current at node Q in Fig. 3.20. The line labeled as $\Delta V_{th} = 0$ mV corresponds to a fresh sample case and the line labeled as $\Delta V_{th} = 20$ mV represents a degraded case. Owing to the NBTI degradation, the off-leak current decreases, as shown in Fig. 3.21. Soon after the NBTI stress is removed, there appears a peak current, as shown in Fig. 3.21. Then, this current becomes stable and the measurement delay can be determined (about 20 ns). Figure 3.22 shows the measurement result of the current at node Q. The current

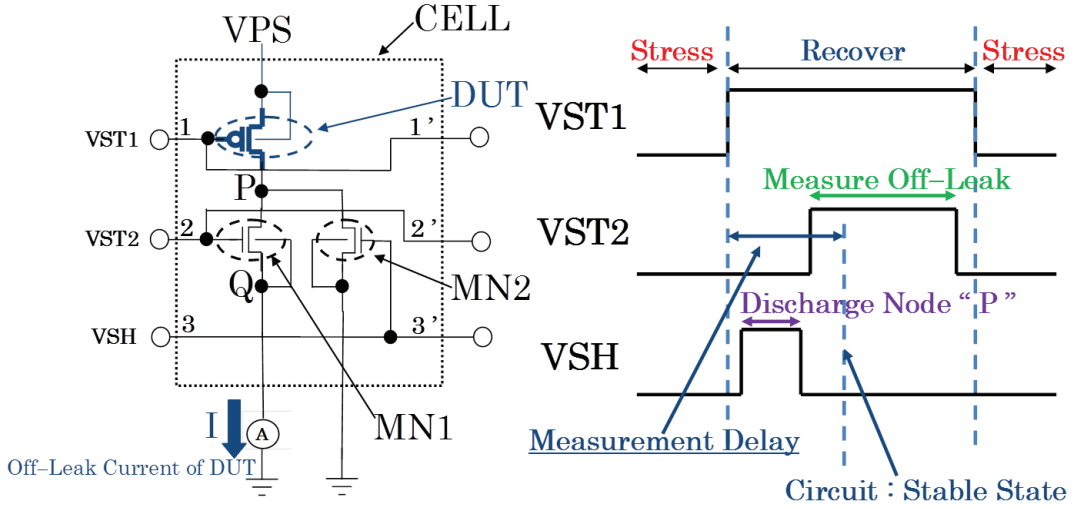


Figure 3.20: Timing chart of the proposed measurement circuit. (© 2011 Japan Soc. App. Phys.)

is measured using a fast current measurement unit[125]. The measurement delay is defined as 400 ns in the case of $M=4$ and $N=54$ as shown in the initial measurement curve (no degradation) of Fig. 3.22.

In the simulation result of Fig. 3.21, an ideal power source is used for the node VPS in Fig. 3.20. On the other hand, DC bias is provided by the SMU of the semiconductor parameter analyser[124]. This SMU needs a few μs time for the worst case to provide a stable output after the current starts to flow from this SMU. The ratio of this current to the current range of the SMU determines the time until the SMU output becomes stable. In the leakage current case, where the number of DUTs is 2160, it is 400 ns and it limits the measurement delay to 400 ns. When the number of DUTs is increased from 2160 to 10000, the measurement delay also monotonically increases and it is a few μs for the case of 10000 DUTs. The measurement sequence in Fig. 3.20 can avoid channel hot carrier injection (HCI) because all the DUTs are in the off state during stress and measurement. Figure 3.23 shows a chip micrograph. The physical gate oxide thickness is 1.7 nm, W/L (drawn) of DUT is 11.75, and the minimum L is 50 nm (physical). It was fabricated in a commercial 65 nm CMOS technology.

Figure 3.24 shows the gate bias condition of Leakage Current (LC) NBTI characterization method. V_{gstress} represents the gate bias under the stress phase and the gate bias under the recovery phase is set to 0 V. The initial measurement is done before the stress phase and the recovery phase follows. The source, the drain and the substrate bias are usually kept to 0 V but the drain bias is set to some finite negative value only in the measurement duration. All measurements

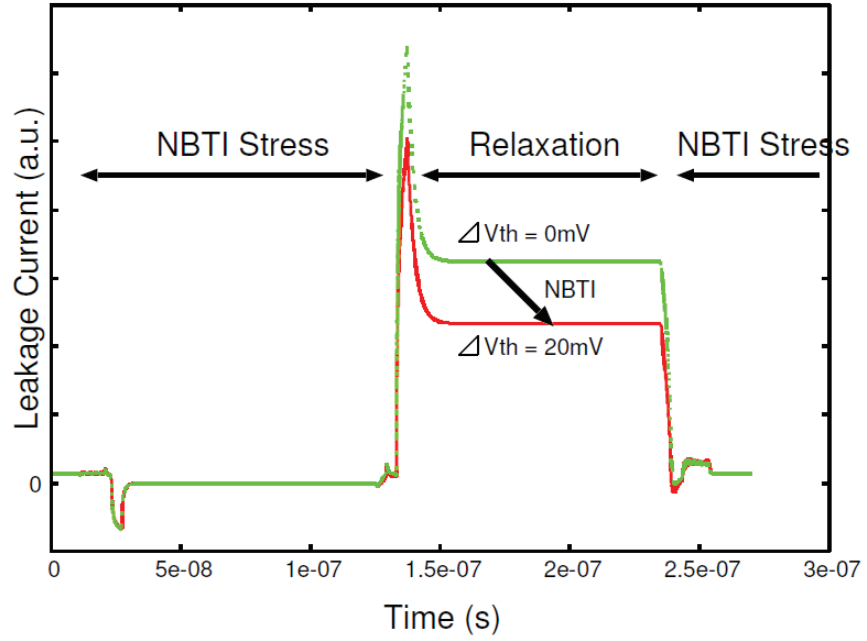


Figure 3.21: Simulation result of current at node Q in Fig. 3.20. $\Delta V_{th} = 0$ mV line means the fresh sample case and $\Delta V_{th} = 20$ mV line means the degraded case. (© 2011 Japan Soc. App. Phys.)

are done in the same bias condition (leakage current monitoring condition) in the LC method.

Figure 3.25 shows the measurement results of NBTI stress phase with 2160 pMOS DUTs ($M=4$ and $N=54$) for various measurement delays. The vertical axis is the leakage current degradation normalized to the initial leakage current ($\Delta I/I_0$). The horizontal axis is the stress time. Both the horizontal axis and the vertical axis are log scale. The measurement delay varies such as 250 ns, 1 μ s, 100 μ s, 10 ms, and 100 ms. The bias during the stress phase is $V_{gs} = -2.2$ V, $V_{ds} = 0$ V, and $V_{sub} = V_s$, and the bias during the measurement phase is $V_{gs} = 0$ V, $V_{ds} = -2.2$ V, and $V_{sub} = V_s$. The stress temperature is 125°C. It is clarified that all the degradation data follow power law (t^n) behavior. As the measurement delay increases, the slope n also increases due to the NBTI recovery during the measurement interruption. Because the measurement is done at $V_{gs} = 0$ V for the LC method, recovery is more pronounced than the usual MSM method. Fast measurement is necessary for the LC NBTI characterization under degradation phase. This circuit can greatly suppress the NBTI recovery during the NBTI degradation characterization.

3.3. High-Fidelity NBTI Recovery Characterization by Leakage Current (LC) Method41

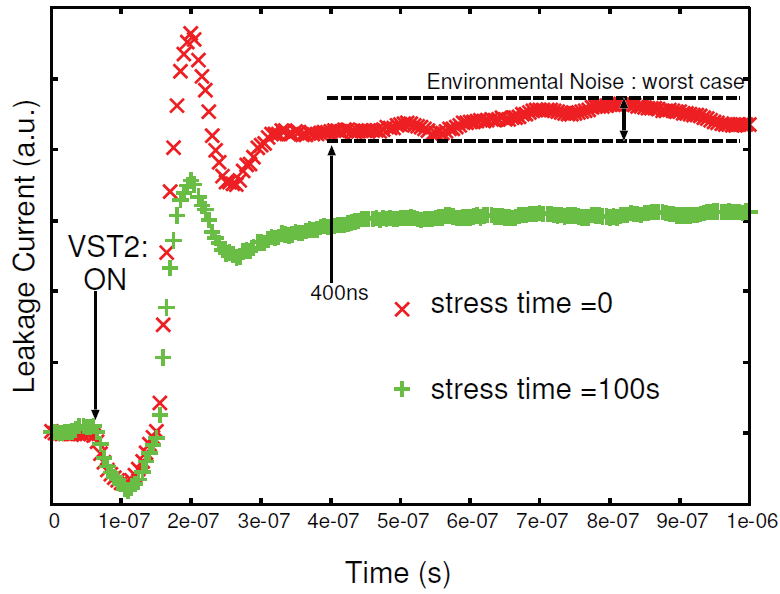


Figure 3.22: Measurement result of the current at node Q is shown. The measurement delay is 400 ns in the case of $M = 4$ and $N = 54$. (© 2011 Japan Soc. App. Phys.)

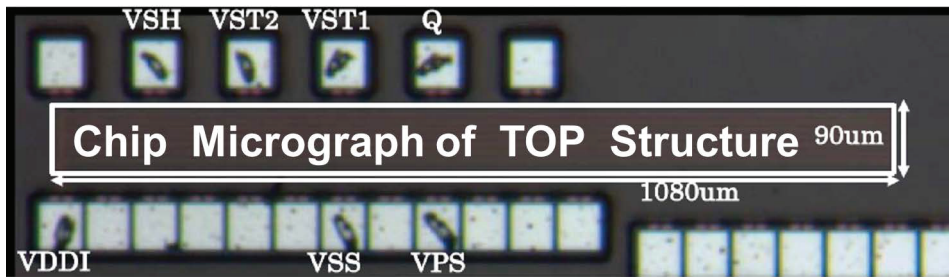


Figure 3.23: Chip micrograph fabricated in a 65nm CMOS. (© 2011 Japan Soc. App. Phys.)

Figure 3.26 shows the measurement results of NBTI recovery with 2160 pMOS DUTs ($M=4$ and $N=54$) after a 1000 s stress. The horizontal axis is the log scale and the vertical axis is the linear scale. The current integration time is also shown and the integration time is set to the optimal value corresponding

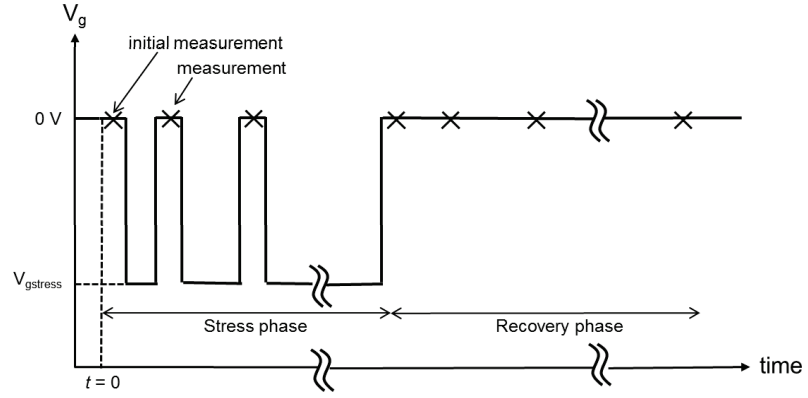


Figure 3.24: Gate bias condition of leakage current (LC) NBTI characterization method.

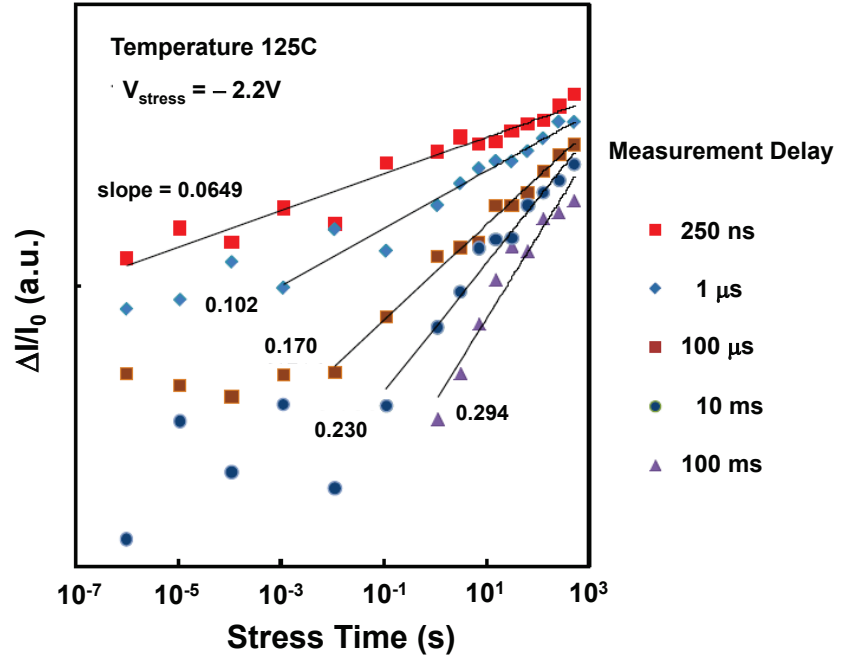


Figure 3.25: Measurement results of NBTI degradation under the stress phase with 2160 pMOS DUTs ($M=4$ and $N=54$) for various measurement delays.

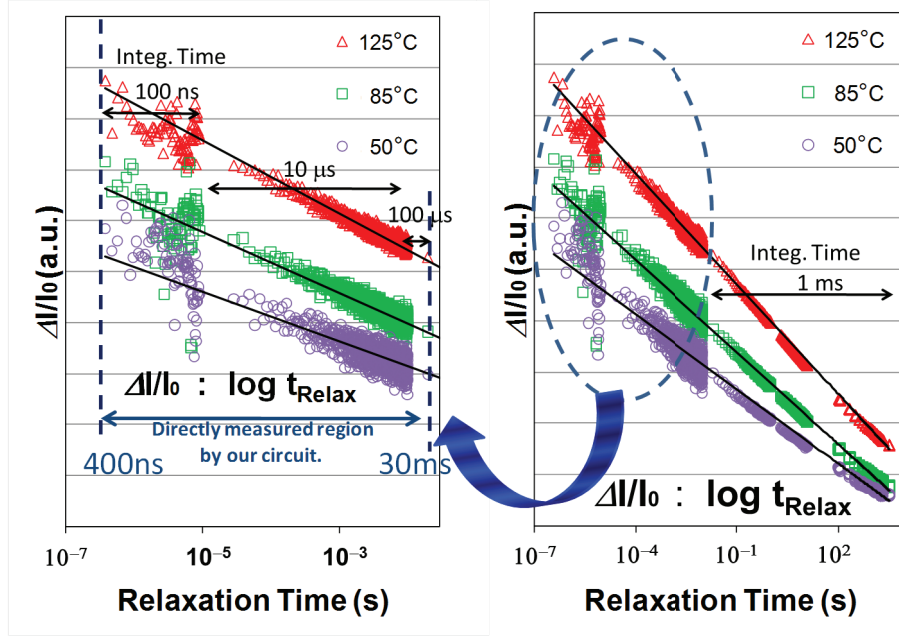


Figure 3.26: NBTI recovery measurement by the proposed circuit. NBTI recovery follows $\log t$ from 400 ns for all temperatures. Fitting lines ($\log t$) to the experimental data are also shown. (© 2011 Japan Soc. App. Phys.)

to the relaxation time. When the current integration time is below 100 μs , the measurement points have some variation owing to environmental noise that is as large as the environmental noise shown in Fig. 3.22 for the worst case. After one sample is stressed at one temperature for 1000 s, it is recovered for 3000 s at the same temperature. The temperature is varied from 50 to 125°C. The measurement delay as defined in Fig. 3.20 is 400 ns. Proposed circuit can measure the unknown region in Fig. 3.17. NBTI recovery clearly follows $\log t$ from 400 ns to 3000 s for all temperatures. This is because the time constants of positively charged defects are log-uniformly distributed in the pMOS devices[129]. What is observed in Fig. 3.26 is the averaged recovery behavior of 2160 pMOS transistors connected in parallel. Such a $\log t$ behavior can be observed without measuring many single transistors individually. When a DUT is in the recovery mode, it is in the off state. Thus, there is no perturbation to the gate bias of DUTs. This enables high-fidelity NBTI recovery measurement, and other conventional methods do not have such a high fidelity.

Finally, the amount of the recoverable component is clarified quantitatively by the LC method, which is a crucial step for lifetime extension. The amount of the recoverable component can be measured by using MSM method and LC

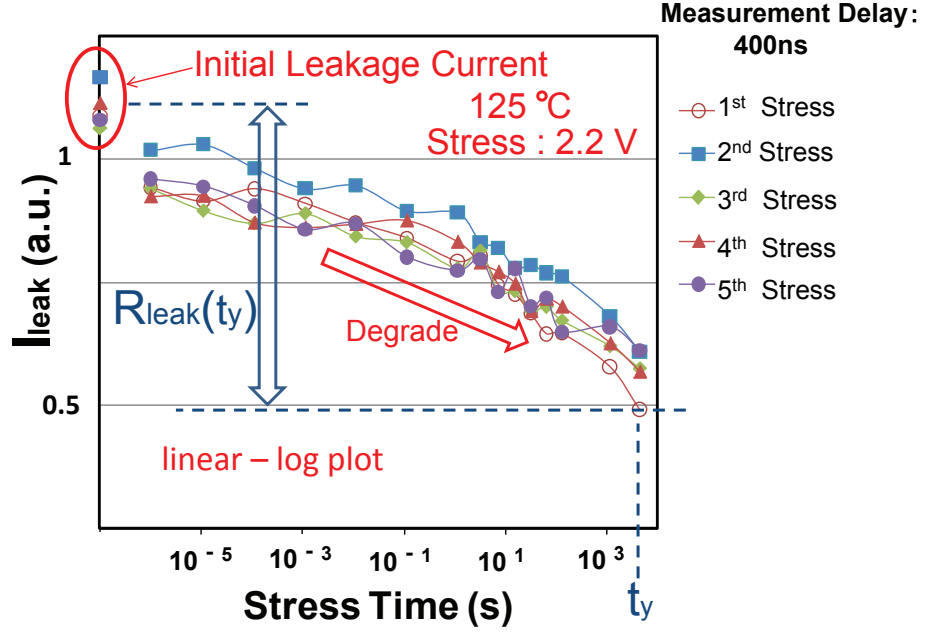


Figure 3.27: The off-leak current decreases with stress time compared with its initial value. The measured recoverable component using the off-leak current remains almost constant after repeatedly adding NBTI stress. The amount of the recoverable component is denoted by $R_{leak}(t_y)$ for the stress time t_y . (© 2012 Japan Soc. App. Phys.)

method. Figure 3.27 shows that the leakage current decreases with stress time compared with its initial value that is also plotted in the same figure. The biases of 2160 pMOS transistors during the stress phase are $V_{gs} = -2.2$ V, $V_{ds} = 0$ V, and $V_{sub} = V_s$, and the biases during the measurement phase are $V_{gs} = 0$ V, $V_{ds} = -2.2$ V, and $V_{sub} = V_s$. The stress temperature is 125 °C. The NBTI degradation rate of a one-year order nominal operating condition generally roughly corresponds to the order of 1%. When pMOSFET is stressed at $V_{gs} = -2.2$ V and 125 °C as in Fig. 3.27, the stress time of 2000 s generally roughly corresponds to one-year order circuit operation at room temperature and a nominal operating voltage. After adding this 2000 s NBTI stress to a DUT, the off-leak current decreases to about half of its fresh value. After sufficient recovery, the off-leak current of the same DUT is again measured, and it is found that the off-leak current almost recovers to its fresh value, as shown in Fig. 3.27. This DUT is further repeatedly stressed under the same stress condition, and it is found that the initial off-leak current always recovers to its

fresh value, as shown in Fig. 3.27. This means that the recoverable component shown in Fig. 4.1 measured using the off-leak current remains almost constant after repeatedly adding NBTI stress. The amount of the recoverable component is denoted by $R_{\text{leak}}(t_y)$ for the stress time t_y . Recoverable component can be characterized by the MSM or the LC method. On the other hand, the permanent component can be characterized by the MSM method as already described. LSI performance can be recovered by NBTI recovery. Its lifetime can be further extended by repeatedly recovering degraded circuits. This concept is further described in Chapter 4.

3.4 Chapter Summary

This chapter described NBTI degradation and recovery measurement results at a transistor-level with fast characterization method. In the NBTI characterization results by the MSM method, the measurement delay is kept to be as short as $1\ \mu\text{s}$. The transistor is fabricated in a commercial 65 nm CMOS technology. The device degrades rapidly in the early phase of the degradation that is followed by the rapid recovery in the early phase of the recovery. The recovery saturates after several thousands of the recovery time but the saturation level slightly increases as the number of degradation-recovery cycle increases. It is considered that the monotonic increase of the saturation level is due to the permanent component accumulation. Although MSM method suffers from NBTI recovery during NBTI characterization, these results are obtained with a comparably short measurement delay when it is compared with other papers. Even in this method, about 20% recovery is already observed at $t = 2\ \mu\text{s}$ for the each recovery cycle. When each recovery starts from various degradation levels, it is found that all data recover in a similar way. The weak dependence of the recovery on degradation level helps recovery modeling much simpler. How to include observed recovery results into a circuit simulation model is remained to be a future work.

To compensate the MSM method, the leakage current (LC) method that has the highest fidelity to NBTI recovery measurement is developed in this thesis. This chapter has described an LC method-based NBTI-recovery sensor with a 400 ns measurement delay that includes many unit cells of ten pMOS DUTs and two assist nMOS devices. NBTI recovery monitored by the leakage current is found to follow $\log t_{\text{recovery}}$ where t_{recovery} is the recovery time. It is confirmed for the first time in the region of $400\ \text{ns} \leq t_{\text{recovery}} \leq 30\ \text{ms}$. By degrading and recovering thousands of pMOS transistors at the same time, we can observe that the time constants of positively charged defects, which are related to NBTI, are log-uniformly distributed in the pMOS devices. Measurement results by the LC method show that the recoverable component measured using the off-leak current remains almost constant after repeatedly adding NBTI stress. Recoverable component is shown to be characterized by the MSM or the LC method. Permanent component is shown to be characterized by the MSM method.

Chapter 4

Multicore LSI Lifetime Extension by NBTI Recovery based Self-healing

Previous chapter gives information of the recoverable and the permanent component in NBTI degradation. Making the most of NBTI recovery, this chapter describes a multicore LSI lifetime extension method. Section 4.1 describes the concept of LSI lifetime extension by NBTI recovery based self-healing. It is applied to a multicore LSI lifetime extension in Section 4.2. Combined with NBTI recovery, circuit parallelization plays an important role for the lifetime extension. It is shown for the first time that transforming silicon area into LSI lifetime is a promising and realistic concept.

4.1 Concept of LSI Lifetime Extension by NBTI Recovery based Self-healing

The impact of the reliability of transistors that construct the synchronous circuit has increased in recent years. As already described in Section 2.2, NBTI is one of the major concerns for the recent transistor reliability that is related to a physical property of a very thin gate oxide insulator. When transistors degrade owing to NBTI, the propagation delay of combinational logic increases. The correct operation of a register may not be guaranteed. Furthermore, the timing of registers that is generated by a clock tree may be skewed. As a result, owing to NBTI degradation, the circuit does not operate correctly or does not reach the lower limit of LSI performance. The lower limit of LSI performance means the lowest acceptable spec of the LSI performance. Figure 4.1 shows that LSI performance degrades with time and finally reaches its lifetime, for example, 10 years, which is defined by the lower limit of LSI performance. If LSI performance is recovered by NBTI recovery, its lifetime can be further extended, as shown

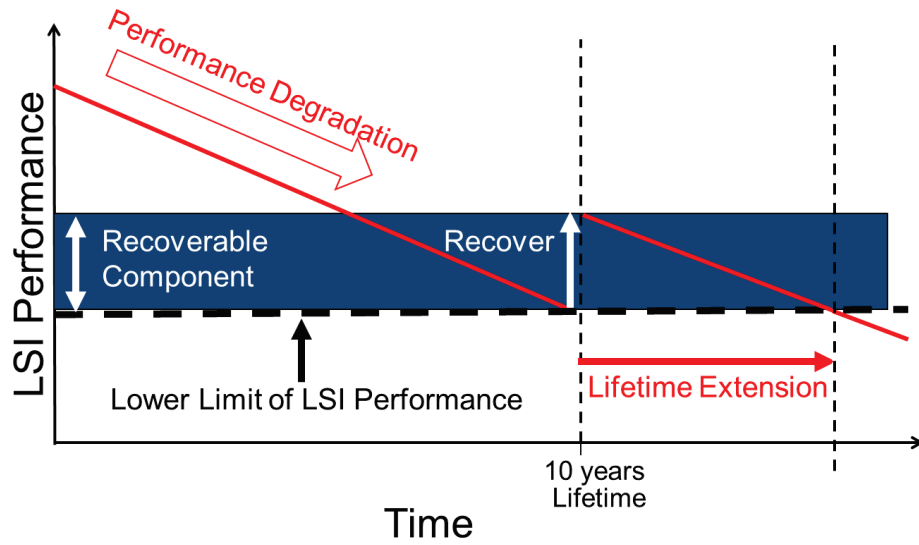


Figure 4.1: Degraded LSI performance can be recovered by NBTI recovery that leads to LSI lifetime extension. (© 2012 Japan Soc. App. Phys.)

in Fig. 4.1. NBTI degradation under normal operating conditions is a gradual process, whereas NBTI recovery is a fast process. Thus, the recovery time is very short in Fig. 4.1. As a result, it is a crucial step for this lifetime extension method with NBTI recovery to clarify the amount of the NBTI recoverable component shown in Fig. 4.1. The nature of the recoverable component have already been clarified in Chapter 3 by using the MSM method or the LC method. By the MSM method, it is clarified that 10–20% of NBTI degradation becomes unrecoverable and 80–90% of that becomes recoverable (Fig. 3.10). Because most of the degraded component can be recovered, the lifetime extension method with NBTI recovery is very effective in this technology.

4.2 Multicore LSI lifetime Extension Method

The recent scaling of the CMOS device leads to circuit parallelization or multicore architecture in many applications[130]. Conventionally, yield is improved, power is decreased, and the hot spot on a die is decreased by circuit parallelization. For example, it is described that with the continuing trend of the denser technology through scaling, a new degree of freedom in architectural design has been made possible, in which silicon area can be traded off against power consumption[131].

This section describes for the first time that transforming silicon area into LSI lifetime is a promising and realistic concept for the ever-shrinking CMOS

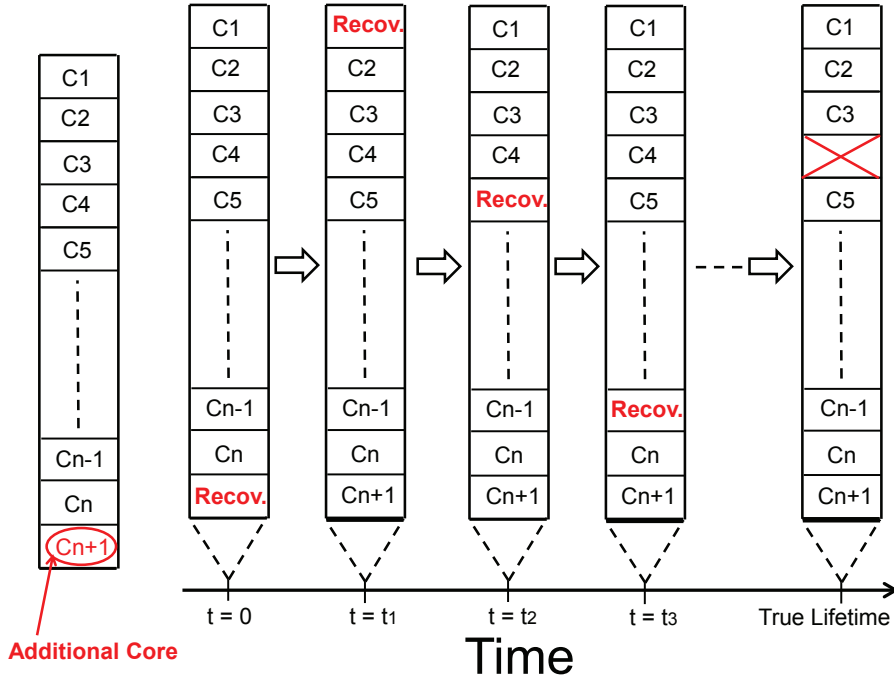


Figure 4.2: An example of $(n + 1)$ -core LSI (C_1 - C_{n+1}) operation is shown. Shortly before C_1 reaches its lifetime at $t = t_1$, C_1 becomes the recovery mode, and C_{n+1} becomes the active mode. By recovering one of the $n + 1$ cores, the n -core LSI system does not stop and the lifetime can be extended by NBTI recovery. (© 2012 Japan Soc. App. Phys.)

technology. Figure 4.2 shows the $(n + 1)$ -core LSI (C_1 - C_{n+1}). It is a homogeneous $(n + 1)$ -core LSI, and one core is always set to the sleep mode (or NBTI recovery mode). It is assumed that each core reaches its lifetime at a different time because of the process variation and different workload. When one core reaches its lifetime faster than any other cores, this core is set to the sleep mode instead of the previously recovered core, and the previously recovered core is set to the active mode. For example, shortly before C_1 reaches its lifetime at $t = t_1$, C_1 becomes the recovery mode, and C_{n+1} becomes the active mode. Thus, this LSI keeps n -core circuits active. As a result, by recovering one of the $n + 1$ cores, the n -core LSI system does not stop and the lifetime can be extended to the “true lifetime” in Fig. 4.2 by NBTI recovery [originally, the lifetime is only t_1 for n -core (C_1 - C_n) LSI]. The recovery time is at most 1 hour. Furthermore, both C_1 and C_{n+1} operate under the same workload for a short time (around

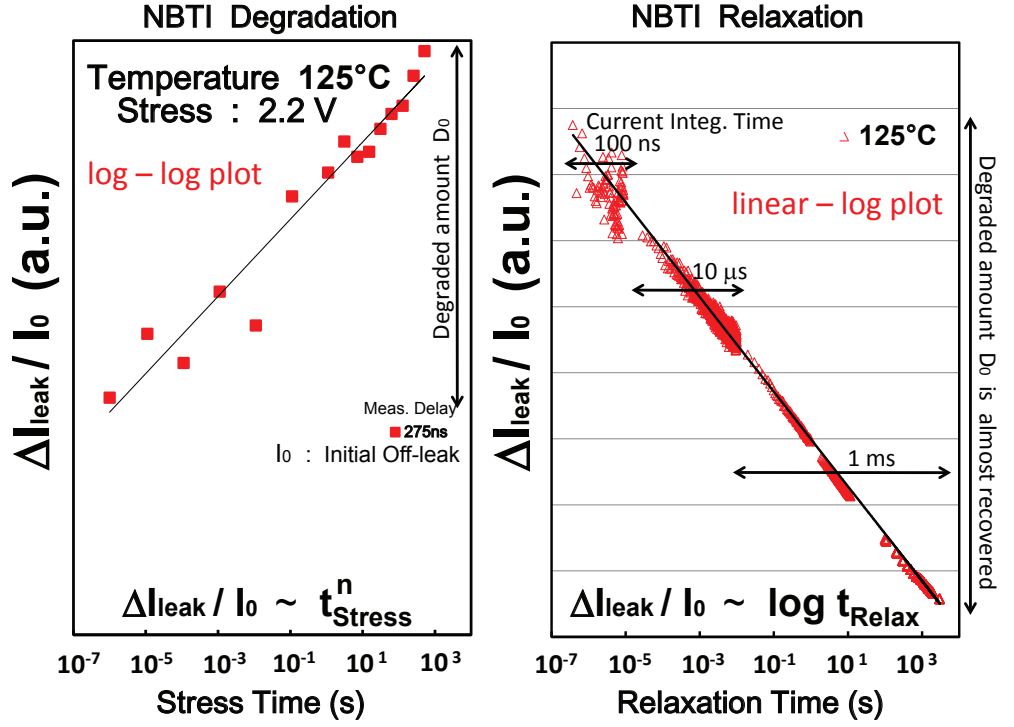


Figure 4.3: (left) The measurement result of NBTI degradation follows power law. (right) The measurement result of NBTI recovery follows $\log t$. In the case of nominal operation, the relaxation speed is much higher than the degradation speed. Owing to this asymmetrical nature of NBTI, lifetime extension by NBTI recovery is a very effective method. (© 2012 Japan Soc. App. Phys.)

$t = t_1$) so as not to stop LSI operation when cores are exchanged.

In a real application, there may not be sufficient time to recover. It is necessary to know how the NBTI recovery occurs with respect to the recovery time. Characterizing recovery can be done by using the MSM method or the LC method as already described in Chapter 3. The degradation and the recovery characterization by the LC method in Section 3.3 is summarized in Fig. 4.3. Figure 4.3(right) shows that NBTI recovery clearly follows $\log t$ from 400 ns to 3000 s. By modeling the recovery behavior shown in Fig. 4.3(right), the amount of NBTI recovery can be tuned by the relaxation time in a real application. Figure 4.3(left) shows the NBTI degradation measurement result, and the degradation can be predicted on the basis of the power law behavior. Figure 4.4 shows the proposed LSI lifetime extension method by utilizing the recoverable

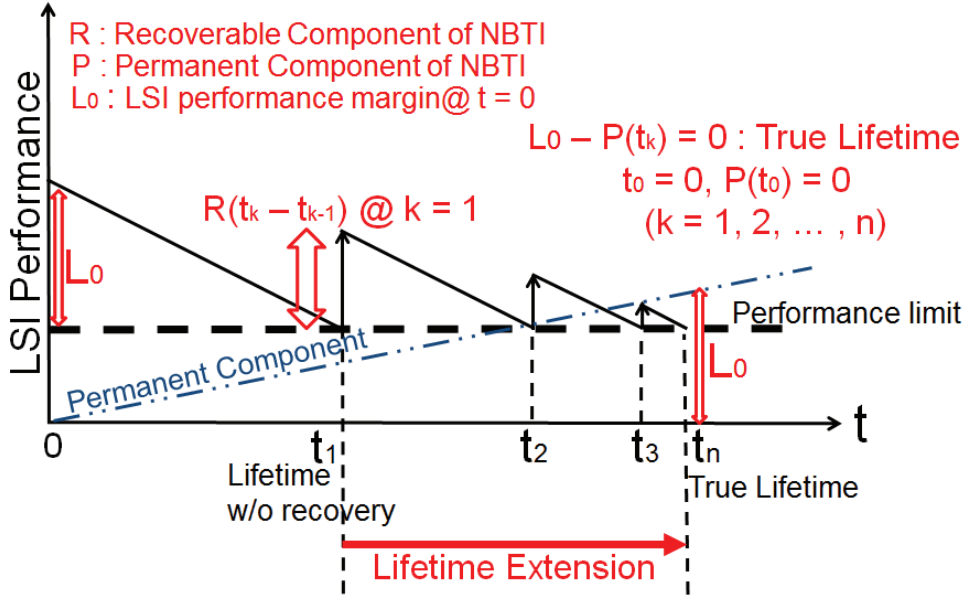


Figure 4.4: Concept of circuit operation to extend its lifetime. LSI performance can be repeatedly recovered until $L_0 = P(t)$. (© 2012 Japan Soc. App. Phys.)

component measured by the MSM method or the LC method. In Fig. 4.4, $R(t)$ is the recoverable component and $P(t)$ is the permanent degradation of NBTI at the (stress) time t . $P(t)$ is characterized by the MSM method (Fig. 3.10). L_0 is the LSI performance margin at $t = 0$. The permanent component $P(t)$ increases gradually with stress time t (conceptually shown in Fig. 4.4), and LSI performance can be recovered by $R(t_k - t_{k-1})$ at $t = t_k$. Shortly before LSI reaches its lifetime at $t = t_1$, LSI performance can be recovered by $R(t_1)$. LSI performance can be repeatedly recovered until $L_0 = P(t)$. The amount of $L_0 - P(t)$ gradually decreases because $P(t)$ gradually increases with time. When the power supply (VDD) decreases, the true lifetime can be further extended. NBTI degradation at a nominal operating voltage is a gradual process compared with the NBTI recovery that follows $\log t$ with a very fast component, as shown in Fig. 4.3(right). Owing to this asymmetrical nature of NBTI, lifetime extension by NBTI recovery is a very effective method. When process variation is considered, the performance margin defined in Fig. 4.4 decreases as the process becomes slow. Figure 4.3 shows that about 50% can be recovered for the recovery time of 1 ms. For the recovery time of 1 h, the degradation measured using the off-leak current is almost recovered. The degradation under nominal operation for 1 h can be ignored. As a result, more than two cores that reach their lifetime simultaneously can be detected at least 1 h before their

lifetime. In the case of using one additional core for recovery, the time to set the core to the recovery mode must be carefully tuned so that another core does not reach its lifetime during the recovery mode. In the case of multicore LSI at a given workload, NBTI-recovery-based self-healing by the additional core works effectively when the degradation speed of the slow process corner core is reduced.

4.3 Chapter Summary

It is shown that LSI lifetime can be extended by combining NBTI recovery and circuit parallelization. It is also shown that the amount of NBTI recovery can be tuned by the relaxation time in a real application. As a result, multicore LSI lifetime extension can be achieved. For the first time, transforming silicon area into LSI lifetime is shown to be a promising and realistic concept for the ever-shrinking CMOS technology.

Chapter 5

RTN Characterization of CMOS Transistors

Previous chapters described the impact of NBTI on CMOS circuit. This chapter describes RTN characterization of CMOS transistors. It is confirmed that RTN-induced transistor current fluctuation can be strongly influenced by both the gate bias and the substrate bias.

5.1 RTN Characterization at Transistor Level

In this section, RTN characterization at transistor level is described. Figure 5.1 shows the test structure schematic of nMOS 3×5 transistor array. G1, G2, $\dots$ and G5 represent gate terminals and D1, D2 and D3 represent drain

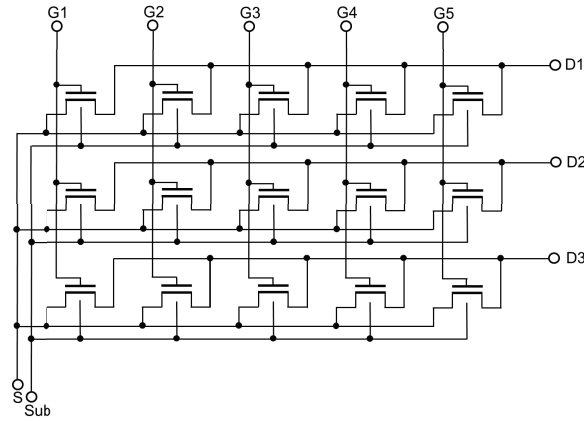


Figure 5.1: Test structure schematic of 3×5 transistor array.

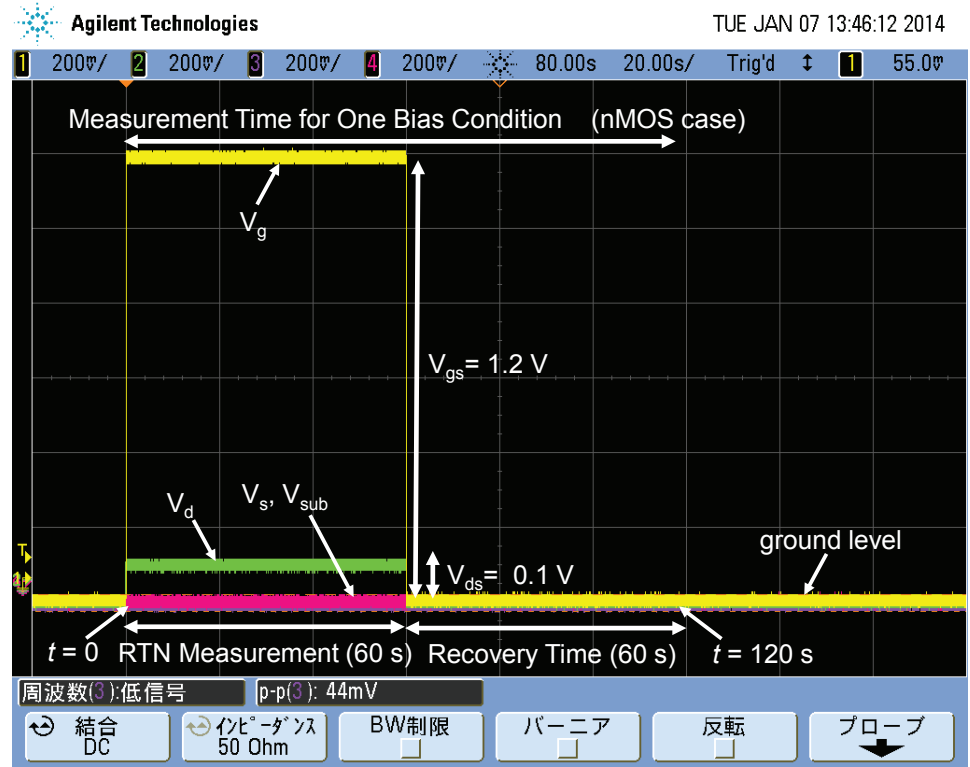


Figure 5.2: The bias condition of RTN characterization for nMOSFET case.

terminals. S and Sub represent source terminal and substrate terminal respectively. The array has ten external pads and they are connected to a commercial semiconductor parameter analyser[124, 125]. The test structure for pMOSFET is also the same as Fig. 5.1 (not shown). One of the 15 transistors is selected for RTN measurement. This test structure is fabricated in a commercial 65 nm CMOS technology. We use the minimum-size transistors for both nMOSFET and pMOSFET allowed in the technology.

Figure 5.2 shows the bias condition of RTN characterization for an nMOSFET case. Figure 5.2 shows the generated voltage waveform. V_g , V_d , V_s and V_{sub} mean gate bias, drain bias, source bias and substrate bias, respectively. The RTN measurement of 60 s is followed by the recovery time of 60 s for each bias condition. All four nMOSFET terminals are set to 0 V during the recovery time. Figure 5.2 shows an example of nMOSFET RTN measurement for $V_{gs} = 1.2$ V and $V_{ds} = 0.1$ V. The role of 60 s recovery time is to detrapp carriers trapped during the RTN measurement. Figure 5.3 shows the IV characteristic of 6 nMOS transistors in one test structure of Fig. 5.1. The horizontal axis is the absolute value of V_{gs} and the vertical axis (linear scale) is the absolute value of

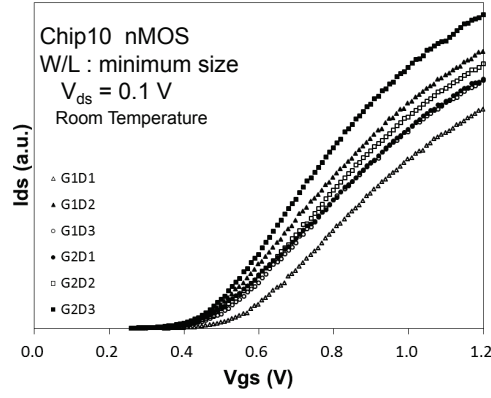


Figure 5.3: I_V characteristic of 6 nMOS transistors in one test structure of Fig. 5.1.

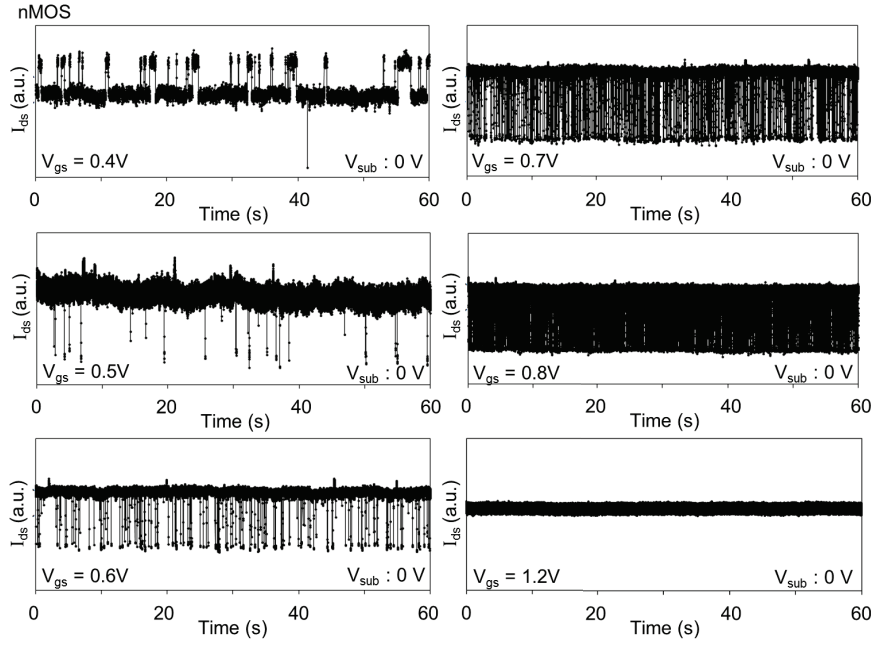


Figure 5.4: Voltage dependence of a two-state RTN.

I_{ds} . V_{ds} is set to 0.1 V to prevent hot carrier degradation during RTN measurement. All measurements are done in room temperature. The time constant of RTN is affected by the gate bias and the frequency of switching becomes higher if a trap energy level (E_T) is close to the Fermi level (E_F). Figure 5.4 shows

the RTN-induced nMOS drain current (I_{ds}) fluctuation of a single transistor for various gate biases (V_{gs}). The current integration time is 5 ms for $V_{gs} = 0.4V$, 0.5V and 500 μs for $V_{gs} \geq 0.6V$. When V_{gs} is increased from 0.6 V to 0.8 V, the two-state switching becomes more frequently but it disappears at 1.2 V. It indicates the gate bias gives a big influence on RTN. The power spectral density (PSD) of Fig. 5.4 is obtained by quantizing the measurement data into the 2-state waveform. Lorentzian power spectrum is obtained for $V_{gs} = 0.4V$, 0.6V, 0.7V and 0.8V (Fig. 5.5). The large two-state switching disappears for $V_{gs} = 1.2V$ and only a high frequency noise with small amplitude remains. Lorentzian power spectrum is not obtained for $V_{gs} = 0.5V$, because a frequent but a small two-state fluctuation and a large sharp fluctuation are superposed.

Figure 5.6 shows time constant (τ_c , τ_e) distributions of Fig. 5.5 for $V_{gs} = 0.8V$. Figure 5.6 is obtained after quantizing the measurement data of Fig. 5.4 into the 2-state waveform. As already suggested in Section 2.3, time constants follow exponential distribution,

$$\frac{1}{\langle \tau_c \rangle} \exp(-t/\langle \tau_c \rangle), \quad (5.1)$$

$$\frac{1}{\langle \tau_e \rangle} \exp(-t/\langle \tau_e \rangle). \quad (5.2)$$

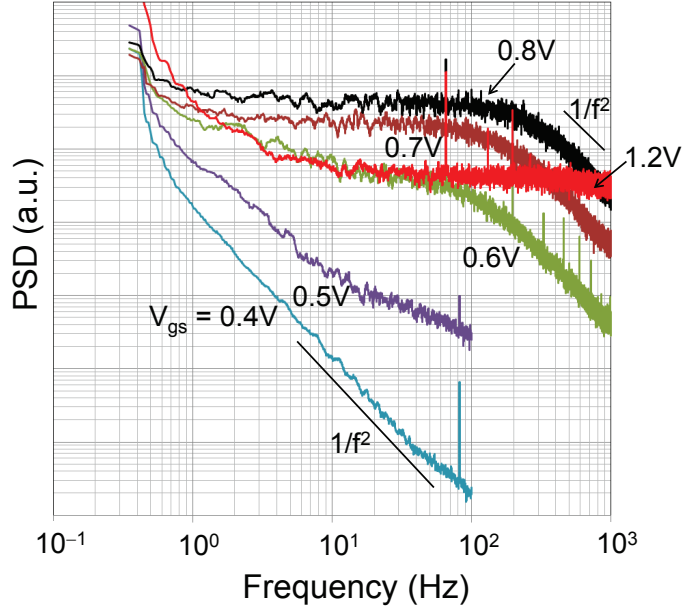


Figure 5.5: Power spectral density of Fig. 5.4 after the measured time domain data is exchanged to two-state waveform.

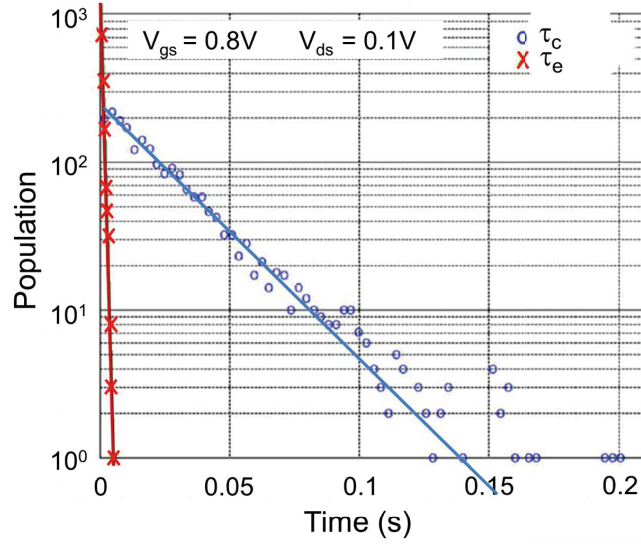


Figure 5.6: Time constant distribution of Fig. 5.4 ($V_{gs} = 0.8$ V).

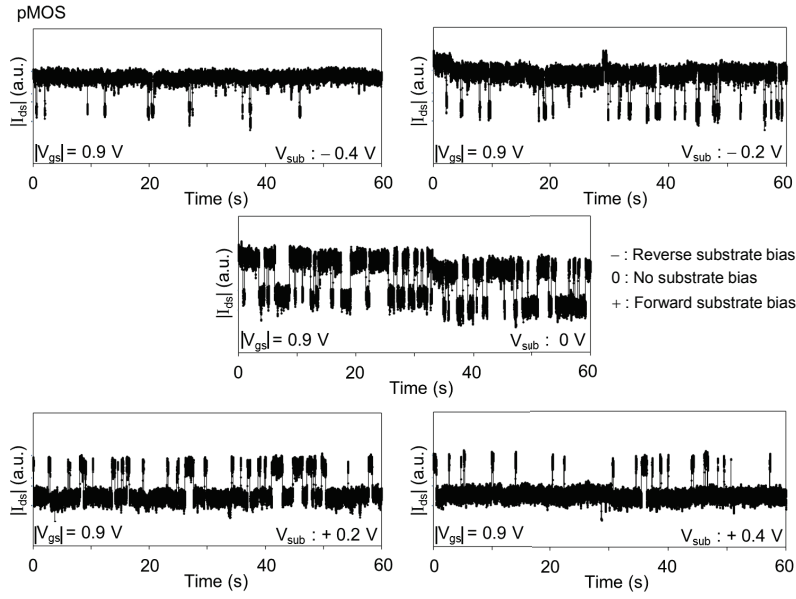


Figure 5.7: RTN-induced pMOSFET drain current fluctuation of one transistor for various substrate biases.

It is found that both distributions actually follow exponential distribution.

Figure 5.7 shows I_{ds} fluctuation for various substrate biases (V_{sub}) at $|V_{gs}| = 0.9V$. The body-biasing technique has been widely used to compensate for die-to-die parameter variations[132]. The body bias V_{sub} is changed between $-0.4V$ and $+0.4V$. The minus and plus signs in V_{sub} represent reverse bias and forward bias respectively. $V_{sub} : 0V$ is the zero body-bias condition. The large two-state RTN is observed for each V_{sub} . I_{ds} stays at the high-current state most of the time when the substrate is reverse-biased ($V_{sub} : -0.4V$), while it stays at the low-current state most of the time when the substrate is forward-biased ($V_{sub} : +0.4V$). I_{ds} stays almost equally at both states for the zero substrate bias case ($V_{sub} : 0V$). It suggests that RTN time constants can be strongly influenced by the substrate bias.

From these measurement results, it is confirmed that RTN-induced transistor current fluctuation can be strongly influenced by both the gate bias and the substrate bias.

5.2 Chapter Summary

This chapter has described RTN-induced transistor performance fluctuation. From the drain current RTN measurements in a 65 nm chip, it was described that I_{ds} fluctuation can be strongly influenced by both the gate bias and the substrate bias. Lorentzian power spectrum was obtained for a two-state fluctuation. Time constants followed exponential distribution.

Chapter 6

Impact of RTN on CMOS Logic Circuit Performance

This chapter describes the impact of RTN on CMOS logic circuit performance. The impact of RTN on CMOS logic circuit reliability is described based on our results from 40 nm test chips[94, 96]. Section 6.1 describes the test structure for RTN evaluation. Section 6.2 shows measurement results of combinational circuit delay fluctuation. Section 6.3 describes the impact of RTN on logic circuits under low voltage operation. Section 6.4 shows how an RTN-induced logic delay is influenced by the substrate bias. Finally, Section 6.5 deals with the impact of RTN-induced logic delay fluctuation with respect to that of process variation.

6.1 Test Structure for RTN Evaluation

In this section, a test structure for the statistical characterization of RTN-induced logic delay fluctuation is described. A logic path exists between two

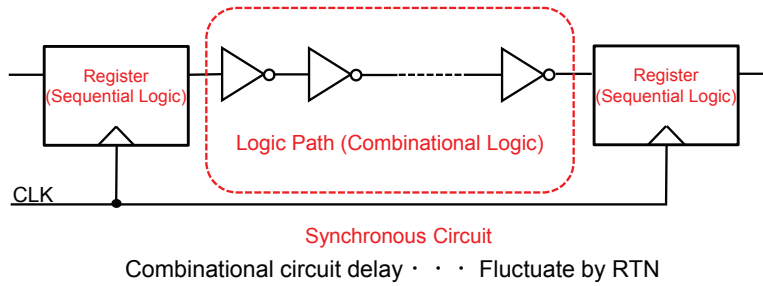


Figure 6.1: Typical synchronous circuit structure.

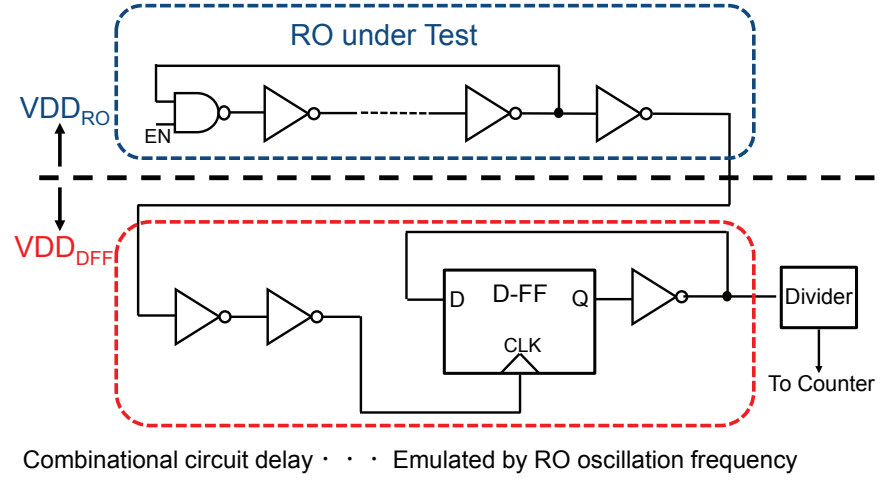


Figure 6.2: Simplest test structure that can emulate the synchronous circuit operation.

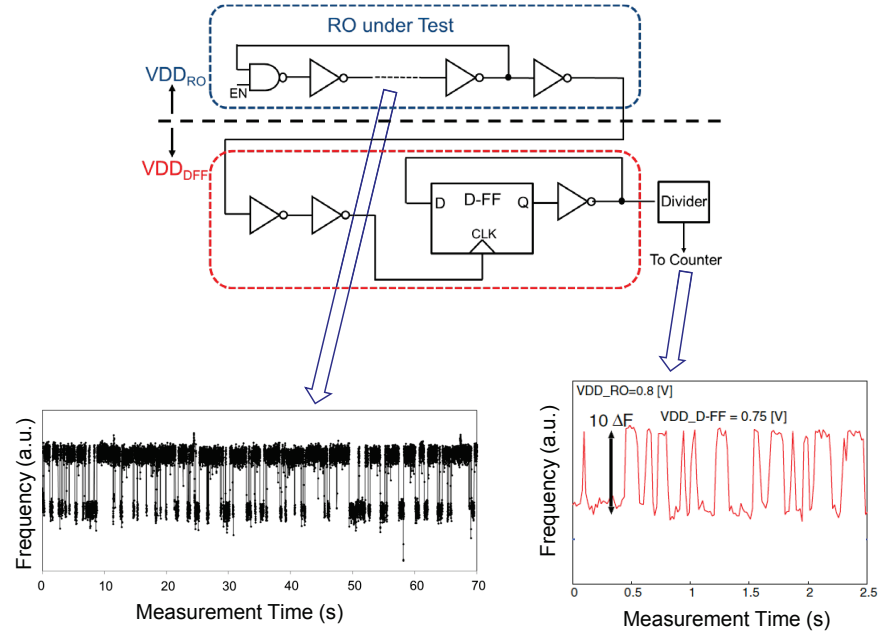


Figure 6.3: Impact of RTN on a synchronous circuit.

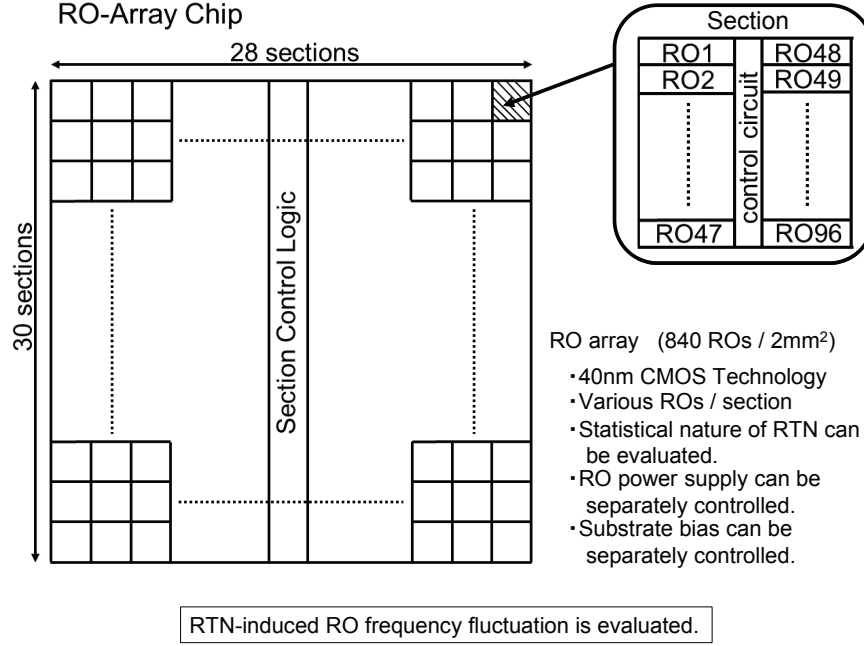


Figure 6.4: Whole test structure for RTN measurement. One test structure contains 840 ROs (30 ROs $\times$ 28 ROs).

registers in a typical synchronous circuit structure as shown in Fig. 6.1. When RTN occurs in the logic path, propagation delay of the logic path fluctuates with time. Figure 6.2 shows a simple test structure that can emulate the synchronous circuit operation of Fig. 6.1. In Chapter 5, RTN-induced drain current fluctuation is evaluated under a DC bias condition. Four biases of a transistor are fixed during a 60 s RTN measurement. In this chapter, combinational circuit delay is emulated by ring oscillator (RO) oscillation frequency. The gate bias of a transistor in the RO is switching corresponding to the RO oscillation frequency during RTN evaluation. All logic gates except NAND2 with EN input are homogeneous in this chapter. Sequential circuit operation is emulated by D flip-flop (DFF) toggled by the RO output. The power supply for RO ($V_{DD_{RO}}$) and DFF ($V_{DD_{DFF}}$) can be independently supplied. The substrate bias for pMOSFET and nMOSFET can also be controlled. Figure 6.3 shows the impact of RTN on a synchronous circuit. These are actual measurement data in 40 nm and 65 nm CMOS technologies. The left data is obtained by the RO of an inverter chain fabricated in a commercial 40 nm CMOS technology[94, 96]. A DFF that is used in the register has a maximum operating frequency (MOF). The right data in Fig. 6.3 is obtained when the input frequency to the DFF is close to the MOF[93]. Under 0.75 V operation, a large frequency fluctua-

tion is observed at the counter output after the DFF and dividers. The DFF is fabricated in a commercial 65 nm CMOS technology. Figure 6.4 shows the whole test structure for the RTN measurement. RTN-induced delay fluctuation is measured by the RO frequency fluctuation. Various types of ROs are included in one circuit unit, which is called a section. One section contains 96 different ROs. There are 840 identical sections on 2 mm² area. The statistical nature of RTN can be evaluated by the RO array. Only one RO is activated for the oscillation to reduce an external noise during the RTN measurement. This chip is fabricated in a commercial 40 nm CMOS technology. All measurements are done at room temperature.

6.2 Measurement Results of Logic Delay Fluctuation

Figure 6.5 (a) shows measurement results of oscillation frequencies of two 7-stage ROs for about 80 s at $V_{DD_{RO}} = 0.65V$. The size of the inverter (INV) is smallest in this technology. The body bias for pMOSFET ($V_{bs-pMOS}$) and nMOSFET ($V_{bs-nMOS}$) are set to 0V. Measurement results show the large step-like frequency fluctuation. Here, F_{max} is defined as the maximum oscillation frequency and ΔF is defined as the maximum frequency fluctuation as shown in Fig. 6.5(a). $\Delta F/F_{max}$ is a good measure for the impact of RTN-induced

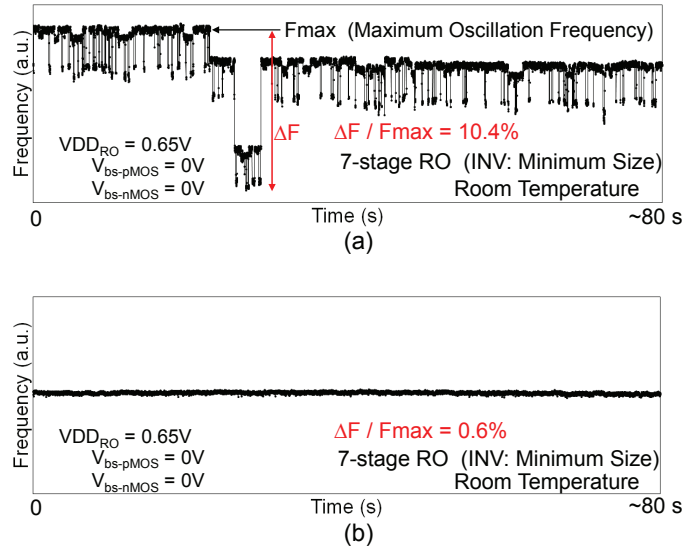


Figure 6.5: Measurement result of RTN-induced RO frequency fluctuation. (a) $\Delta F/F_{max} = 10.4\%$ (b) $\Delta F/F_{max} = 0.6\%$.

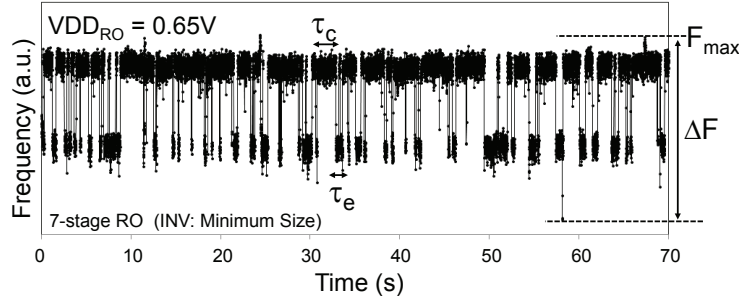


Figure 6.6: Measurement results that contains large 2-state fluctuation.

frequency fluctuation for logic delay. It is 10.4% for one RO (Fig. 6.5(a)). However, significant fluctuation is not observed for another RO (Fig. 6.5(b)). Although large fluctuation such as Fig. 6.5(a) is a rare event, it has a large impact on circuit performance. Figure 6.6 shows a typical measurement data of a 7-stage RO at $VDD_{RO}=0.65V$ that contains a large 2-state fluctuation. Time constants τ_c and τ_e represent the time that the RO stays at high-frequency state and low-frequency state respectively. The PSD of Fig. 6.6 is obtained by quantizing the measurement data of Fig. 6.6 into a 2-state waveform. Figure 6.7 shows Lorentzian power spectrum obtained from Fig. 6.6. Figure 6.8 shows time constant (τ_c , τ_e) distributions of Fig. 6.6. It is found that both distributions for τ_c and τ_e follow exponential distribution ($e^{-t/\tau}$). Lorentzian PSD and $e^{-t/\tau}$ distribution are observed for the case of a transistor where a single defect causes RTN fluctuation (Fig. 5.4, 5.5 and 5.6). It indicates that the large 2-state RTN fluctuation of Fig. 6.6 is caused by a single defect in a specific transistor in the 7-stage RO. Due to RTN, various complex frequency fluctuations are observed.

Figure 6.9 shows the histogram of measured $\Delta F/F_{\max}$ for the whole test structure of Fig. 6.3 over three chips (2,520 ROs). It is found that a small number of samples have a large RTN-induced fluctuation and a long tail exists for larger $\Delta F/F_{\max}$.

6.3 Impact of RTN on CMOS Logic Circuit under Low Voltage Operation

In this section, the impact of RTN on logic circuit reliability is described. As shown in Fig. 6.10, the distribution of RO frequency ($F_{\max}$) variation for 7-stage ROs follows normal distribution when data are collected from the whole test structure of Fig. 6.3 over 15 chips (12,600 ROs) under 0.65V operation. Figure 6.11 is the distribution of $\Delta F/F_{\max}$ for the same ensemble. The maximum value of $\Delta F/F_{\max}$ becomes 16.8%. It is found that a small number of samples have a large RTN-induced fluctuation. Compared with Fig. 6.9, the tail in the

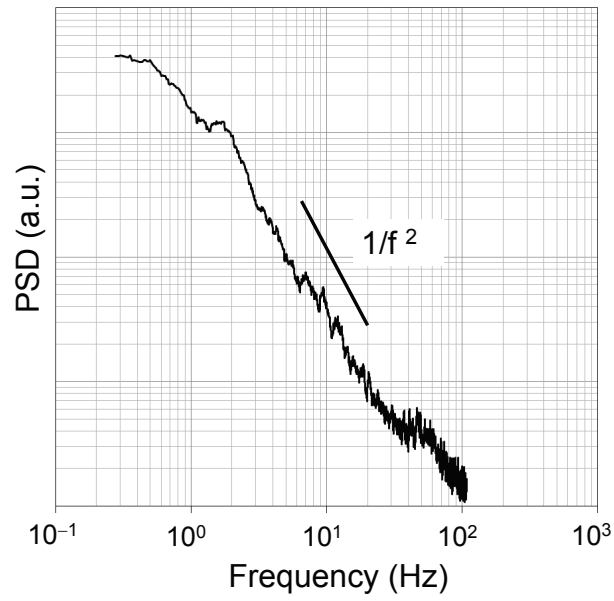


Figure 6.7: Power spectrum density of Fig. 6.6.

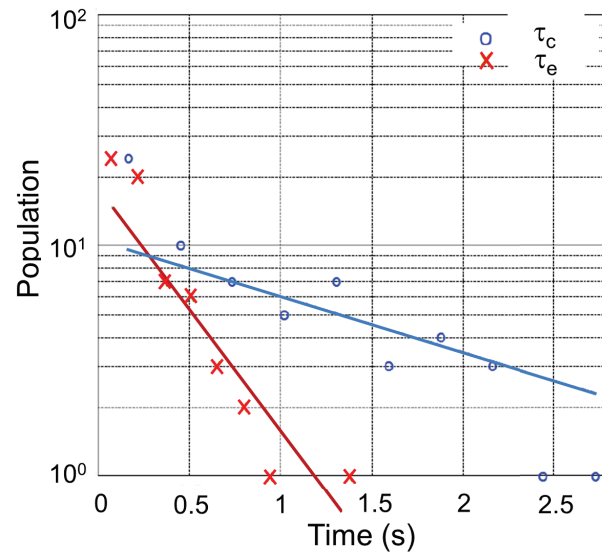


Figure 6.8: Time constant distribution of Fig. 6.6.

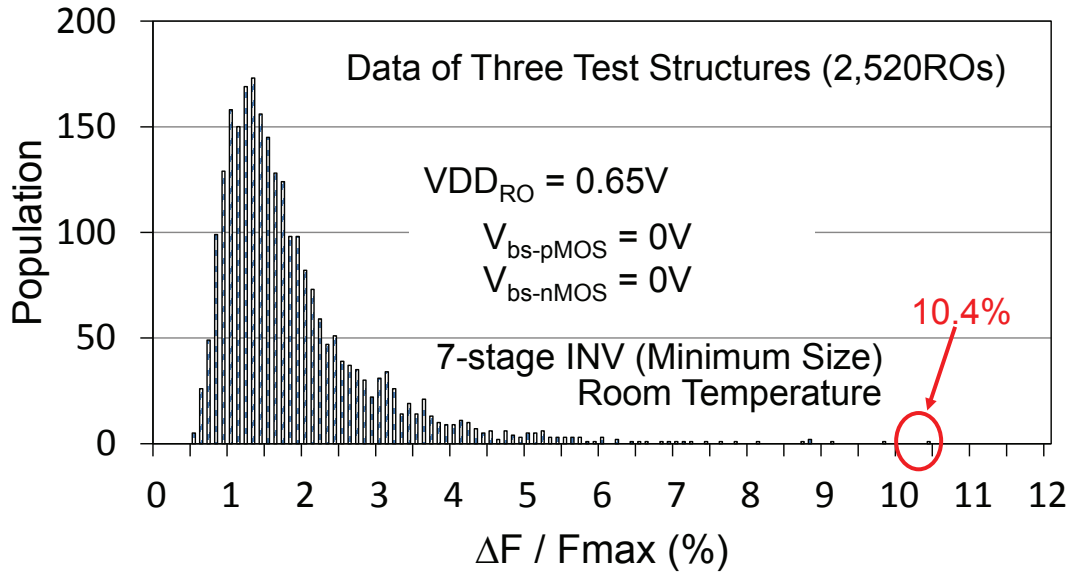


Figure 6.9: Histogram of measured $\Delta F / F_{\max}$ (© 2012 IEEE).

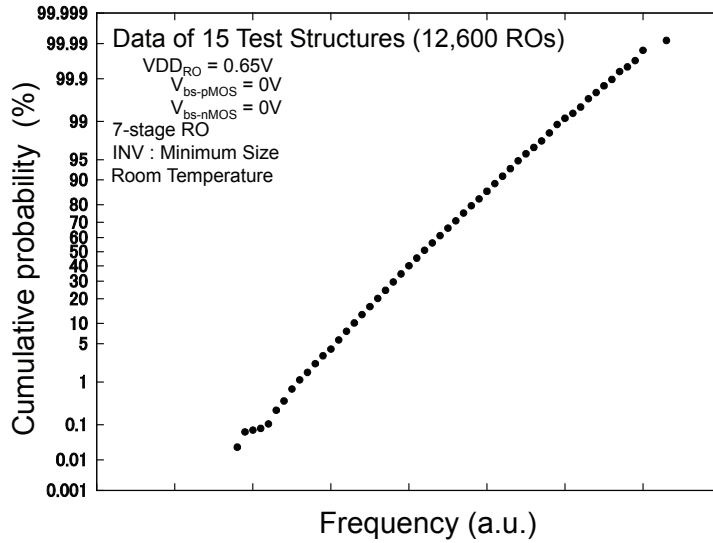


Figure 6.10: Normal distribution plot of RO frequency ($F_{\max}$) variation caused by process variation.

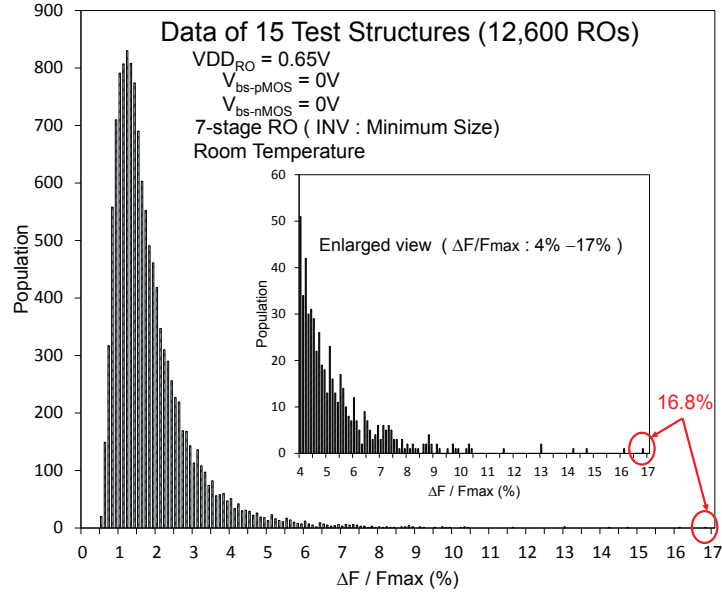


Figure 6.11: Histogram of RO frequency fluctuation ($\Delta F/F_{max}$) using the same ensemble of Fig. 6.10.

distribution becomes longer because RO sample number increases. Figure 6.11 is the cumulative probability of $\Delta F/F_{max}$ calculated from the distribution. The horizontal axis is $\Delta F/F_{max}$ that is plotted with log scale. The distribution follows a log-normal distribution above 50% level in cumulative probability. The maximum value of $\Delta F/F_{max}$ becomes 16.8%. If $\Delta F/F_{max}$ follows the log-normal distribution up to 6σ level, $\Delta F/F_{max}$ becomes as much as 60%. These results suggest the impact of RTN-induced fluctuation increases when it is compared with the frequency variation caused by manufacturing process. When the supply voltage decreases, the impact of ΔV_{th} caused by RTN becomes larger as shown in Fig. 6.13. Log-normal plot of $\Delta F/F_{max}$ for $V_{DD_{RO}} = 1.0V$, $0.75V$ and $0.65V$ over the same 840 ROs indicates the rapid increase of $\Delta F/F_{max}$ towards lower $V_{DD_{RO}}$. The impact of RTN also becomes larger as the gate area shrinks and the number of stages decreases. Figure 6.14 indicates more than 50% reduction of $\Delta F/F_{max}$ at 95% level in cumulative probability can be achieved by increasing the INV size for 7-stage RO under $0.75V$ operation. Here, the ratio of pMOSFET and nMOSFET gate areas ($W \times L$) of the minimum size INV to the standard size INV is 0.21 and 0.30 respectively. Figure 6.15 shows that the impact of RTN becomes larger as number of stages decreases from 19-stage to 7-stage. The impact of supply voltage, gate area and number of stages on $\Delta F/F_{max}$ is summarized in Fig. 6.16. The impact of RTN is drastically reduced by increasing supply voltage, gate area and number of stages.

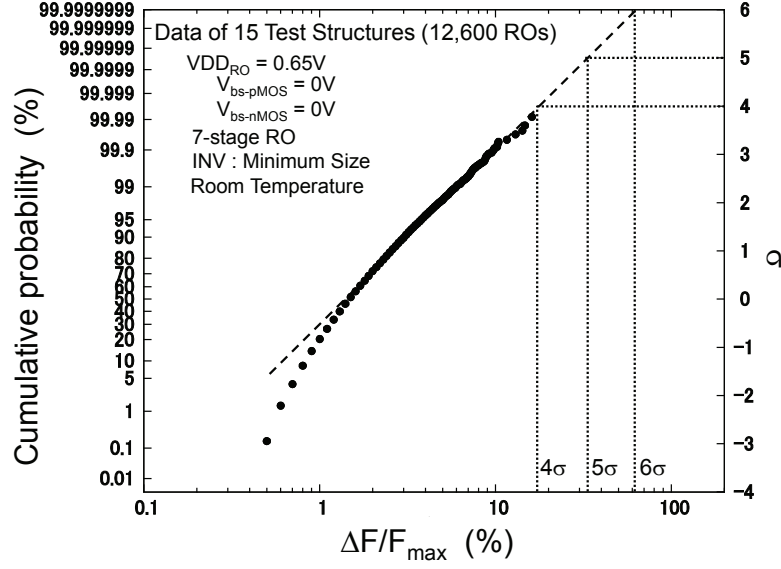


Figure 6.12: Log-normal distribution plot of Fig. 6.11.

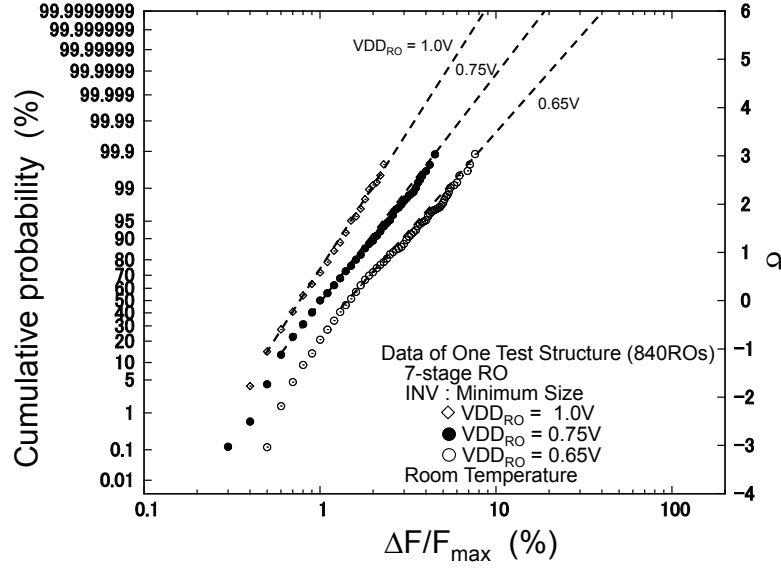
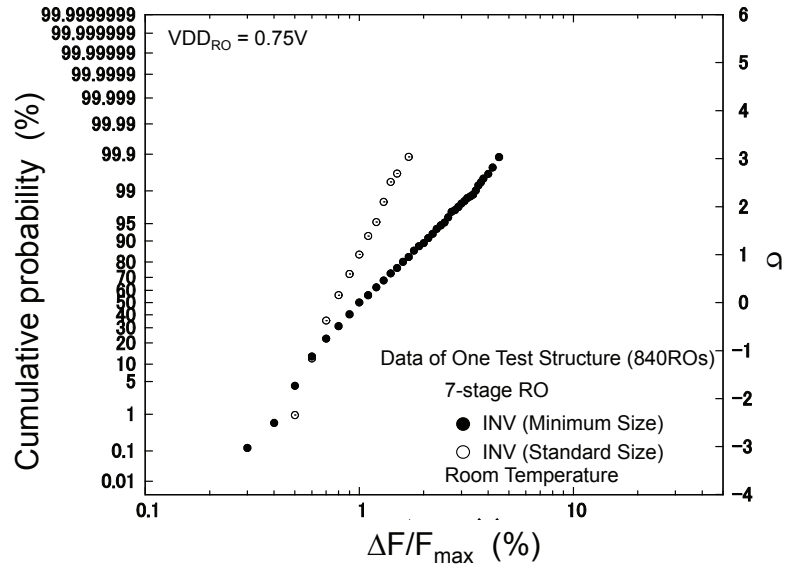
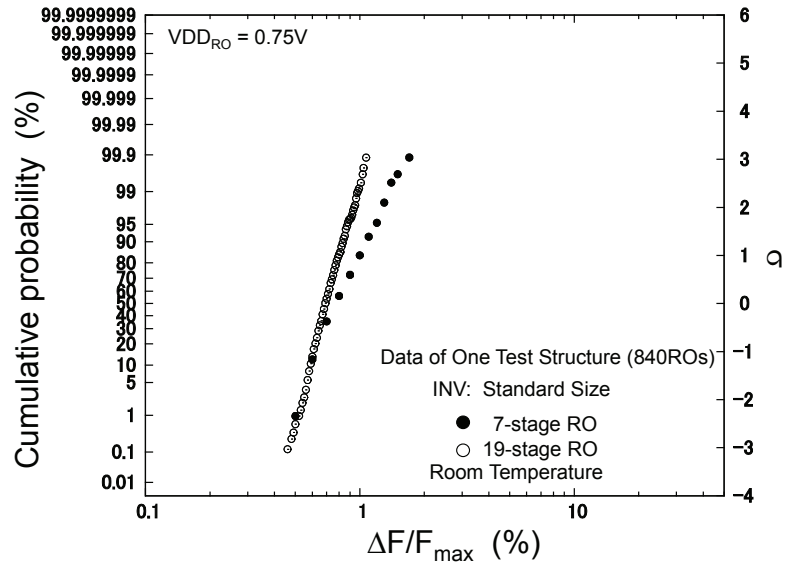


Figure 6.13: Cumulative probability of $\Delta F/F_{\max}$ for various VDD_{RO} which follows log-normal distribution.

Figure 6.14: The impact of gate area on $\Delta F/F_{\max}$.Figure 6.15: The impact of number of stages on $\Delta F/F_{\max}$.

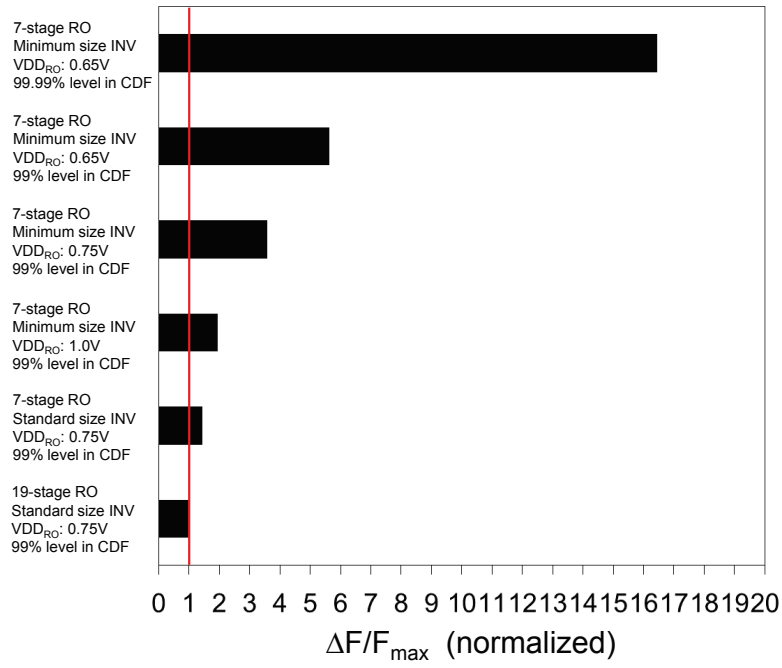


Figure 6.16: The impact of supply voltage, gate area, and stage number on $\Delta F/F_{\max}$ (normalized).

6.4 Impact of Body-Bias Technique on RTN-induced CMOS Logic Delay Fluctuation

An adaptive substrate bias control has been widely used to compensate for die-to-die parameter variations[132]. However, the impact of the substrate bias on RTN at the circuit level has not been well understood. It is already described in Section 5.1 (Fig. 5.7) that the RTN time constant can be affected by the substrate bias. Figure 6.17 shows the measurement results of frequency fluctuation of one RO for 60 s under three substrate bias conditions. For this sample, the time constant is modulated considerably only when the pMOS substrate bias is changed from 0V to +0.2V (middlemost figure). Then PSD for the same sample of Fig. 6.17 for five substrate bias conditions are calculated (Fig. 6.18). When the pMOS substrate bias is changed from 0V to +0.2V (c, e), the large two-state fluctuation rarely happens ($\tau_c \gg \tau_e$). Observed results are the effect of one trap at the pMOS transistor in the RO that induces large noise at the circuit level (a, b, d). Figure 6.19 shows the frequency fluctuation of RO location (section No.) 1 for three substrate bias conditions. Four-state fluctuation due to two traps is

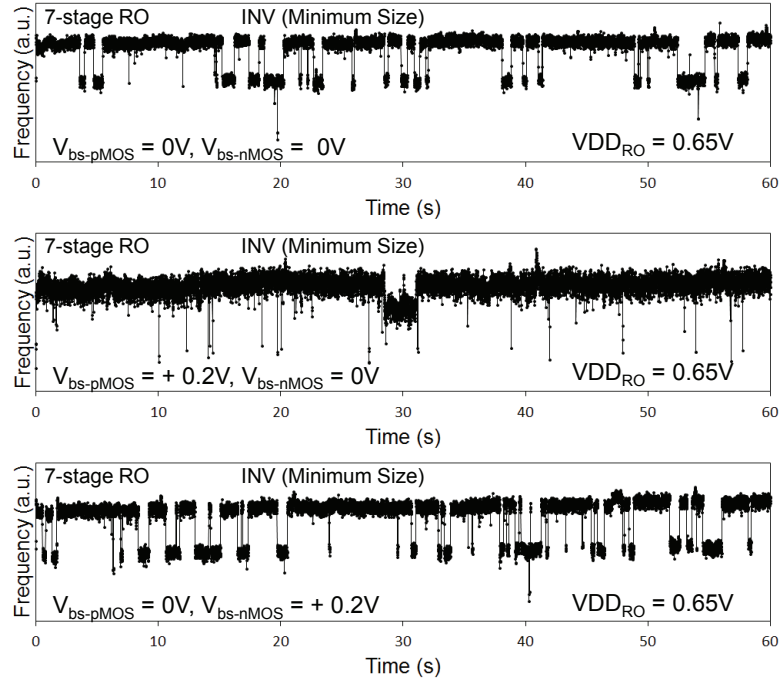


Figure 6.17: RTN-induced RO frequency fluctuation for three substrate bias conditions.

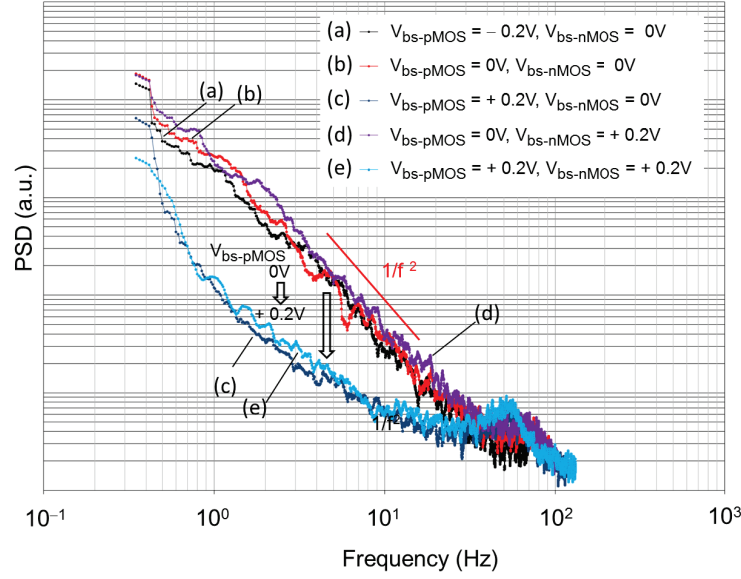


Figure 6.18: PSD of RTN-induced RO frequency fluctuation for five substrate bias conditions.

clearly observed for the zero substrate bias ($V_{bs-pMOS} = 0$ V, $V_{bs-nMOS} = 0$ V) case. The effect of one of two traps disappears only when nMOS transistor is forward biased by 0.2 V (middlemost figure). The disappeared two-state fluctuation is caused by a single trap in a specific nMOS transistor in the RO.

Finally, the statistical result of the impact of RTN on logic delay fluctuation is described. Substrate bias conditions are categorized as the reverse bias case ($V_{bs-pMOS} = -0.2$ V, $V_{bs-nMOS} = 0$ V), zero bias case ($V_{bs-pMOS} = 0$ V, $V_{bs-nMOS} = 0$ V), and forward bias case ($V_{bs-pMOS} = +0.2$ V, $V_{bs-nMOS} = +0.2$ V). To evaluate the forward body-bias effect on large $\Delta F/F_{max}$ samples, ROs that have more than 4% fluctuation at the reverse bias case (28 ROs) are shown in Fig. 6.20. When the substrate bias is changed from the reverse bias to the forward bias, $\Delta F/F_{max}$ tends to decrease monotonically due to F_{max} increase. However, it does not decrease monotonically in the case of the RO location “68”, “160” and “219” when substrate bias is changed from the reverse bias case to the forward bias case. It is because RTN time constants in these three ROs are strongly influenced by the substrate bias. Next, $\Delta F/F_{max}$ for one test structure under three substrate bias conditions is plotted in log-normal way (Fig. 6.21). The impact of RTN-induced delay fluctuation can be statistically reduced by the forward substrate bias control.

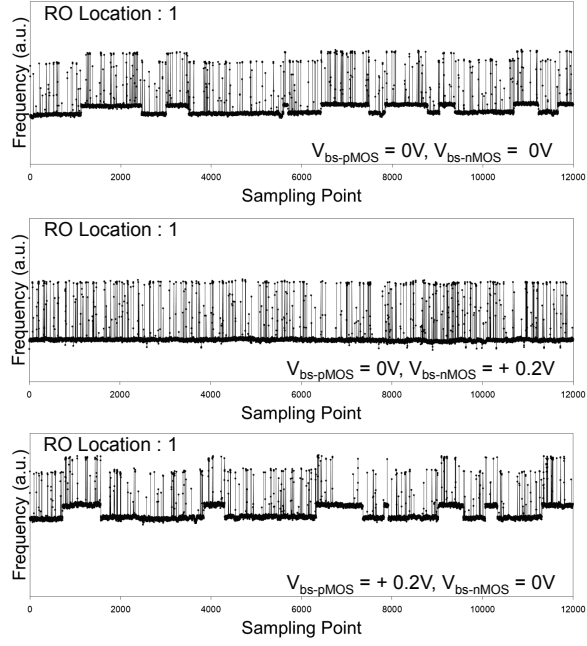


Figure 6.19: RTN-induced RO frequency fluctuation for three substrate bias conditions (RO Location 1).

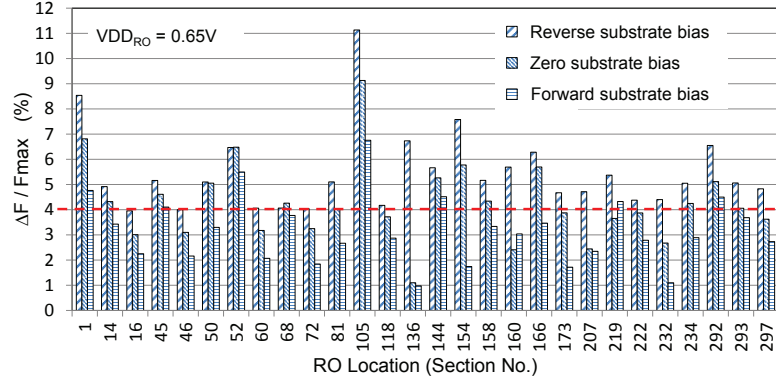


Figure 6.20: $\Delta F/F_{\max}$ of different ROs for three substrate bias conditions. RO that have more than 4% fluctuation at reverse substrate bias case are shown.

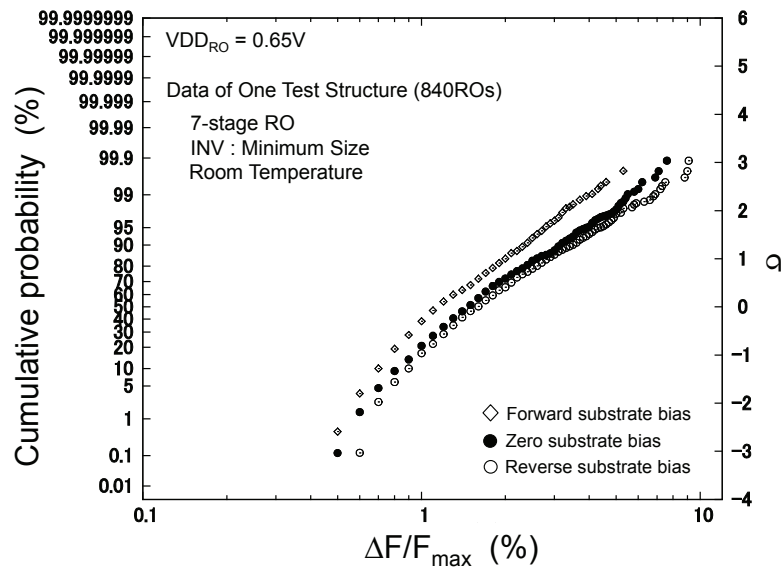


Figure 6.21: Log-normal distribution plot of $\Delta F/F_{\max}$ for one test structure under three substrate bias conditions.

6.5 Impact of RTN-induced Delay Fluctuation with respect to Process Variation

In a circuit that contains a large number of small transistors, the impact of RTN-induced fluctuation is considered to increase when it is compared with the frequency variation caused by manufacturing process. Figure 6.22 shows $\Delta F/F_{\max}$ versus $F_{\max}$ plot over 12,600 ROs. It represents how RTN distribution correlates with process variation distribution. The triangle shape distribution suggests that there is no or weak correlation between RTN variation and process variation. Figure 6.23 can be obtained by plotting the vertical axis of Fig. 6.22 with log scale. The circle shape distribution suggests that there is no or weak correlation between RTN variation and process variation. Figure 6.24 shows the impact of RTN when it is compared with that of process variation. The impact of RTN on process variation is defined as

$$\frac{(\Delta F/F_{\max})_{n\sigma}}{(n\sigma/\mu)}. \quad (6.1)$$

The plot for the minimum size 7-stage RO at 0.65 V ($\times$) can be obtained as follows. $\Delta F/F_{\max}$ follows log-normal distribution as already shown in Fig. 6.12.

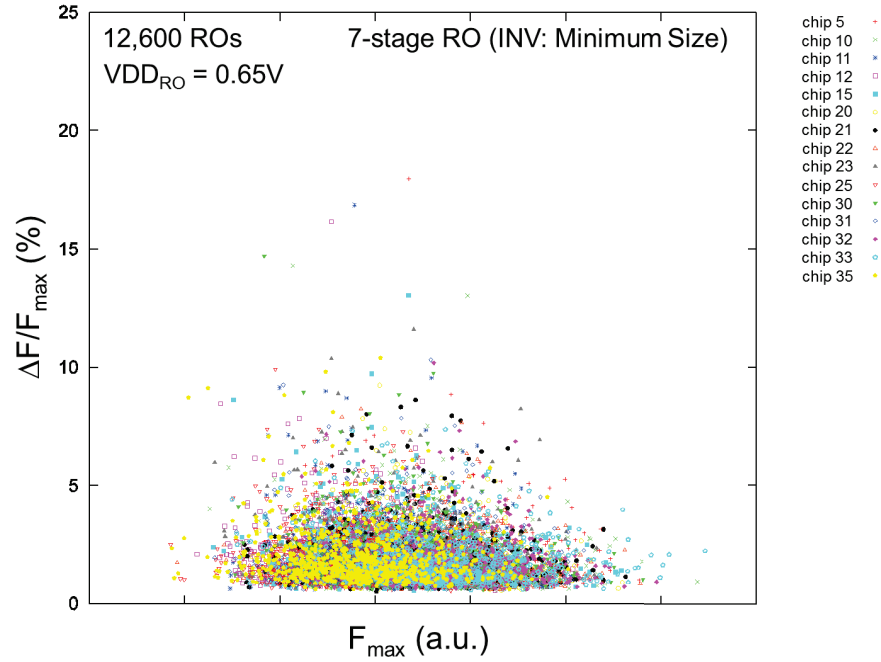


Figure 6.22: $\Delta F/F_{\max}$ versus $F_{\max}$ plot over 12,600 ROs.

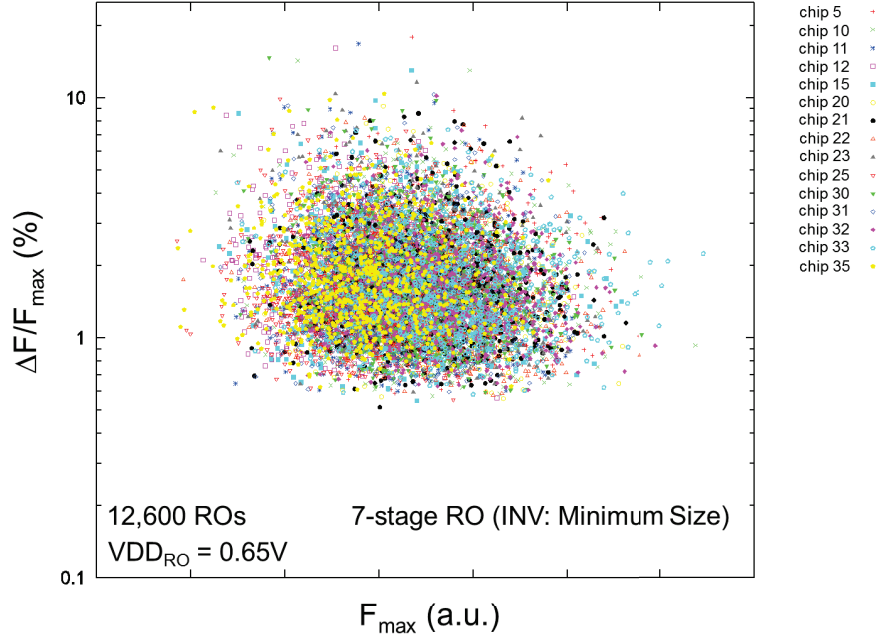


Figure 6.23: $\Delta F/F_{\max}$ versus $F_{\max}$ plot over 12,600 ROs (vertical axis: log-scale).

$(\Delta F/F_{\max})_{n\sigma}$ can be obtained for each σ using the log-normal distribution. $F_{\max}$ follows normal distribution as already shown in Fig. 6.10. $(n\sigma/\mu)$ can be obtained for each σ using the normal distribution. The dotted line is estimated from measured distributions of both RTN and process variation. For the minimum size 7-stage RO at 0.65 V ($\times$), the impact grows exponentially when σ is increased. Around 7σ value, RTN becomes comparable to process variation. When the operating voltage is slightly increased to 0.75 V ($\triangle, \circ$), the RTN impact decreases rapidly. As the transistor size is increased from minimum to standard size, RTN has almost no impact on process variation. The impact of RTN on process variation with respect to combinational circuit performance is for the first time estimated to increase exponentially by experimental data.

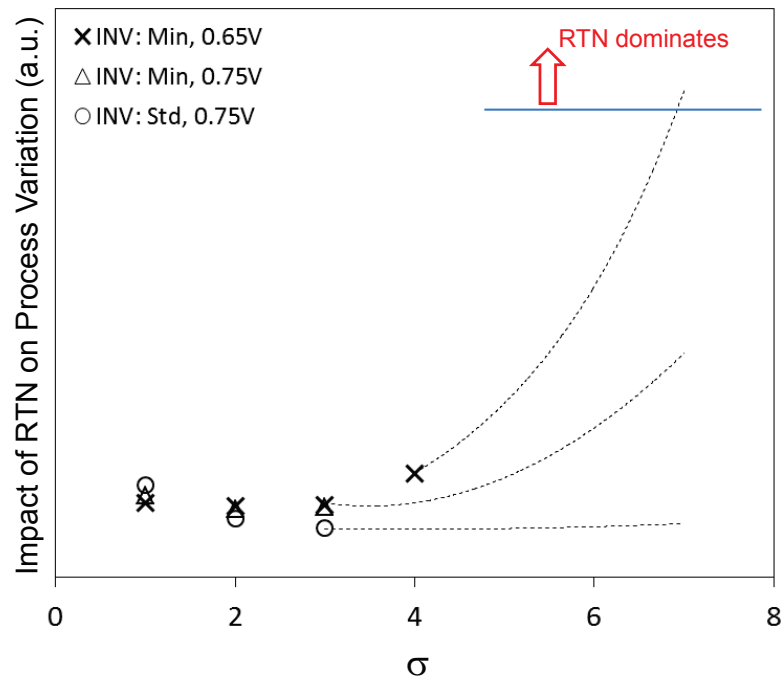


Figure 6.24: The impact of RTN on process variation.

6.6 Chapter Summary

The impact of RTN on CMOS logic circuit reliability is described based on our measurement results from 40 nm test chips. Even for a combinational circuit, its operation under a low supply voltage is for the first time found to be affected seriously by RTN. Statistical nature of RTN-induced delay fluctuation is described by measuring 12,600 ROs fabricated in a commercial 40 nm CMOS technology. RTN-induced delay fluctuation denoted by $\Delta F/F_{\max}$ becomes as much as 16.8% of the nominal oscillation frequency under low supply voltage (0.65V) operation. By increasing the transistor size from the minimum to the standard size, more than 50% reduction of $\Delta F/F_{\max}$ can be achieved at 95% level in cumulative probability under 0.75V operation. RTN-induced delay fluctuation also decreases rapidly with increasing the supply voltage. The impact of RTN-induced delay fluctuation can be statistically reduced by the forward substrate bias control. From measurement results, $\Delta F/F_{\max}$ increases log-normally when the number of logic circuits increases. RTN-induced delay fluctuation of a combinational circuit is for the first time estimated to be growing exponentially when it is compared with delay variation due to process variation. For the minimum size 7-stage RO at 0.65 V, the impact grows exponentially when σ in the cumulative probability is increased. Around 7σ value, RTN is estimated to be comparable to process variation. Measurement data suggests that there is no or weak correlation between RTN variation and process variation. The impact of RTN can be a serious problem even for logic circuits when they are densely integrated and operated under low supply voltage. But choosing proper circuit parameters can reduce the impact.

Chapter 7

Conclusion

This thesis describes the impact of NBTI and RTN on CMOS logic circuits based on the measurement results from 65 nm and 40 nm test chips. The contribution of this thesis is as follows. It is divided into two topics corresponding to NBTI and RTN.

Although MSM method is known to suffer from NBTI recovery during NBTI degradation characterization, results in this thesis are obtained with a comparably short measurement delay when it is compared with other papers. Measurement results of MSM method with $1\mu\text{s}$ delay show about 20% recovery at $t = 2\mu\text{s}$ recovery time. Measurement results do not show the tendency to saturate even at $t = 1\mu\text{s}$ recovery time. Recovery within $1\mu\text{s}$ recovery time is considered to affect a usual digital circuit performance degradation that has MHz to GHz operation frequency. When the recovery shows the tendency to saturate remains to be a future issue to be solved. By the MSM method, NBTI recoveries under various recovery conditions are found to follow one simple recovery curve. More than 80% of NBTI degradation is found to recover in a few hours under zero gate bias condition. The weak dependence of the recovery on degradation level helps recovery modeling much simpler. How to include observed recovery results into a circuit simulation model is remained to be a future work. NBTI degradation during recovery characterization by the MSM method can be avoided if the gate bias is set to 0 V during recovery measurement. The LC method that has the highest fidelity to NBTI recovery measurement is developed in this thesis. An NBTI recovery sensor with a 400 ns measurement delay based on LC method is proposed. It is shown that NBTI recovery follows $\log t$ from 400 ns to 3000 s. It is confirmed for the first time in the region of $400\text{ ns} \leq t_{\text{recovery}} \leq 30\text{ ms}$. By degrading and recovering thousands of pMOS transistors at the same time, we can observe that the time constants of positively charged defects, which are related to NBTI, are log-uniformly distributed in the pMOS devices.

Making the most of NBTI recovery, the concept of a multicore LSI lifetime extension method is proposed. Measurement results show that the recoverable component measured using the off-leak current remains almost constant after repeatedly adding NBTI stress. It is also shown that the amount of NBTI recovery can be tuned by the relaxation time in a real application. Combined with NBTI recovery, circuit parallelization plays an important role for the lifetime extension. As a result, multicore LSI lifetime extension can be achieved. For the first time, transforming silicon area into LSI lifetime is shown to be a promising and realistic concept for the ever-shrinking CMOS technology.

As for RTN, recent researches on RTN and its impact on circuits are briefly summarized. The impact of RTN on CMOS logic circuit reliability is described based on our results from 65 nm and 40 nm test chips. From the drain current RTN measurements in 65 nm chip, RTN-induced logic delay fluctuation can be strongly influenced by both the gate bias and the substrate bias. Even for a combinational circuit, its operation under a low supply voltage is for the first time found to be affected seriously by RTN. Statistical nature of RTN-induced delay fluctuation is described by measuring 12,600 ROs fabricated in a commercial 40 nm CMOS technology. RTN-induced delay fluctuation ($\Delta F/F_{\max}$) becomes as much as 16.8% of nominal oscillation frequency under 0.65 V operation. By increasing the transistor size from the minimum to the standard size, more than 50% reduction of $\Delta F/F_{\max}$ can be achieved at 95% level in cumulative probability under 0.75V operation. RTN-induced delay fluctuation also decreases rapidly with increasing the supply voltage. The impact of RTN-induced delay fluctuation can be statistically reduced by the forward substrate bias control. From measurement results, $\Delta F/F_{\max}$ increases log-normally when the number of logic circuits increases.

The impact of RTN can be a serious problem even for digital circuits when they are densely integrated and operated under a low supply voltage. The impact of RTN on process variation with respect to combinational circuit delay is for the first time estimated to grow exponentially by experimental data. Measurement data suggests that there is no or weak correlation between RTN variation and process variation. It is found that the impact of RTN fluctuation can be drastically reduced by slightly increasing supply voltage and gate area. Circuit designers can know how the impact of RTN on a combinational circuit can be decreased by tuning their design parameters.

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3. **T. Matsumoto**, H. Makino, K. Kobayashi, H. Onodera, "Multi-core LSI lifetime extension by negative-bias-temperature-instability recovery-based self-healing," *Japanese Journal of Applied Physics (JJAP)*, vol. 51. (2012) p. 04DE02
4. **T. Matsumoto**, H. Makino, K. Kobayashi, H. Onodera, "A 65 nm complementary metal-oxide-semiconductor 400 ns measurement delay negative-bias-temperature-instability (NBTI) recovery sensor with minimum assist circuit," *Japanese Journal of Applied Physics (JJAP)*, vol. 50. (2011) p. 04DE06

Invited Paper

1. **T. Matsumoto**, K. Kobayashi, H. Onodera, "Impact of random telegraph noise on CMOS circuit reliability," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2014.
2. **Takashi Matsumoto**, Kazutoshi Kobayashi, and Hidetoshi Onodera, "Impact of random telegraph noise on CMOS logic delay uncertainty under low voltage operation [IEDM]," IEEE Electron Devices Society Kansai Chapter, 13th Kansai Colloquium Electron Device Workshop, 2013.
3. **T. Matsumoto**, K. Kobayashi, and H. Onodera, "Impact of random telegraph noise on CMOS logic delay uncertainty under low voltage operation," *Japan Soc. App. Phys. Silicon Technology*, No. 154, pp. 27 - 30, 2013.

International Conference

1. (Invited) **T. Matsumoto**, K. Kobayashi, H. Onodera, "Impact of random telegraph noise on CMOS logic circuit reliability," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2014.
2. **T. Matsumoto**, K. Kobayashi, H. Onodera, "Impact of random telegraph noise on CMOS logic delay uncertainty," *ACM The TAU Workshop (TAU)* 2013, pp.35-40.
3. **T. Matsumoto**, K. Kobayashi, H. Onodera, "Impact of random telegraph noise on CMOS logic delay uncertainty under low voltage operation," *IEEE International Electron Devices Meeting (IEDM)* 2012, Session 25-6, pp.581-584.
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5. S. Nishimura, **T. Matsumoto**, K. Kobayashi, H. Onodera, "Impact on delay due to random telegraph noise under low voltage operation in logic circuits," *International Conference on Solid State Devices and Materials (SSDM)* 2012, Session PS-5-16, pp. 170-171.
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2. S. Nishimura, **T. Matsumoto**, K. Kobayashi, and H. Onodera, "Characterization of random telegraph noise using inhomogeneous ring oscillator," Technical Report of IEICE, 2014.
3. (Invited) **Takashi Matsumoto**, Kazutoshi Kobayashi, and Hidetoshi Onodera, "Impact of random telegraph noise on CMOS logic delay uncertainty under low voltage operation [IEDM]," IEEE Electron Devices Society Kansai Chapter, 13th Kansai Colloquium Electron Device Workshop, 2013.
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