

Binary-weighted Modular Multi-level Digital Active Gate Driver

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Abstract—This paper proposes a modular multi-level digital active gate driver topology consisting of several sub-modules with binary-weighted voltages. It can coordinate both the dynamic and the static behavior of SiC MOSFETs by shaping the gate voltage waveform using 15 voltage levels, which is particularly beneficial in parallel operation of the power devices. It is verified that the proposed gate driver can improve the current-sharing performance of parallel-connected SiC MOSFETs under several usually-undesired conditions with mismatched parameters.

I. INTRODUCTION

Active gate drive (AGD) has gained increasing attention for bringing out the maximum performance from SiC power MOSFETs [1], [2]. It is a technique to control the switching transient of the power devices by adding active mechanisms or components to the gate drive circuit. It has been shown by many research works that it can suppress the overshoots of device current and voltages while achieving fast switching, which decreases the risk of serious electromagnetic interference and malfunction of the device or the circuit operation. AGD is also promising for providing additional features to the gate drive circuit, such as device protection [1] and thermal management [3]. A number of AGD topologies have

been proposed so far, which can be roughly divided into three types: resistor-controlled AGDs [4], [5], voltage-controlled AGDs [6]–[8], and current-controlled AGDs [9], [10]. While AGD has shown benefits in driving a single power device, the technique is also, or particularly, promising for parallel operation of SiC MOSFETs [11].

It is well-understood that the mismatch of the device parameters and even the parasitic inductance among the parallel-connected power devices will lead to a disastrous imbalance of current-sharing performance [12], [13]. It can destroy the device immediately in extreme cases or, if not immediately, can also damage the device and the package in the long run, which will accelerate the imbalanced aging among the parallel-connected devices. A careful selection of SiC MOSFETs within a strict allowance of variations and the symmetrical placement of devices are required, leading to an increased design effort with limited flexibility. These challenges get even more difficult as more number of SiC MOSFETs are involved. It is expected that AGD will compensate for the mismatches instead, easing these restrictions. As the critical parameters are governed by gate-voltage characteristics, such as threshold voltage and on-resistance [12], the use of voltage-controlled multi-level AGD is considered suitable for a balanced operation of parallel-connected SiC MOSFETs [7], [14].

Three or four-level AGDs, which are the simplest configurations of multi-level AGDs, have been proposed in several research works [6], [7], [15]. One or two intermediate voltage levels are additionally supplied to slow down the switching momentary during the switching transient. As the effective gate voltage level depends on the operating conditions, especially the drain current, AGDs with small numbers of fixed voltage levels may not be enough for purposes requiring several different sequences. Another configuration of multi-level AGDs is to use modular topology, which has been proposed in several research works. In [4], a modular topology using

two additional sub-gate-drivers is reported to retrofit a 5-V current-controlled AGD into a 15-V SiC MOSFET gate driver. Modular multi-level topologies have also been studied, using 4-V SOI-CMOS-based integrated modules [16] or using 5-V discrete gate driver ICs [8]. However, the adjustable gate voltage levels are restricted within the 5-V range in [4] or limited to the multiplies of 4 in [16], which are not sufficient for the precise control of switching transient. In [8], the gate voltage is controlled between the multiplies of 5 by constantly switching the modules using 2.5-ns-resolution PWM, which can be challenging to generate and also be dangerous considering the risk of false-turn-on.

We have proposed another concept of multi-level AGD inspired by the digital-to-analog converter (DAC) architecture [17]. It offers a flexible shaping of gate voltage waveform using 15 levels generated by the switching of the binary-weighted resistors during the switching transient. It is demonstrated that the optimization of the digitally-expressed gate voltage waveform can be performed in a combinatorial optimization approach, such as genetic algorithm, which would eliminate the design effort by humans [18]. However, the voltage division using resistors generates non-negligible loss in the gate driver, making it inadequate for practical application.

In this work, we propose a modular multi-level digital AGD (MMDAGD) topology. Series connection of binary-weighted floating submodule voltages enables a DAC-like shaping of the gate voltage waveform, offering a flexible and straightforward control during the switching transient using multi-bit gate signal sequences. MMDAGD can also adjust the gate bias level during the steady state of switching to control the on-resistance of power devices, making it particularly suitable for applications in parallel-connection of SiC MOSFETs. The concept and design of MMDAGD are presented, and its operation is verified in the balancing of the current sharing of parallel-connected SiC MOSFETs.

II. DESIGN OF MODULAR MULTI-LEVEL DIGITAL ACTIVE GATE DRIVER

This section describes the concept and the operation of MMDAGD, which is a mix of the modular multi-level topology and the DAC architecture.

A. Concept and operation

Fig. 1 (a) shows the overall schematic configuration of 4-bit MMDAGD. It consists of four submodules (SM_i , $i = \{0, 1, 2, 3\}$), which mainly consist of a half-bridge circuit with a submodule capacitor (C_{SM_i}). A binary-weighted submodule voltage of $V_{SM_i} = 2^i E$ [V] is stored

in each submodule capacitor. The output of SM_i is shorted when the input signal (b_i) is 0, and is connected to C_{SM_i} when b_i is 1. Hence, the output voltage of MMDAGD, or V_{GS} , is expressed as the sum of the output voltages of submodules as given by (1).

$$V_{GS} = \sum_{i=0}^3 b_i V_{SM_i} = \sum_{i=0}^3 2^i b_i E \quad (1)$$

V_{GS} waveform is shaped by switching these submodules successively during the switching transient. Fig. 1 (b) shows an example of turn-on V_{GS} waveform generated by 4-bit MMDAGD, and Fig. 1 (c) describes the transition of submodules. Note that the gate signal is expressed as $b_3 b_2 b_1 b_0$ and in hexadecimal numbers, where b_3 is MSB (SM_3) and b_0 is LSB (SM_0). During the off state, the gate signal is 0, which means that all the submodules are off. When the gate signal turns 0xA (1010), SM_1 and SM_3 are turned on, which gives the total voltage of $10E$ at the output. Lastly, the gate signal is changed to 0xE, yielding $14E$ at V_{GS} . In this manner, the time-series sequence of gate signals is converted into the 15-level V_{GS} waveform, just as is done in DAC. The time constant of these transitions is determined by the external gate resistor R_G .

The number of available voltage levels is determined by the number of bits (n) as $2^n - 1$ levels. Increasing the number of bits would improve the controllability but adds to the design complexity, especially the generation of V_{SM} . A 4-bit configuration is selected in the prototype to simplify the design while achieving enough controllability of 15 voltage levels. The time resolution of V_{GS} -waveform shaping is governed by the clock rate of the controller. The use of FPGA is supposed, as it can achieve a clock rate of hundreds of MHz for multiple synchronized signal lines, and can also easily expand the original gate signal into a multi-bit signal sequence by developing a HDL module.

Another important feature of MMDAGD is that it can control $V_{GS,on}$, which is a V_{GS} level applied during the MOSFET is in on-state, by changing the gate signal given during the period (b_{on}) as shown in Fig. 1 (b). It is known that on-resistance (R_{on}) of SiC MOSFETs can be controlled by $V_{GS,on}$. If several devices with different values of R_{on} are connected in parallel, the static-current distribution can be balanced by adjusting b_{on} .

It is noted that Fig. 1 (b) is a simple example of feasible V_{GS} waveform; the number of voltage steps during turn-on is not limited to 1 or 2 but can be expanded to more. There is a physical limitation for the number of steps due to the response speed of each submodule,

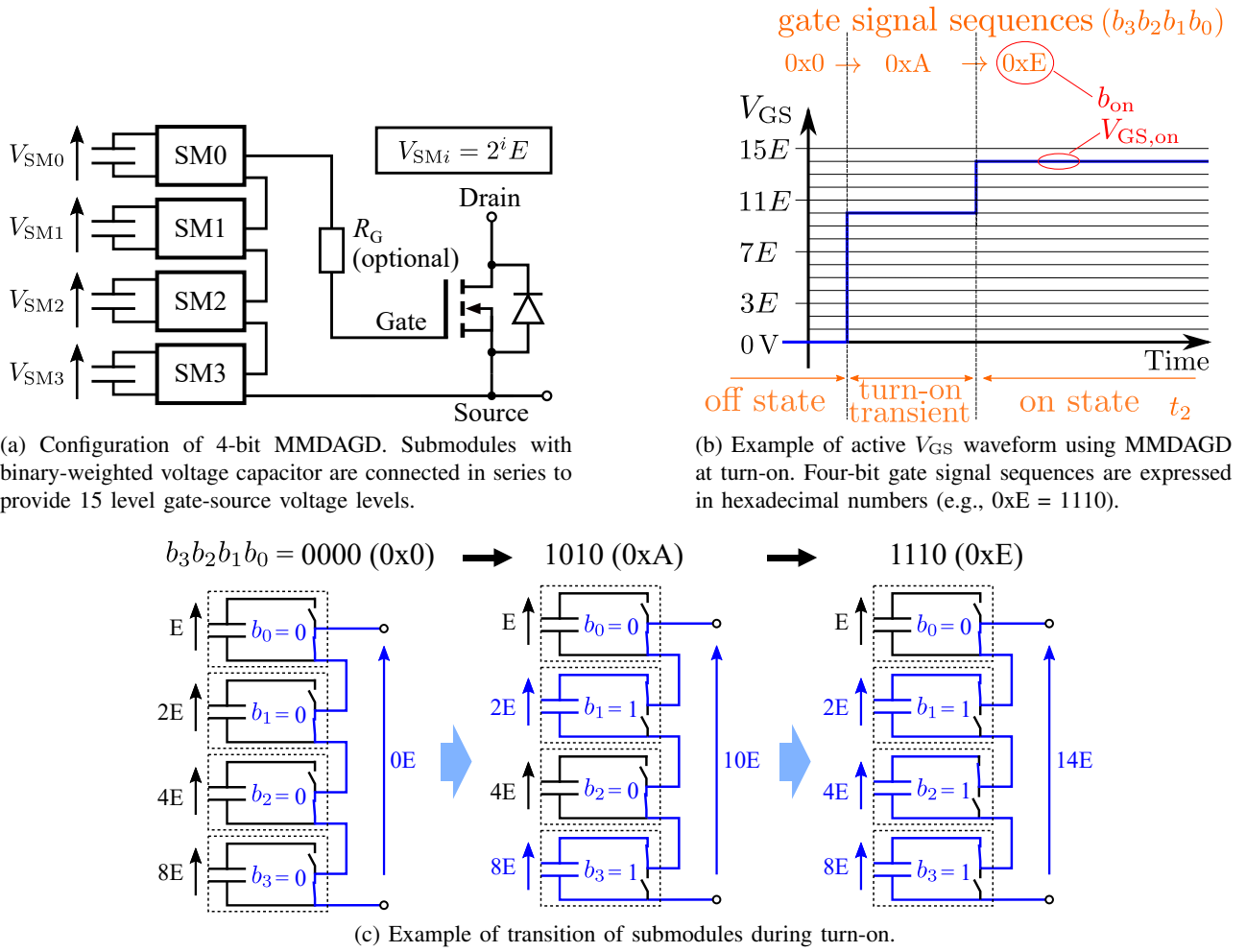


Fig. 1: Concept and operation of 4-bit MMDAGD.

which is around 15-20 ns, and also the complexity of controlling the waveform.

B. Submodule configuration

Fig. 2 (a) shows the schematic configuration of a submodule (SM_i), where GND_i indicates the reference ground of the submodule. Its output stage is composed of a half-bridge circuit of n-type Si MOSFETs. They are driven by the input signal b_i , which is transferred through digital isolators with 5 V output. The output of the low-side isolator is powered by V_{DDL} , which is referenced from GND_i , while that of high-side isolators is powered by V_{DDH} , which is generated from V_{DDL} using another 5 V-to-5 V type isolated DC-DC converter. The deadtime between the high-side and low-side signals are determined to be 5 ns, which is generated externally.

The half-bridge circuit is connected to the submodule capacitor C_{SMi} with V_{SMi} generation circuit. As each submodule needs to be floating from others considering

the operating principle, each V_{SMi} is supplied using an isolated DC-DC converter. In the prototype configuration shown in this paper, the submodule voltages are set as $V_{SM0} = 1.25$ V, $V_{SM1} = 2.25$ V, $V_{SM2} = 4.5$ V, and $V_{SM3} = 9.0$ V, respectively, which gives the maximum V_{GS} value of 17 V. For SM0, SM1, and SM2, V_{SMi} is generated using 5 V output DC-DC converter, which is then regulated using low-drop-out (LDO) regulator, as shown in Fig. 2 (b). The 5 V is also supplied as V_{DDL} . For SM3, V_{SM3} is taken directly from the 9 V-output of the DC-DC converter as shown in Fig. 2 (c). A LDO regulator is also utilized to obtain V_{DDL} .

It should be noted that V_{SM} can be as small as 1 V or less to achieve precise adjustment of V_{GS} . In such a case, the use of p+n type complementary MOSFETs with shared gate signal is not beneficial; the gate signal line cannot be shared because, assuming the gate signal swing is from 0 to 5 V, the gate-source voltage of the p-type MOSFET would swing between -1 and 4 V, which

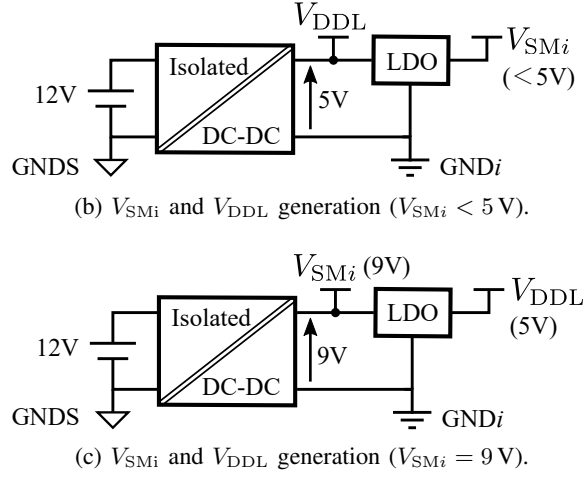
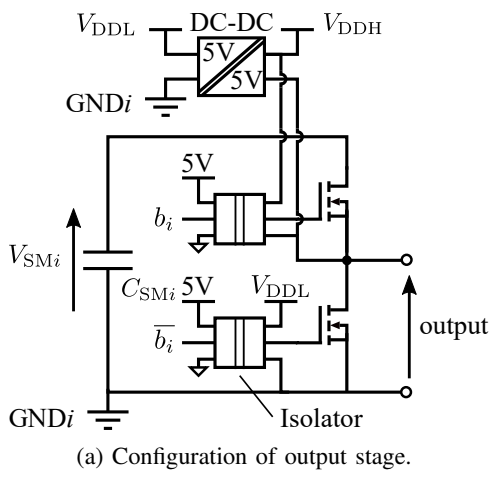


Fig. 2: Schematic configuration of submodules (SMi).

is not sufficient for its operation. It is also not possible to use commercial gate driver ICs as submodules because the under-voltage lock-out feature prevents the operation at low V_{SMi} . These are the reasons to use n-type dual MOSFETs as the half-bridge with two isolated gate signals. Works are ongoing to simplify the configuration of the output stage.

C. Comparison with existing topologies

The major difference between MMDAGD and the modular AGDs proposed in the literature [8], [16] is that every submodule has a different value of submodule voltage. This feature enables the DAC-like operation featuring readily-available 15 V_{GS} levels, adding to the flexibility of the V_{GS} shaping. The expansion of the configuration is also possible by re-configuring the submodule voltages or adding another. Particularly, adding a negative-bias submodule will be useful for applications in need of cross-talk suppression [19].

D. Fabricated MMDAGD

Fig. 3 shows the prototype of 4-bit MMDAGD, which is designed using discrete components and fabricated on a four-layer printed circuit board with the size of around $8\text{ cm} \times 8\text{ cm}$. The list of main components used in the prototype is provided in Table I. As recognized in Fig. 3, the half-bridge MOSFETs and submodule capacitors are placed compactly, while signal isolators and DC-DC converters take up much of the space of the PCB surface. It is expected that most of the components will be integrated into a chip eventually.

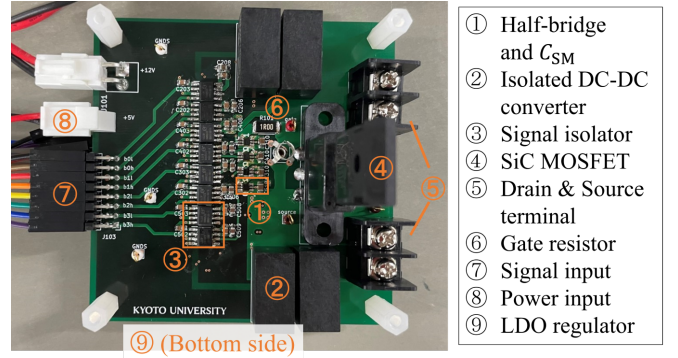


Fig. 3: Photograph of prototype MMDAGD.

III. CURRENT-BALANCING OF PARALLEL-CONNECTED SiC MOSFETs

The operation and effectiveness of MMDAGD is experimentally verified in the current balancing of parallel-connected SiC MOSFETs, focusing on the switching behavior at the turn-on. Fig. 4 shows the schematic diagram of the test circuit. A standard double-pulse switching testing circuit is adopted with clamped inductive load consisting of a SiC Schottky-barrier diode (SCS206AM, ROHM Co., Ltd.) and an inductor of $300\mu\text{H}$. Two SiC MOSFETs (device-under-test: DUT) are connected in parallel (DUT1 and DUT2), each of which is driven by MMDAGD. The gate signal sequences for each MMDAGD are generated by an FPGA (Zynq UltraScale+ MPSoCs, Xilinx), whose clock rate of the output signals is set at 200 MHz. The operating condition is set at 240 V and 6 A, which is split to 3 A for each DUT in an ideal operation. Fig. 5 shows the photograph of the test setup. The difference in wire length between DUT1

TABLE I: List of main components utilized in the prototype of MMDAGD.

Model	Description	Notes
US6K2TR	Dual n-type Si MOSFET	output stage of half-bridge
Si8610BB	Digital isolator	gate signal isolation
CRE1S0505MC	Isolated DC-DC converter, 5 V to 5 V	power supply for high-side isolators
MEJ2S1209SC	Isolated DC-DC converter, 12 V to 9 V	power supply for SM ₃
MEJ2S1205SC	Isolated DC-DC converter, 12 V to 5 V	power supply for SM ₀ , SM ₁ , SM ₂
NCV317MBDTRKG	LDO regulator	adjustable output: 1.2 V to 37 V
Capacitor	10 μ F MLCC	submodule capacitor
Resistor	1.0 Ω chip resistor	external gate resistor

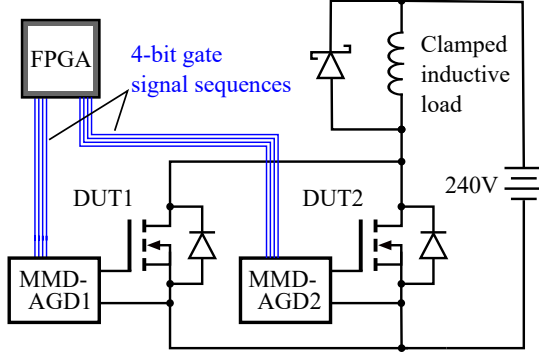


Fig. 4: Schematic diagram of double-pulse switching test circuit with two parallel-connected SiC MOSFETs.

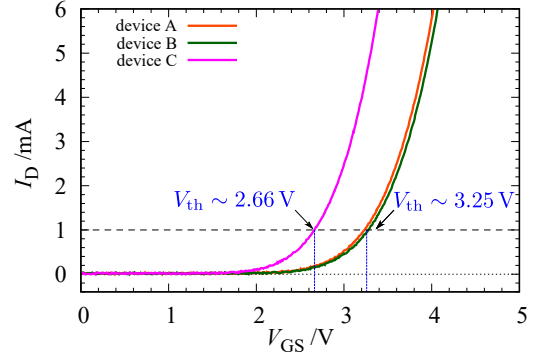


Fig. 6: I_D - V_{GS} characteristics and V_{th} (at $I_D = 1$ mA) of selected DUTs measured at $V_{DS} = 10$ V.

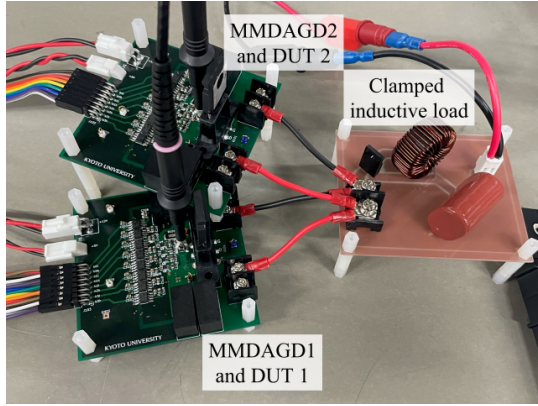


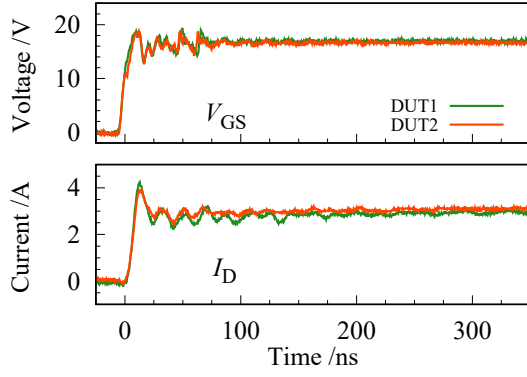
Fig. 5: Photograph of test circuit.

and DUT2 is as minimized as possible to exclude the influence of layout difference on the switching behavior of the two DUTs. The drain current (I_D) and V_{GS} of the two DUTs are measured using current probes and voltage probes (TCP0020 and TPP0200, Tektronix, Inc.), and the waveform is acquired in an oscilloscope (MDO4104, Tektronix, Inc.).

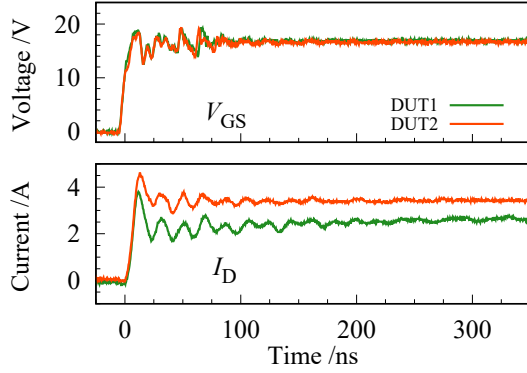
A. Selection of DUTs with parameter variations

We selected three DUTs based on the measurements of I_D - V_{GS} characteristics using a curve tracer (CS-3000 series, IWATSU Co., Ltd.). Fig. 6 shows the measured I_D - V_{GS} curves and V_{th} of the three DUTs. Devices A and B have almost the same characteristics of $V_{th} \sim 3.25$ V, while device C has clearly different characteristics of $V_{th} \sim 2.66$ V. Such differences in the device characteristics are often found in commercial SiC power MOSFETs due to the process variation [20]. We prepare two cases, one with matched devices and one with unmatched; devices A and B are adopted as DUT1 and DUT2 in case 1, while devices A and C are adopted in case 2.

The influence of these difference on the parallel operation is investigated. Fig. 7 shows the turn-on switching waveforms in each case without AGD operation, where the gate signal is changed from 0000 to 1111. From Fig. 7 (a), it is found that I_D is equally balanced both dynamically and statically in parallel operation of matched devices. On the other hand, in Fig. 7 (b), DUT2 turns on faster than DUT1, leading to the dynamic



(a) case 1 (DUT1: device A, DUT2: device B).



(b) case 2 (DUT1: device A, DUT2: device C).

Fig. 7: Turn-on switching waveforms without AGD.

TABLE II: List of adopted gate signal sequences.

name	gate signal sequence (in hex.)
w/o AGD	0x0 $\rightarrow$ 0xF
AGD i	0x0 $\rightarrow$ 0xA (40 ns) $\rightarrow$ 0xF
AGD ii	0x0 $\rightarrow$ 0xB (40 ns) $\rightarrow$ 0xF
AGD iii	0x0 $\rightarrow$ 0xA (40 ns) $\rightarrow$ 0xD
AGD iv	0x0 $\rightarrow$ 0xA (35 ns) $\rightarrow$ 0xF

imbalance. It is also shown that the static current is not shared equally due to the difference in R_{on} .

B. Balancing current-sharing using AGD

We now activate the AGD operation to improve the current-sharing performance and also to suppress the overshoot of I_D . The AGD sequences are searched manually via try-and-error in this work, and the list of adopted sequences is given in Table II.

1) *Parallel connection of matched devices:* Firstly, the AGD is applied to case 1. Fig. 8 show the switching waveforms of two DUTs, which are driven using the same AGD sequence (AGD i). The switching waveforms

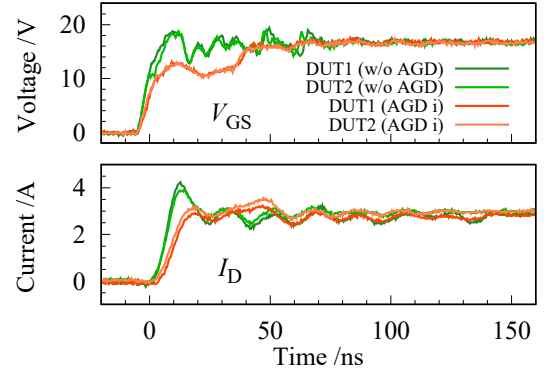


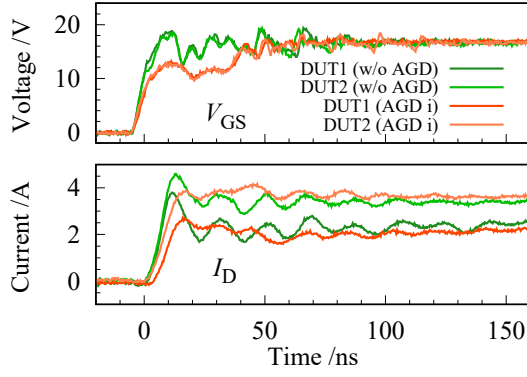
Fig. 8: Turn-on switching waveforms in case 1 with AGD (orange) and without AGD (green).

without AGD are also shown for reference. The I_D waveforms of two devices are consistent under the AGD operation and the overshoot is decreased. Therefore, for parallel operation of matched devices, the overshoot can be suppressed by adopting the same AGD sequence without interfering with the originally-balanced current-sharing.

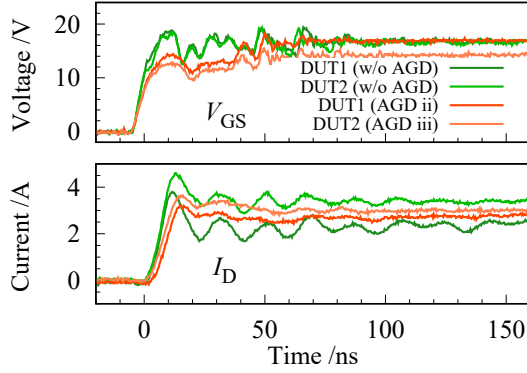
2) *Parallel connection of unmatched devices:* Secondly, the AGD is applied to case 2. Fig. 9 (a) shows the switching waveforms when the same AGD sequence (AGD i) is applied to both devices. Although the overshoot is suppressed slightly, the dynamic and static imbalance still remains. Consequently, the AGD sequence is adjusted individually to mitigate these differences. Fig. 9 (b) shows the switching waveforms using adjusted AGD sequences, which have 1-bit difference during the transient and 2-bit difference during the steady state. It is confirmed that the current-sharing performance is improved both dynamically and statically, with static current difference decreased from 1 A to 0.2 A.

C. Parallel connection with unmatched layout

Lastly, we investigate a scenario with an unmatched layout. The pair of case 1 is adopted, but the length of both wires between the DUT2 and the test circuit is doubled. Fig. 10 (a) shows the switching waveform without AGD and with AGD i, which was effective in case 1 (Fig. 8). The I_D waveforms now do not overlap each other without AGD, and the application of the same AGD sequence does not help the imbalance to decrease. Accordingly, the AGD sequence is individually adjusted as shown in Fig. 10 (b), and the current-sharing performance is improved. These results confirmed that the AGD sequence to balance the current-sharing needs to consider not only the differences in device characteristics but also those of the circuit layout.

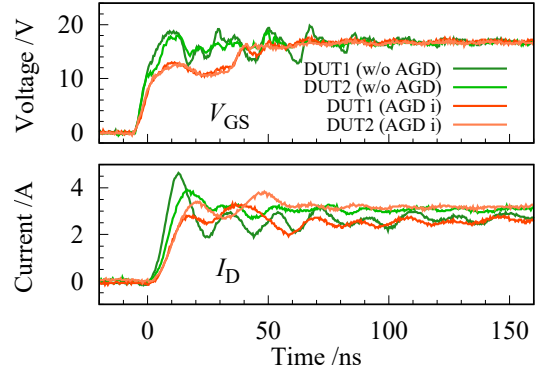


(a) Same AGD sequence is applied.

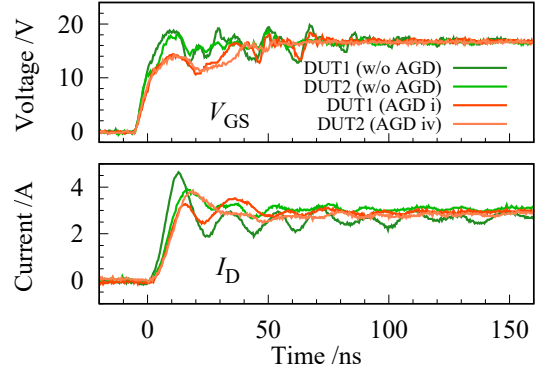


(b) Individually-adjusted AGD sequence is applied.

Fig. 9: Turn-on switching waveforms in case 2 with AGD (orange) and without AGD (green).



(a) Same AGD sequence is applied.



(b) Individually-adjusted AGD sequence is applied.

Fig. 10: Turn-on switching waveforms in case 1 with different wire lengths.

IV. CONCLUSION

This paper presented the design and the operation of the modular multi-level digital active gate driver, which consists of series-connected submodules with binary-weighted floating voltages. The gate voltage is expressed as the sum of the outputs of switched submodules. This structure enables the DAC-like direct and flexible shaping of V_{GS} waveform for SiC MOSFETs to control both the dynamic and the static behavior of switching operation. Taking benefit of these features, MMDAGD is applied to the balancing of current-sharing in parallel-connected SiC MOSFETs. The prototype of 4-bit MMDAGD is fabricated using discrete components, and its operation is confirmed. It is verified that MMDAGD can simultaneously balance the device current both dynamically and statically, while suppressing the current overshoots. The experiment was performed in several different scenarios where the difference in the device characteristics or the circuit layout exists. It is shown that the imbalance can be mitigated by adopting a unique V_{GS} waveform for each device.

These imbalances are attributed mainly to the variations in device parameters, which could exist inherently from the process level or could appear a posteriori due to the aging of the device. Detecting these changes and adjusting the AGD operation would be the essential techniques to fulfill the potential of AGDs. By adopting MMDAGD, the current balancing of parallel-connected SiC MOSFETs could be solved as a combinatorial optimization problem of the gate signal sequences, making it easier to deal with these changes computationally. This would eliminate the necessity for the intrinsically heuristic parameter-tuning of the hardware design of the gate driver itself or the circuit layout. The difficulty in parallel-connecting multiple SiC MOSFETs would be eased upon the development of a proper algorithm for adjusting the AGD sequence for each parallel-connected device. The authors will continue to improve the circuit configuration aiming at the integration and explore the potential of building-block style digital AGDs.

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