

Switching Trajectory Control of SiC MOSFET Based on I–V Characteristics Using Digital Active Gate Driver

Hajime Takayama*, Shuhei Fukunaga, and Takashi Hikiyama

Department of Electrical Engineering, Kyoto University,
Nishikyo, Kyoto 6158510, Japan.

*Email: h-takayama@dove.kuee.kyoto-u.ac.jp

Abstract— In this work, we investigate a control strategy for the digital active gate drive of silicon carbide (SiC) MOSFETs to select the crucial gate signal for improving the switching characteristics. The strategy is developed on the state space of the SiC MOSFET, utilizing its current–voltage characteristics obtained from a device model. The proposed gate driver and the strategy are verified for both turn-on and turn-off operation in a double-pulse testing. Experimental results confirm that the overshoot and ringing of the drain current and drain–source voltage is successively suppressed in wide operating conditions by selecting appropriate gate signal sequences.

Index Terms—device model, digital active gate drive, GaN HEMT, SiC MOSFET, switching trajectory

I. INTRODUCTION

Wide-bandgap (WBG) semiconductor power devices, such as SiC MOSFETs and GaN HEMTs, are highly expected to open the door for high-frequency, integrated power circuits [1]–[3]. Recent advancements of SiC MOSFETs have already seen many industrial applications, including electric vehicles and railway tractions [4]. Normally-off gallium nitride (GaN) power devices have also become available recently, enhancing their application especially in high-frequency and relatively low-power converters [5]. Their fast-switching capability, however, increases the ringing and the overshoots of device current and voltage, which can lead to the device breakdown or serious electromagnetic interference (EMI) [6]–[8]. Not only they lower the reliability of the device and the system [7], their presence forces us to select power devices with higher voltage and current ratings than the actual operating conditions for safety concern, which can greatly sacrifice the potential of the material [4]. For these reasons, the suppression of the overshoots and ringing is a crucial problem for the application of WBG power devices.

To achieve a good balance between the EMI and the switching loss without sacrificing the fast switching-speed, active gate drive (AGD) has been gathering attention [8]–[19]. The fundamental idea of this technique is to control the switching speed of the device actively during the switching transient, either by variable gate resistance methods [8]–[10], variable gate voltage methods [11]–[15], or variable gate current methods [16]–[18]. AGD was first

applied to insulated-gate bipolar transistors (IGBTs) [15]–[17]. Since they are relatively slow switching devices, real-time feedback controls have been adopted either in analog ways [15]–[17] or digital ways [18]. AGD for SiC MOSFETs and GaN FETs have begun to be studied recently [8]–[13]. The intrinsic challenge of AGD for WBG power devices is their fast-switching capability. Although some real-time feedback controls of AGD for SiC MOSFETs are reported [8], [9], they become harder to realize as the switching speed and the frequency become higher, because ultra-fast comparators and analog-digital converters are necessary [10], [13], [16]. The noise-immunity issue further makes it difficult. Instead of real-time feedback methods, open-loop controlled or sequentially optimized AGDs have been studied [13], [14], whose operation is digitally adjustable after the circuit implementation. In particular, multi-voltage level, or variable gate voltage level AGDs [11]–[13] are investigated for SiC MOSFETs for relative simplicity in their implementation.

Our research group has developed a digital active gate driver for SiC MOSFETs based on the architecture of a digital-to-analog converter [19]. The proposed gate driver generates the gate-source voltage (V_{GS}) waveform of the MOSFET flexibly by the successive alteration of V_{GS} using a multibit gate signal sequence. It can be categorized as a variable gate voltage method. Multi-voltage level AGDs are strongly related to the characteristics of the MOSFET, because the V_{GS} governs the static characteristics, such as the relationship between drain current and drain-source voltage ($I_D - V_{DS}$ curve), under the condition. Therefore, identifying the voltage level corresponding to the gate signal which is effective for the operating condition of the given device is a crucial point in AGD strategy. The strategy has been addressed in [13], and the trajectory model for the proposed AGD method is developed. However, the strategy is not clearly understood based on the device characteristics.

This work proposes the strategy for the digital active gate driver developed on the state space, using the $I_D - V_{DS}$ characteristics obtained from a device model. The switching trajectory of MOSFETs is often referred in explaining the switching behavior [9], [16]. We are

directly going to control the trajectory by choosing the operating points on the state space, which is previously predicted with the device model. It is confirmed in the experiment that the method is valid in different operating conditions. The difference in the strategies at turn-on/turn-off is also addressed.

II. ACTIVE-GATE-DRIVE STRATEGY USING DIGITAL ACTIVE GATE DRIVER

This section summarizes the digital active gate driver proposed in [19], and proposes the improvement for high-frequency operation. Based on the dynamical behavior of AGD, the strategy is designed using the behavior estimated by a device model.

A. Configuration of Digital Active Gate Driver Using GaN HEMTs

The configuration of n -bit digital active gate driver is shown in Fig. 1. It is designed from the binary-weighted resistor digital-to-analog converter [20] and composed of n -parallel gate drive circuits with gate resistances of $2^n R$ Ohms, where R is the gate resistance for the most significant bit (MSB). The V_{GS} waveform of the MOSFET is treated discretely by a multibit gate signal sequence. In this work, we investigate the four-bit system and $b_{in} = b_3 b_2 b_1 b_0$ is defined as the gate signal in a hexadecimal number. The MOSFET is on/off when $b_{in} = 0xF / 0x0$, where ‘0x’ means the following number is hexadecimal. During the switching transient, the gate signals are successively changed at the clock rate of the controller to divide the gate-input voltage (V_{drv}) by gate resistors, thereby turning on/off the MOSFET actively.

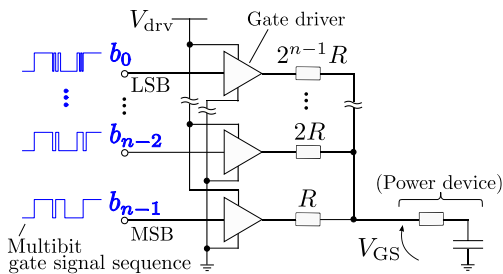


Fig. 1. Configuration of n -bit digital active gate driver.

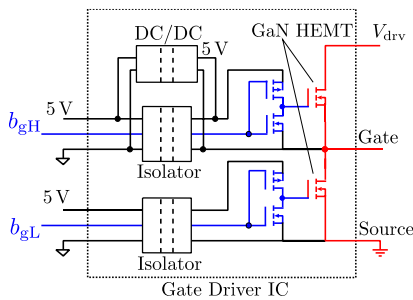


Fig. 2. Configuration of GaN HEMT-based gate driver IC [21]. $b_{\text{gH}}/b_{\text{gL}}$ refers to the high/low-side input signal. Each GaN HEMT of the half-bridge is driven by a push-pull circuit of Si MOSFETs (kataban, manufacturer). A DC-DC converter (ROE-0505S, RECOM Power GmbH) is used to provide the isolation for the high-side GaN HEMT.

For the gate driver in each bit, we apply GaN HEMT-based gate driver proposed in [21]. Its schematic diagram is shown in Fig. 2, which consists of a half-bridge circuit of GaN HEMTs (EPC2014C, EPC Corp.). They are driven by push-pull circuits of Si MOSFETs (US6M1, ROHM Co., Ltd.). In the proposed digital active gate driver, each single gate drive circuit needs to be switched at a much higher frequency than the driven SiC MOSFET. Therefore, GaN HEMT's high-frequency-switching capability is preferable.

B. AGD strategy based on the I-V characteristics

The proposed digital active gate driver requires proper gate signal sequences to improve the switching characteristics. Here we propose a strategy for signal sequence selection utilizing the $I_D - V_{DS}$ characteristics of SiC MOSFETs obtained from a surface-potential-based device model [22]. The device model is based on the surface potential of the channel of the MOS structure and can reproduce the $I_D - V_{DS}$ characteristics accurately especially in high-power regions.

As described above, the digital active gate driver designates the V_{GS} value corresponding to the gate signal. This is equal to selecting the $I_D - V_{DS}$ curve corresponding to the gate signal. Figure 3 shows the $I_D - V_{DS}$ curves of a SiC MOSFET (SCT2450KE, ROHM Co., Ltd.) for several V_{GS} values obtained from the simulation using the device model. Here, the designated V_{GS} values can be selected by the 4-bit digital active gate driver, and the corresponding gate signals (b_{in}) are provided together. When we draw a load line for a given operating condition, the cross-points between the load line and the $I_D - V_{DS}$ curves are evaluated. They are regarded as the operating points of the MOSFET selected by the corresponding gate signals. Note that the $I_D - V_{DS}$ curves will vary because of the variations in device parameters. In this work, the parameters of the device model are adjusted to match the characteristics of the MOSFET implemented in the experiment described in Section III.

We investigate the strategy at the turn-on and the turn-off operations of the SiC MOSFET in double-pulse testing.

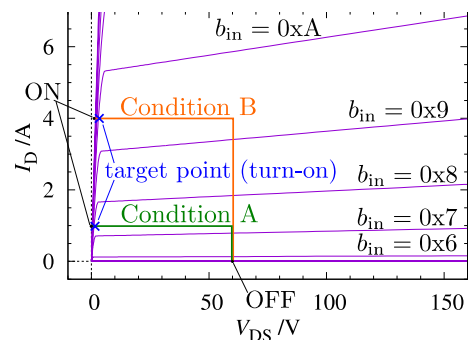


Fig. 3. $I_D - V_{DS}$ characteristics of SCT2450KE SiC MOSFET obtained from the device model [22], and load lines of an ideal inductive load. b_{in} refers to the input signal of digital active gate driver in hexadecimal number. Target points in AGD strategy during turn turn-on are shown

with crosses.

The two operating conditions at the different drain current shown in Fig. 3 are picked up to investigate the effective gate signal sequence which governs the operating conditions. Here, the operating points during the MOSFET is on/off are named as ON/OFF points, respectively. In this work, we adopt a simple gate signal sequence: $0x0 \rightarrow b_{act}$ (for 60ns) $\rightarrow 0xF$ for turn-on and $0xF \rightarrow 0x0$ (for 20ns) $\rightarrow b_{act}$ (for 80ns) $\rightarrow 0x0$ for turn-off, where b_{act} is the gate signal to be selected during the active period. The appropriate b_{act} at a given condition is predicted by checking the cross point of the $I_D - V_{DS}$ curves and the load line. For example, in the turn-on operation, the operating point right after the trajectory transits near the OFF point is predicted to be effective, as given as target points in Fig. 3.

III. EXPERIMENTAL VERIFICATION IN DOUBLE-PULSE TESTING

The proposed strategy for selecting the crucial gate signal is verified in double-pulse testing. The two operating conditions are picked up at the different values of the drain current as shown in Fig. 3. AGD for the turn-on and turn-off operations are investigated independently. The difference of the strategies is also addressed.

A. Experimental Setup

Figure 4 shows the photograph of the 4-bit digital active gate driver and the experimental circuit fabricated on a PCB. The schematic diagram is given in Fig. 5. The four

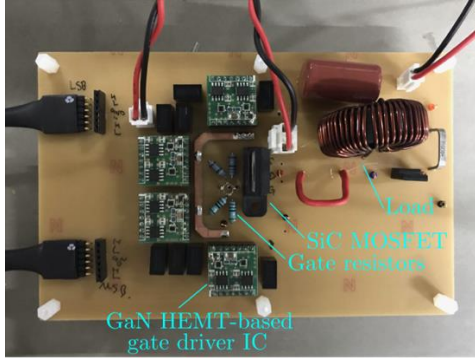


Fig. 4. Photograph of 4-bit GaN HEMT-based digital active gate driver and experimental circuit.

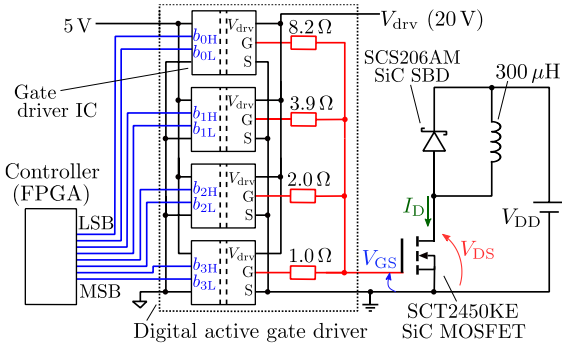


Fig. 5. Schematic diagram of experimental circuit for double-pulse testing.

GaN gate driver ICs are used to form the 4-bit digital active gate driver. The gate resistances are chosen to be $2^k \Omega$, where k refers to the number of the bit. The supplied voltage is set at 20 V to drive the SiC MOSFET (SCT2450KE). Gate signals are generated by a digital controller, which incorporates an FPGA (Zynq UltraScale+MPSoCs, Xilinx Inc.). The clock rate of the gate signals is set at 200 MHz. A SiC Schottky barrier diode (SCS206AM, ROHM Co., Ltd.) and an inductor of 300 μ H configure the double-pulse testing circuit, and $V_{DD} = 60$ V is supplied. The measuring apparatus is as follows; oscilloscope: MDO-4104-3 (Tektronix, Inc.), voltage probes: TPP1000, P5122 (Tektronix), current probe: TCP0300A (Tektronix).

B. AGD Results During Turn-on

At the turn-on operation, the switching trajectory transits from the same OFF point on the state space but converges into different ON points according to I_D . Therefore, the AGD strategy for turn-on strongly depends on the operating condition set here.

Firstly, operating condition A is investigated. From Fig. 3, $0x8$ is selected as the gate signal to be set during the active period. The adopted gate signal sequence is listed in Table I as AGD-ON 1. The switching waveforms of the MOSFET during turn-on with/without AGD are shown in Fig. 6. It is confirmed that the ringings of I_D and V_{DS} are suppressed, and the peak of I_D decreased from 2.65 A to 1.63A. It is also noted that the fluctuation of V_{GS} is also mitigated during the active period. The switching trajectories of the SiC MOSFETs on $I_D - V_{DS}$ state space are provided in Fig. 7. With AGD, the trajectory first moves toward the cross point of the $I_D - V_{DS}$ curve and the load line (target point in Fig. 3), suppressing the ringings. The designated operating point during the active period is almost in the quasi-linear region of the MOSFET. The Miller effect of the MOSFET has almost finished during the period.

Next, the operating condition is changed to B. In this case, from Fig. 3, $0xA$ is predicted as the gate signal to select during the active period. Here we set three cases for comparison; without AGD, AGD-ON 2 (gate signal sequence for condition B), and AGD-ON 1, as listed in Table I. The switching waveforms and the trajectories of the three cases are shown in Figs. 8 and 9. With AGD-ON 2, the overshoot of I_D is clearly suppressed from 5.34 A to 4.54 A. However, with AGD-ON 1, the switching trajectory first stays in the middle of the transition during the active period. Subsequently, the trajectory transit toward ON point from that point to face larger ringing than the case without AGD. We can see that the gate signal sequence of AGD-ON 1 is no longer valid in condition B.

TABLE I ADOPTED GATE SIGNAL SEQUENCES FOR TURN-ON	
Case	Gate signal sequence (in hexadecimal number)
without AGD	$0 \rightarrow F$
AGD-ON 1	$0 \rightarrow 8$ (for 60 ns) $\rightarrow F$
AGD-ON 2	$0 \rightarrow A$ (for 60 ns) $\rightarrow F$

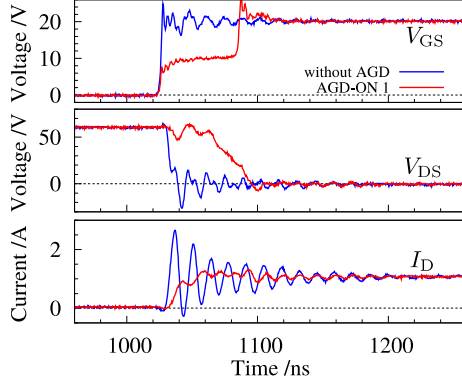


Fig. 6. Switching waveforms during turn-on with/without AGD in condition A.

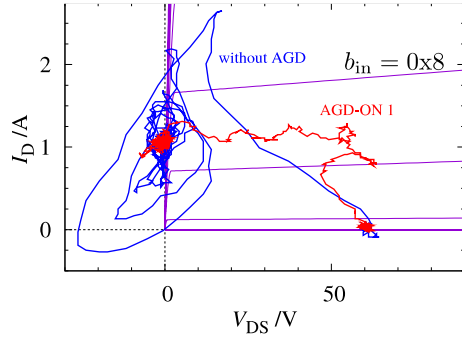


Fig. 7. Switching trajectories on state space during turn-on with/without AGD in condition A.

These results confirm that the crucial gate signal for turn-on operation depends on the value of I_D , and the signal can be identified by checking the corresponding operating point. It is also shown that selecting inappropriate gate signals lead to even worse ringing.

C. AGD Results During Turn-off

At the turn-off operation, the switching trajectory transits from different ON points on the state space according to the operating condition. However, they converge into the same OFF point, as long as the V_{DS} is kept at the same. What is more, even the value of the V_{DS} becomes different, it is expected that it makes less significant changes on which gate signal to choose when compared to turn-on operation.

For these reasons, we set the two AGD sequences as shown in Table II. The signal $b_{in} = 0x6$ designates an operating point slightly above the OFF point on the state space, and the signal $b_{in} = 0x5$ designates a point almost in a cut-off region. Figs. 10 and 11 show the results in condition A and Figs. 12 and 13 show those in condition B. In both conditions, the two AGD cases show different behaviors. With AGD-OFF 1, the switching trajectory stays at an operating point above the OFF point during $b_{in} = 0x6$ is given, and after that period the V_{DS} and I_D oscillate. It is expectable that the farther the operating point is from the OFF point, the larger the following oscillation will be. On the other hand, with AGD-OFF 2, the switching trajectory converges into the OFF point during the active period without additional ringing. The peak of V_{DS} is reduced

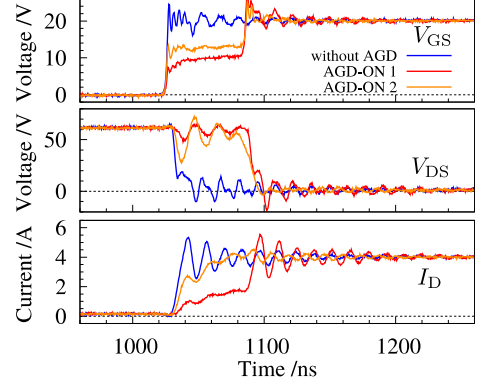


Fig. 8. Switching waveforms during turn-on with/without AGD in condition B.

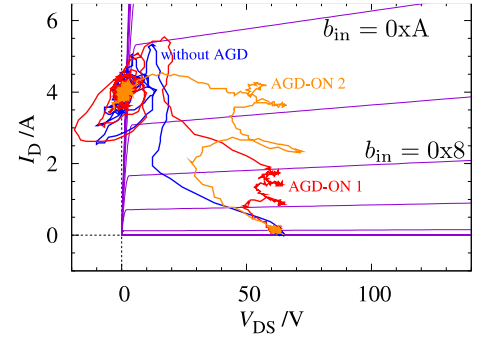


Fig. 9. Switching trajectories on state space during turn-on with/without AGD in condition B.

from 75.6 V to 66.8 V in condition A, and from 134.0 V to 80.4 V in condition B.

The results indicate that the ringing is suppressed by setting the gate signal whose corresponding operating point is almost in a cut-off region at the end of the turn-off sequence. It is also confirmed that the crucial gate signal for turn-off does not so much depend on the value of I_D .

TABLE II ADOPTED GATE SIGNAL SEQUENCES FOR TURN-OFF	
Case	Gate signal sequence (in hex. number)
without AGD	$F \rightarrow 0$
AGD-OFF 1	$F \rightarrow 0$ (for 20 ns) $\rightarrow 6$ (for 80 ns) $\rightarrow 0$
AGD-OFF 2	$F \rightarrow 0$ (for 20 ns) $\rightarrow 5$ (for 80 ns) $\rightarrow 0$

D. Discussions

The experimental results confirm that the proposed digital active gate driver can suppress the ringing in different operating conditions during both turn-on and turn-off according to the designed strategy. It is also confirmed that the required condition is obtained for setting the appropriate gate signal sequence. It implies that the device model can predict the state.

To conduct a simple experiment, the target V_{GS} waveform is simplified with a resolution of 4 bit. The strategy does not focus on the minimization of the switching loss or the switching time. Based on this work, the algorithm for generating the gate signal sequences needs to be developed, together with a more sophisticated strategy and a larger number-of-bit gate driver. One major

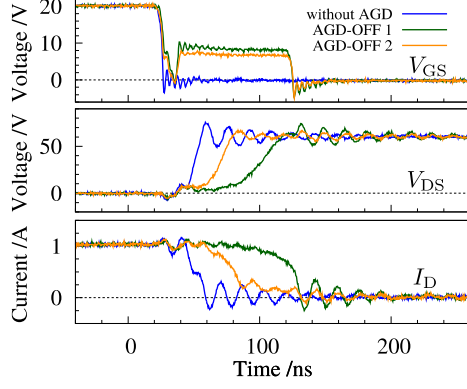


Fig. 10. Switching waveforms during turn-off with/without AGD in condition A.

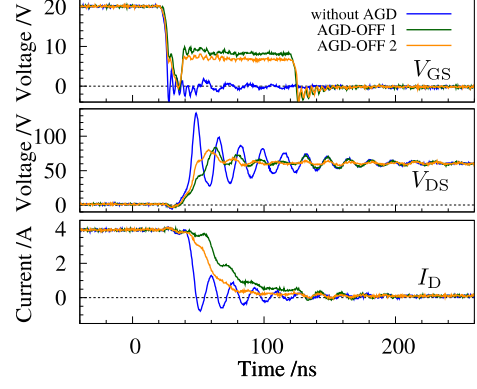


Fig. 12. Switching waveforms during turn-off with/without AGD in condition B.

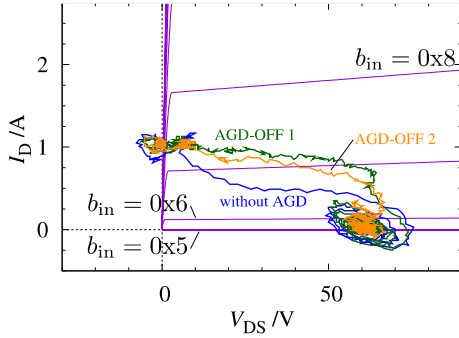


Fig. 11. Switching trajectories on state space during turn-off with/without AGD in condition A.

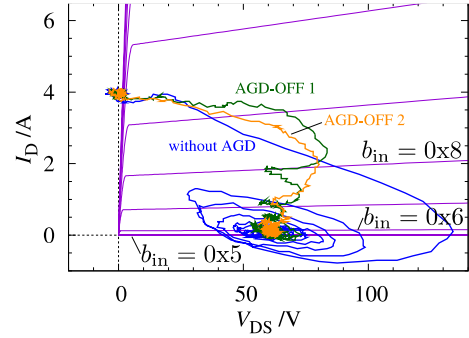


Fig. 13. Switching trajectories on state space during turn-off with/without AGD in condition B.

future challenge is the handling of the variations in device parameters. It is clear that the variation is hard to predict before the implementation of the device. This challenge should be assessed with some optimization methods [23], such as sequential optimization, together with the predictive method.

IV. CONCLUSIONS

In this work, we investigated an AGD strategy for the digital active gate driver for SiC MOSFETs. The strategy utilizes the $I_D - V_{DS}$ characteristics of the SiC MOSFET obtained from the device model, and the operating points on the state space are analyzed. The experimental results show that the proposed strategy can suppress the overshoot and the ringing during both turn-off and turn-on by selecting appropriate gate signal sequences. It is also confirmed that the strategy is feasible in different operating conditions by adjusting the gate signal, which is predicted from the device model. Since the signal is easily adjustable by the outer controller, the proposed gate driver can be applied to wide operating conditions without adjusting the circuit.

This work focused on the selection of the crucial gate signal, so the target V_{GS} waveform is simplified. Also, only the static characteristics are utilized in the strategy. Even so, the result can benefit other types of multi-voltage level AGDs, because the $I_D - V_{DS}$ characteristics and the value of V_{GS} are strongly related to each other. To address this point of view, we need to focus on the switching

trajectory on the state space. Further researches are under consideration, such as dealing with variations in device parameters and its application to power converters. A more sophisticated strategy and an improved resolution of the digital active gate driver are necessary for these challenges.

ACKNOWLEDGMENT

This work was partially supported by the Program on Open Innovation Platform with Enterprises (OPERA), Research Institute and Academia of Japan Science and Technology Agency, Cross-ministerial Strategic Innovation Promotion Program (SIP) of New Energy and Industrial Technology Development Organization, and JSPS KAKENHI Grant Number 20J10227. The authors would like to thank Dr. Takafumi Okuda for his support in the experiment.

REFERENCES

- [1] J. Palmour, R. Singh, R. Glass, O. Kordina, and C. Carter, "Silicon carbide for power devices," in *Proceedings of 9th International Symposium on Power Semiconductor Devices and IC's*, pp. 25–32, 1997.
- [2] T. Kimoto, "Material science and device physics in SiC technology for high-voltage power devices," *Jpn. J. Appl. Phys.*, vol. 54, no. 4, art. no. 040103, 2015.
- [3] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, 2014.

- [4] X. She, A. Q. Huang, O. Lucía, and B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, 2017.
- [5] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 707–719, 2016.
- [6] I. Josifović, J. Popović-Gerber, and J. A. Ferreira, "Improving SiC JFET Switching Behavior Under Influence of Circuit Parasitics," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3843–3854, 2012.
- [7] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Stability Considerations for Silicon Carbide Field-Effect Transistors," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4453–4459, 2013.
- [8] A. P. Camacho, V. Sala, H. Ghorbani, and J. L. R. Martinez, "A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9032–9042, 2017.
- [9] S. Acharya, X. She, F. Tao, T. Frangieh, M. H. Todorovic, and R. Datta, "Active Gate Driver for SiC-MOSFET-Based PV Inverter with Enhanced Operating Range," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1677–1689, 2019.
- [10] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active Gate Driver for Crosstalk Suppression of SiC Devices in a Phase-Leg Configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, 2014.
- [11] N. Rouger, Y. Barazi, M. Cousineau, and F. Richardeau, "Modular Multilevel SOI-CMOS Active Gate Driver Architecture for SiC MOSFETs," in *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2020, pp. 278–281.
- [12] H. C. P. Dymond, D. Liu, J. Wang, J. J. O. Dalton, and B. H. Stark, "Multi-level Active Gate Driver for SiC MOSFETs," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 5107–5112.
- [13] S. Zhao *et al.*, "Adaptive Multi-Level Active Gate Drivers for SiC Power Devices," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1882–1898, 2020.
- [14] D. J. Rogers and B. Murmann, "Digital active gate drives using sequential optimization," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 1650–1656.
- [15] N. Idir, R. Bausière, and J. J. Franchaud, "Active Gate Voltage Control of Turn-on di/dt and Turn-off dv/dt in Insulated Gate Transistors," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 849–855, 2006.
- [16] S. Musumeci, A. Raciti, A. Testa, A. Galluzzo, and M. Melito, "Switching-Behavior Improvement of Insulated Gate-Controlled Devices," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 645–653, 1997.
- [17] S. Igarashi, S. Takizawa, M. Tabata, M. Takei, and K. Kuroki, "An Active Control Gate Drive Circuit for IGBTs to Realize Low-noise and Snubberless System," in *Proceedings of 9th International Symposium on Power Semiconductor Devices and IC's*, 1997, pp. 69–72.
- [18] K. Miyazaki, S. Abe, M. Tsukuda, I. Omura, K. Wada, and M. Takamiya, "General-Purpose Clocked Gate Driver (CGD) IC with Programmable 63-Level Drivability to Reduce IC Overshoot and Switching Loss of Various Power Transistors," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 1640–1645.
- [19] H. Takayama, T. Okuda, and T. Hikiyara, "A Study on Suppressing Surge Voltage of SiC MOSFET Using Digital Active Gate Driver," in *2020 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, 2020, pp. 1–5.
- [20] D. F. Hoeschele Jr., *Analog-to-Digital/Digital-to-Analog Conversion Techniques*. John Wiley and Sons Ltd, 1968, Chapter 5.
- [21] K. Nagaoka, K. Chikamatsu, A. Yamaguchi, K. Nakahara, and T. Hikiyara, "High-speed Gate Drive Circuit for SiC MOSFET by GaN HEMT," *IEICE Electron. Express*, vol. 12, no. 11, pp. 1–8, 2015.
- [22] Y. Nakamura, M. Shintani, K. Oishi, T. Sato, and T. Hikiyara, "A simulation model for SiC power MOSFET based on surface potential," in *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 2016, pp. 121–124.
- [23] S. Fukunaga, H. Takayama, and T. Hikiyara, "A Study on Optimizing Waveform of Digital Active-Gate Driving for SiC MOSFET Using Genetic Algorithm," in *the Annual Meeting record, I.E.E. Japan*, 2020, 4-100 (in Japanese).