

**Experimental considerations for integration method of Si
thin-film microchips for fluidic self-assembly**

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Abstract

Fluidic self-assembly is a technique in which numerous semiconductor chips are integrated spontaneously. Here, we demonstrate that the integration efficiency is significantly improved by optimizing the separation conditions and appropriately controlling the external forces to which the microchips are subjected to the solution. In particular, an external drag force was found to prevent the Si microchips from forming aggregations and prompting transfer to the Si receiver pockets. This resulted in a significant improvement in the integration selectivity. Moreover, experiments with various microchip sizes statistically determined the effect of the Si receiver chip rinse on the evaluation functions: deposition selectivity, yield, and overall yield. While rinsing was effective for fluidic self-assembly of 10- μm -scale Si microchips, rinsing of 800-nm-scale chips is indicated to have different integration mechanisms. Our quantitative analysis indicated the potential applicability of the fluidic self-assembly technique to the integration technologies of Si micro semiconductor devices.

Introduction

In the field of optoelectronics, scaling down, high-density integration, low-cost and high-throughput production are in high demand for a variety of devices, such as electronic large-scale-integration chips, light-emitting-diode displays, and photonic integrated circuits [1–7]. Integrating ultrasmall-scale semiconductor chips, often referred to as microchips or microelectronic devices, offers several significant advantages and opens up new possibilities in various fields. Smaller chip sizes enable higher transistor densities, leading to improved performance. With more transistors packed into a smaller area, microchips can offer faster processing speeds, increased computational power, and enhanced functionality. The ability to create smaller chips allows for miniaturization of electronic devices. This is particularly important in applications where size and weight constraints are critical, such as in mobile devices, wearables, medical implants, and aerospace systems. Smaller chips generally require less power to operate, leading to improved energy efficiency. This is beneficial in applications where power consumption is a concern, such as in battery-operated devices or energy-constrained environments. It can result in longer battery life and reduced energy costs. Integrating very small-scale semiconductor chips thus opens up possibilities for high-performance, compact, and energy-efficient electronic and photonic devices across various industries, such as ultrahigh-speed nanoelectronic computing systems [8], photodetector arrays [9], optical waveguides [10], photonic integrated circuits [11–13], and biosensing [14,15]. However, the conventional pick-and-place integration method inevitably suffers from the limitations regarding the

required factors. Fluidic self-assembly is a technique that integrates microscale chips with various functions released from multiple types of wafers onto a single host chip in the liquid phase [16–25]. In fluidic self-assembly, many microscale chips can be simultaneously integrated, in contrast to the pick-and-place method. However, the previous research has focused on device integration at several millimeters or tens of micrometers, as summarized in Table 1, presumably due to the severe adhesion of smaller chips to their original substrates [16–25]. Recently, we conducted a fluidic transfer of submicron-scale Si chips by controlling the surface tension as a technical step towards ultrahigh-density integration [26]. However, the yield of the process was as small as 2%, based on the fraction of pockets of the host chip that are filled with the microchips, in our previous work [26]. In this study, we investigated the technical methods used in the fluidic transfer process of Si microchips to improve the yield. In this process, Si microchips, which are initially patterned on a SOI wafer, are firstly separated by taking advantage of the difference in etching rate between Si and SiO₂ by hydrofluoric acid. Subsequently, these microchips are integrated onto another substrate (receiver piece) using gravity in an etching solution. Finally, external force is applied to move these microchips into pockets within the receiver pieces. We utilize fluidic resistance as this external force by rinsing the receiver pieces with water. To quantitatively evaluate the integration efficiency, we set up evaluation functions: deposition selectivity, yield, and overall yield. An integration method for high integration efficiency was then proposed based on the quantitative evaluation of various integration conditions.

Experimental Methods

As the substrate that releases the Si microchips (“releaser”), we employed a silicon-on-insulator (SOI) wafer (single-side polished, *p*-on-*n*-type, diameter: 6 inches, SOI-layer thickness: 200 nm, crystalline plane orientation: <100>, dopant: boron, doping concentration: $\sim 1 \times 10^{15} \text{ cm}^{-3}$, buried-oxide (BOX) layer thickness: 200 nm or 2 μm , Si-substrate thickness: 625 μm , crystalline plane orientation: <100>, dopant: phosphorus, doping concentration: $\sim 1 \times 10^{15} \text{ cm}^{-3}$). Note that while some specifications of the wafers, such as crystal orientation, dopant, and doping concentration, may not be crucial for this study, we still provide a description of these parameters in case they have any potential influence on the chemical etching rate. As the host substrate (“receiver”), we employed a Si wafer (single-side polished, *p*-type, diameter: 6 inches, thickness: 625 μm , crystalline plane orientation: <100>, dopant: boron, doping concentration: $\sim 1 \times 10^{14}\text{--}10^{17} \text{ cm}^{-3}$). The releaser and receiver's square pillar- and pocket-shaped patterns were formed on the SOI and Si wafers by photolithography with dry etching; the details are described below.

Figure 1 presents the schematic flow diagram of the releaser fabrication process. The SOI wafer was first spin cleaned using an $\text{H}_2\text{SO}_4\text{--H}_2\text{O}_2$ solution (5:1 vol.) for 20 s. Then, the SOI wafer was dried on a hotplate at 110 °C for 5 min. Next, a photoresist film (TDMR-AR80-5cp, Tokyo Ohka Kogyo Corp.) was spin-coated (rotation velocity: 800 rpm) onto the SOI wafer to a thickness of 1.3 μm . Then, the SOI wafer with the photoresist was soft-baked on a hotplate at 90 °C for 90 s. Subsequently, the SOI wafer was exposed to a Hg lamp (365 nm, 380 msec) through a photomask in

1 an *i*-line stepper. The photoresist on the SOI wafer was then developed using a
2 tetra-methyl-ammonium-hydroxide aqueous solution. The area of the SOI wafer that
3 was not covered by the photoresist was dry-etched by SF₆ and C₄F₈ to a depth of 300
4 nm (i.e., approximately the middle of the BOX layer). Then, the residual photoresist on
5 the SOI wafer was removed using an oxygen plasma. Figure 2 shows a cross-sectional
6 scanning electron microscope image of the releaser piece. As shown in Figure 2, the Si
7 microchips were found to have a width of 2 μm.

8
9 Figure 3 shows the schematic flow diagram of the receiver fabrication process.
10 After being cleaned in the same manner as the SOI wafer, the Si wafer for the receiver
11 was spin-coated (800 rpm) with a TDMR-AR80-5cp photoresist film to a thickness of
12 1.3 μm. Then, the Si wafer with the photoresist was soft-baked, exposed, and developed
13 in the same manner as the SOI wafer, except for the exposure duration of 420 msec.
14 Then, the area of the Si wafer that was not covered by the photoresist was dry-etched by
15 SF₆ and C₄F₈ to a depth of roughly 2 μm. Subsequently, the residual photoresist on the
16 Si wafer was removed by oxygen plasma. Figure 4 depicts the schematic bird's-eye
17 views, and cross-sectional views of the Si receiver, and Figure 5 presents plane-view
18 scanning electron microscope images of the receiver piece.

19
20 Figure 6 shows the schematic flow diagram of our experimental process of
21 fluidic self-assembly. The patterned releaser and receiver wafers were diced into
22 ~1-cm²- and 25-mm²-area pieces, respectively. A releaser piece was then submerged in a
23 hydrofluoric acid (HF) – ethanol solution (1:4 vol.) with ultrasonication (room
24 temperature, 30 min), with the patterned face of the releaser piece up. As the result of

chemical etching of the BOX layer by HF, Si microchips were released into the solution. In some experiments, RCA cleaning [27–29] was performed for 20 min on a receiver piece and releaser piece to change the surface potential of the Si substrate before submerging the releaser piece. (Detailed information regarding the RCA cleaning process will be provided in section (b) of the Results and Discussion.) Subsequently, a receiver piece was added to the solution. The solution was then left with the patterned face of the receiver piece up without ultrasonication (room temperature, 20 h). Consequently, the Si microchips deposited onto the receiver piece. Incidentally, we roughly dry-etched the Si wafer to form the receiver's pockets with no specific target depth at the stage of this study. Consequently, the depth of pockets became about 2 μm , significantly larger than the thickness of Si microchips, 200 nm. The depth of pockets is to be modified into a comparable scale to the microchip thickness in our future work, to meet the conceptual drawing in Figure 6. The receiver piece was removed from the solution without cleaning and dried naturally in the atmosphere. Some experiments performed a 10-second rinse in ultrapure water using a shaker (2-7827-01, As One Corp.) before drying. (Detailed information about the rinse process will also be provided in section (b) of the Results and Discussion.) After completing the entire experimental process, we counted the number of Si microchips deposited on the receiver piece, as well as those present in the receiver's pockets, using optical microscope images. An image analyzer software Image-J (National Institute of Health) was utilized to accurately count the number of microchips, even in cases where chip aggregation occurred.

Results and Discussion

(a) Optimization of Si microchips separation conditions towards the maximum deposition yield

We define the deposition yield as the fraction of the number of Si microchips on the whole surface of the receiver that separated from the Si releaser piece, the deposition selectivity as the fraction of the number of Si microchips observed in the pockets out of that on the whole surface of the receiver (i.e., pockets + terrace), and the overall yield as the fraction of the number of Si microchips observed in the pockets out of that separated from the Si releaser piece.

Deposition yield Y

$$= \frac{\text{Total number of deposited chips on a receiver piece}}{\text{Total number of chips separated from a Si releaser piece}}$$

$$\text{Deposition selectivity } S = \frac{\text{Number of chips deposited in pockets}}{\text{Total number of deposited chips on a receiver piece}}$$

Overall yield $YS = Y \times S$

$$= \frac{\text{Number of chips deposited in pockets}}{\text{Total number of chips separated from a Si releaser piece}}$$

In our previous work [26], the Si microchips were separated from the releaser piece by immersing the receiver piece in a 100-ml beaker with 10 ml of a 5-fold diluted hydrofluoric acid solution in ethanol and the releaser piece for 30 min at 37 kHz, followed by immersion in the receiver piece for 3 h. The resulting yield, selectivity, and overall yield are shown in Figure 7. Both the deposition yield and overall yield were marginal. In particular, the yield was 0.029, which means that only 2.9% of the Si

microchips separated from the releaser chip were integrated onto the receiver chips. In order to improve the overall yield, it is necessary to improve the yield, as discussed below.

The Si microchip separation conditions were optimized. In the condition that uses a large amount of etching solution for Si microchip separation, it takes much longer for the separated Si microchips to settle and transfer to a receiver piece. The number of microchips adsorbed on the beaker wall is significantly increasing. Therefore, in order to identify the experimental conditions for achieving a high yield, the experiment was conducted under the conditions in which the beaker volume, the amount of etching solution, and the immersion time were changed in the experimental conditions of the previous research [26]. Table 2 lists the volume of the beaker and the amount of etching solution used in the experiment. Figure 8 shows a plot of the yield Y when the immersion time was changed under each experimental condition, as shown in Table 2. Figure 8 indicates that using a smaller beaker and separating the Si microchips with a lower etching solution volume leads to a high deposition yield. This is because the smaller the beaker, the smaller the bottom area of the beaker, the higher the concentration of Si microchips per unit area, and the smaller the volume of etchant, the higher the concentration of Si microchips per unit volume. In addition, the longer the immersion time, the more Si microchips accumulated on the receiver; however, the deposition yield Y did not increase after immersion for more than 20 h. As a result, the maximum deposition yield was 0.9. As clearly observed in Figure 8, it was found that the maximum yield was obtained when 0.9 ml hydrofluoric acid solution was diluted 5-fold with ethanol (the minimum volume for the experimental operation) and the

releaser piece was placed in a 5 ml beaker, and the Si microchips were separated from the releaser piece by ultrasonic vibration at 37 kHz for 30 min, followed by the receiver piece and immersion for 20 h.

(b) Mechanism of aggregate formation and solution to this problem

In achieving a high yield, the Si microchips on the Si receiver piece form aggregates owing to the capillary force while the Si receiver is being dried. Figure 9 shows a microscopic image of the receiver piece after the experiment under the conditions determined in the previous section, showing that the Si microchips that accumulated from the releaser piece to the receiver piece form aggregates. The Si microchips formed aggregates on the receiver piece. When the Si microchips form aggregates on the receiver piece, they do not accumulate in the receiver pocket. Therefore, these aggregates lower deposition selectivity S and overall yield YS . In order to improve S and YS , we discuss how to form Si microchip aggregations and prevent them in detail.

Figure 10 shows a schematic flow of the formation of aggregates of the Si microchips. (i) First, some liquid droplets of Si microchip dispersion remained after the Si receiver chip was pulled up from the Si microchip dispersion. (ii) These liquid droplets contained many Si microchips inside. Subsequently, the Si microchips flow around and collide with each other owing to the difference in temperature and pressure between the inside and outside of the droplets. Subsequently, the collided Si microchips formed cores of the aggregate. (iii) Collision probability between Si microchips

1 increases as droplets dry and aggregates become larger. (iv) Finally, when the droplets
2 are sufficiently dry, adhesive forces derived from liquid cross-linking forces complete
3 the Si microchip aggregates and remain on the Si receiver.

4
5 In this study, two methods to prevent the formation of aggregates were
6 considered: RCA cleaning and direct external force application to Si microchips. RCA
7 cleaning is performed in two steps: SC-1 cleaning and SC-2 cleaning, in which the Si
8 wafer surface is oxidized with hydrogen peroxide by SC-1 cleaning. Then, the Si oxide
9 is etched with ammonia to remove all particles attached to the wafer surface. In addition,
10 the surface potentials of Si and various particles became negative, and the particles were
11 removed by electrostatic repulsion. In this study, we attempted to prevent Si microchip
12 aggregation by creating an electrostatic repulsive force between the Si microchips by
13 negatively affecting their surface potential. The method is described as follows. First,
14 water, hydrogen peroxide, and ammonia were mixed in a volume ratio of 5:1:1 and then
15 preheated to 80°C. The releaser and receiver pieces were immersed in the solution for
16 10 min (SC-1 cleaning). Subsequently, water, hydrogen peroxide, and hydrochloric acid
17 were mixed at a volume ratio of 6:1:1, preheated to 80°C, and the releaser and receiver
18 pieces were immersed in this solution for 10 min (SC-2 cleaning). After RCA cleaning,
19 the Si microchips were separated and integrated onto the receiver piece under the
20 conditions specified above.

21
22 Figure 11 shows a microscopic image of Si microchips integrated onto the
23 receiver piece after RCA cleaning of the receiver and releaser pieces. As shown in
24 Figure 11, the aggregates could not be suppressed. This is because the liquid bridging

force, a factor in the formation of agglomerates, is sufficiently larger than the repulsive force owing to the Coulomb force, and aggregates derived from the liquid bridging force are thought to have formed, overcoming the electrostatic repulsive force.

We considered applying an external force to the Si microchips as a second measure to prevent aggregate formation. Figure 12 shows a schematic diagram of the external force applied to the Si microchips on the receiver piece by shaking the receiver piece in the liquid. As shown in Figure 12, rinsing the receiver piece in a fluid can apply an external force derived from fluid resistance to the Si microchips integrated on the Si receiver piece. Because the rinsing process applies an external force to the Si microchips on the receiver pieces, as shown in Figure 12, the equation of motion for the external force in the horizontal direction can be expressed by the equations of motion [30]. The equation of motion was established as follows:

$$m \frac{dv}{dt} = f(u) - \mu N \quad (1)$$

where m is the mass of the Si microchip, v is the velocity of the Si microchips, t is time, $f(u)$ is the fluid resistance received by the Si microchips, μ is the dynamic friction coefficient, N is the normal force, and u is the vibration speed of the rinse liquid. From Equation (1), it can be seen that the fluid resistance depends on the flow rate of the rinse fluid.

To add a more significant force than the liquid crosslinking force while the Si receiver microchips were dried, we added fluid resistance with a shaker (2-7827-01, As One Corp.). We used the reciprocating shake mode of the shaker to provide fluid resistance. In this scheme, the Si receiver chips were fixed by tweezers in a beaker filled

1 with pure water on the shaker after pulling up from the Si microchip dispersion. Then,
2 the shaker and beaker were shaken at a constant vibration frequency, adding fluid
3 resistance to the fixed Si receiver chip. Using this method, an external force more
4 significant than liquid cross-linking was applied to the Si microchips. The Si microchips
5 were successfully accumulated in the pocket of the Si receiver before aggregates were
6 formed. Simultaneously, we confirmed that the Si microchips on the terrace dispersed in
7 pure water in a beaker resulted in a decrease in yield. Therefore, we attempted to
8 maximize the selectivity and yield by changing the magnitude of the fluid resistance
9 applied to the Si microchips. In subsequent experiments, the rinse frequency was varied
10 from 0 to 100 min⁻¹.

11
12 Figure 13 and 14 show the overhead views after rinsing for the small and large
13 rinse frequencies, respectively. A comparison of the two figures shows that the number
14 of Si microchips accumulated in the pocket of the receiver piece increased when the
15 rinse frequency was high. In contrast, the number of Si microchips on the receiver piece
16 decreased significantly because they were dispersed in the rinse solution. It was
17 confirmed that the rinse suppressed the formation of aggregates and accumulated Si
18 microchips on the terrace in the pocket. The yields Y , selectivity S , and overall yield YS
19 at each frequency are shown in Figure 15. In the graph, L1, L2, L3, L4, and L5 show
20 the receiver pocket widths, with L1 having the narrowest pocket width and L5 having
21 the widest. Figure 15 shows that the yield decreases monotonically with frequency
22 owing to the rinsing dispersion effect of the Si microchips in pure water. In the low
23 rinse frequency region, the selectivity increases with increasing frequency owing to the
24 effect of the accumulation of Si microchips on the terrace into the pocket. In contrast, in

the high rinse frequency region, the selectivity decreases due to the dispersion of Si microchips on the terrace into pure water. This gives an optimum point for the selectivity at the rinse frequency and an optimum point for the overall yield, which is the product of the yield and selectivity. Figure 16 shows the selectivity and overall yield under the experimental conditions of a previous study [26] and the results of the present study. The horizontal axis represents the pocket width of the receiver piece, and the vertical axis represents the selectivity and overall yield. The results showed that the selectivity increased from 48% to 68%, and the overall yield increased from 1.4% to 26.4% under the widest pocket width condition by setting the optimum rinse strength range compared to the previous study. Therefore, it is possible to maximize the yield by separating Si microchips and accumulating them on the receiver piece with the minimum required amount of etching solution and minimum required volume of the container. The rinsing of the receiver piece in pure water at an appropriate frequency suppressed the aggregation of Si microchips. It promoted their accumulation in the receiver pocket, improving selectivity and overall yield.

So far, we have studied Si microchips with a width of 2 μm , and similar studies were conducted for Si microchips with that of 0.8 μm and 10 μm . The respective results are shown in Figure 17 and Figure 19. In an experiment using 10 μm square Si microchips, as shown in Figure 17, it was found that an S close to 1 was obtained under conditions with a wide pocket width at an arbitrary rinse frequency. Comparing these results with those of experiments using 2 μm square Si microchips, it was found that the selectivity was relatively more significant. The reason for this increase in selectivity with increasing Si microchip size is the decrease in the specific surface area of Si

1 microchips. The specific surface area S_a is calculated as follows:

$$S_a = \frac{2L^2 + 4tL}{L^2 \times t} = \frac{2}{t} + \frac{4}{L} \quad (2)$$

2 where L is the length of one side of the Si microchip and t is the thickness of the Si
3 microchip. Figure 18 shows S_a as a function of the width of the Si microchips. As
4 observed in Figure 18, the use of 10 μm square Si microchips instead of 2 μm square Si
5 microchips resulted in a smaller S_a . A smaller S_a is thought to reduce the influence of
6 fluid resistance due to rinsing and thus decrease the mobility of the Si microchips. This
7 trend is believed to have enabled the effective integration of Si microchips into the
8 pocket, which was achieved by moving the microchips at a smaller distance.

9

10 Similar experimental results are shown in Figure 19 for a microchip width of
11 0.8 μm . As observed, both the yield and selectivity decreased significantly when the Si
12 microchip size was small. This trend is thought to be because the larger specific surface
13 area of the Si film is more strongly affected by the fluid resistance, and dispersion in the
14 rinse solution becomes dominant. In addition, it was confirmed that the selectivity
15 increased with an increase in the rinse frequency when the Si receiver pocket width was
16 small. This is an outstanding result that was not observed under the condition of a large
17 microchip size and is considered to indicate a change in the fluid self-accumulation
18 mechanism in devices with a microchip size of several hundred nanometers or smaller.
19 Therefore, when integrating devices using fluidic self-assembly technology, it is
20 important to keep in mind that larger microchips have smaller S_a , which means they are
21 subjected to less fluid resistance. On the other hand, when integrating microchips
22 smaller than a few hundred nanometers, S_a becomes larger, and not only the fluid
23 resistance but also the adhesion force derived from other external forces such as

1 electrostatic force, van der Waals force, or cross-linking force become larger. Therefore,
2 it is necessary to control the external force application properly and thus strictly control
3 the physical and chemical states of the integrated substrate surface.
4

5 Compared to the pick-and-place technique, the fluidic self-assembly method
6 lacks accuracy in terms of controlling the right-left and front-back orientation of
7 microchips integrated into receiver pieces. Therefore, further studies are required to
8 enhance the practical applicability of this technique. Exploring the use of asymmetric
9 microchips in various orientations, such as trapezoids [17], could be a valuable area for
10 investigation. Moreover, the implementation of circular microchips [23,24,26] holds
11 potential in addressing these specific requirements.
12
13

14 **Conclusions**

15 In this study, we investigated multiple technical methods for semiconductor
16 fluidic self-assembly to improve the assembly yield. First, we fabricated Si releaser
17 pieces from an SOI wafer and Si receiver pieces from a Si wafer. The Si microchips
18 were then separated from the Si releaser in the HF solution and transferred to a Si
19 receiver. The maximum deposition yield, which is the quality of the number of Si
20 microchips deposited onto the receiver piece to that of which is separated from a
21 releaser chip, exceeded 0.9 by extending the immersion time of the Si receiver chip and
22 reducing the volume of etching solution and beaker by which a Si microchips are
23 separated. In the high-yield condition, however, the Si microchips form aggregations
24 owing to the capillary force while the Si receiver is dried. Therefore, we rinsed the Si

1 receiver with Si microchip aggregations in pure water to add an external drag force. The
2 external drag force was found to prevent the Si microchips from forming aggregations
3 and prompt transfer to the Si receiver pockets. This led to a maximum deposition
4 selectivity of 0.69 and an overall yield of 0.26. Furthermore, we performed similar
5 experiments with various Si microchip sizes to statistically determine the effect of the Si
6 receiver chip rinse on the evaluation functions: deposition selectivity, yield, and overall
7 yield. The selectivity for Si microchips of 10 μm square was generally close to 1 at all
8 rinse frequencies tested.

9
10 On the other hand, the selectivity was generally low for 0.8 μm square Si
11 microchips and tended to increase with decreasing pocket width. Consequently, we
12 found that rinsing is effective for fluidic self-assembly of 10 μm square Si microchips,
13 and fluid self-accumulation of Si microchips of several hundred-nanometer squares may
14 have a different accumulation mechanism compared to that of larger microchips. When
15 integrating devices using fluidic self-assembly technology, it is important to keep in
16 mind that larger microchips have less fluid resistance owing to their smaller specific
17 surface areas. The smaller microchips are influenced by various external forces, not
18 only fluid resistance but also electrostatic force, van der Waals force, or cross-linking
19 force because of their larger specific surface areas. These results could be helpful in
20 integrating Si microchips with large-scale semiconductor devices.

21 22 23 **Acknowledgments**

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Conflict of Interest

The authors declare that they have no conflict of interest.

Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Table and Figure Captions

Table 1 Semiconductor materials, geometries, and dimensions of the microchips in representative studies on fluidic self-assembly.

Table 2 Experimental No. and experimental conditions for each experimental No.

Fig.1 Schematic flow diagram of the fabrication process of the releaser.

Fig. 2 Cross-sectional scanning electron microscope image of the releaser piece.

Fig.3 Schematic flow diagram of the fabrication process of the receiver.

Fig. 4 Schematic bird's-eye view and cross-sectional view of the Si receiver.

Fig. 5 Plane-view scanning electron microscope images of the receiver piece.

Fig.6 Schematic flow diagram of the experimental process of fluidic self-assembly.

Fig. 7 Dependence of the deposition selectivity S and the overall yield YS on the width of the receiver pockets in our previous study [26].

Fig. 8 Yield plots for various etching solution and beaker size volumes versus

immersion time.

Fig. 9 Bird's-eye view of receiver chip after immersing for 20 hours and integrating Si microchips with 5 ml beaker and 0.9 ml etching solution.

Fig. 10 Presumable schematic flow of forming aggregates of the Si microchips.

Fig. 11 Bird's-eye view of receiver piece after RCA cleaning and integration of Si microchips.

Fig. 12 schematic diagram of the external force applied to the Si microchips on the receiver piece by shaking the receiver piece in the liquid.

Fig. 13 Bird's-eye view of the receiver piece after rinsing at 0 min^{-1} .

Fig. 14 Bird's-eye view of the receiver piece after rinsing at 75 min^{-1} .

Fig. 15 Correspondence between rinse frequency and various evaluation functions; the yield Y , the selectivity S and the overall yield YS , for the Si microchip with width of $2 \mu\text{m}$.

Fig. 16 Comparison of S and YS between our previous [26] and present studies.

1

2 Fig. 17 Correspondence between rinse frequency and various evaluation functions for
3 the Si microchip with width of 10 μm .

4

5 Fig. 18 Relation between width of Si microchips and specific surface area.

6

7 Fig. 19 Correspondence between rinse frequency and various evaluation functions for
8 the Si microchip with width of 0.8 μm .

9

10

1 **Tables and Figures**

2

Authors	Material	Geometry	Width [μm]	Thickness [μm]
Tu <i>et al.</i> ^[17]	GaAs	trapezoidal	40	10
Jacobs <i>et al.</i> ^[20]	GaAs	square	280	280
Srinivasan <i>et al.</i> ^[21]	Si	hexagonal	200	20
Chung <i>et al.</i> ^[23]	Si	circular	100	20
Park <i>et al.</i> ^[24]	Si	circular	2000	100
This work	Si	square	0.8, 2, 10	0.2

3

4 **Table 1**

5

1

No.	Volume of beaker V_B [ml]	Bottom area of beaker S_B [cm ²]	Volume of etching solution V_L [ml]
(1)	5	2.5	0.9
(2)	30	8.6	10
(3)	100	22.1	10
(4)	100	22.1	50

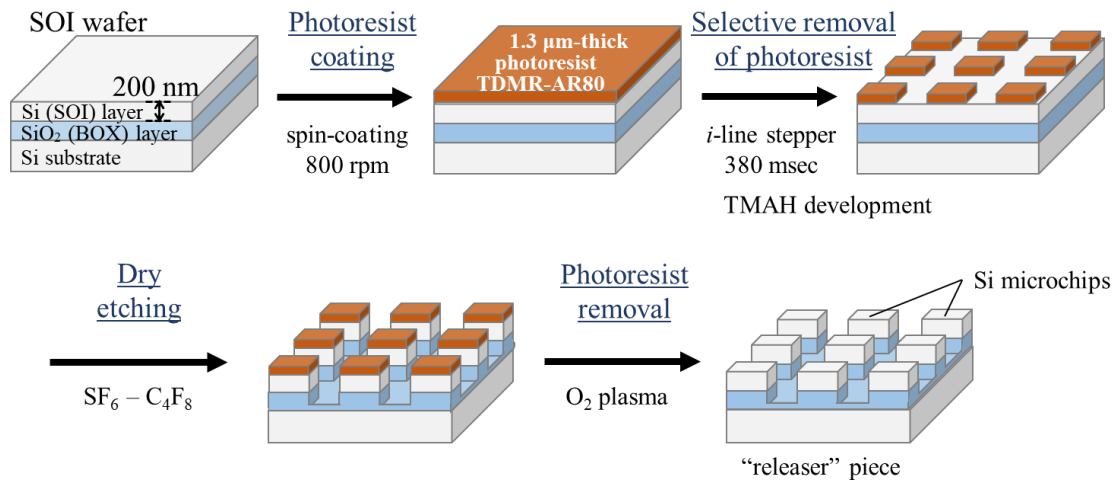
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3 Table 2

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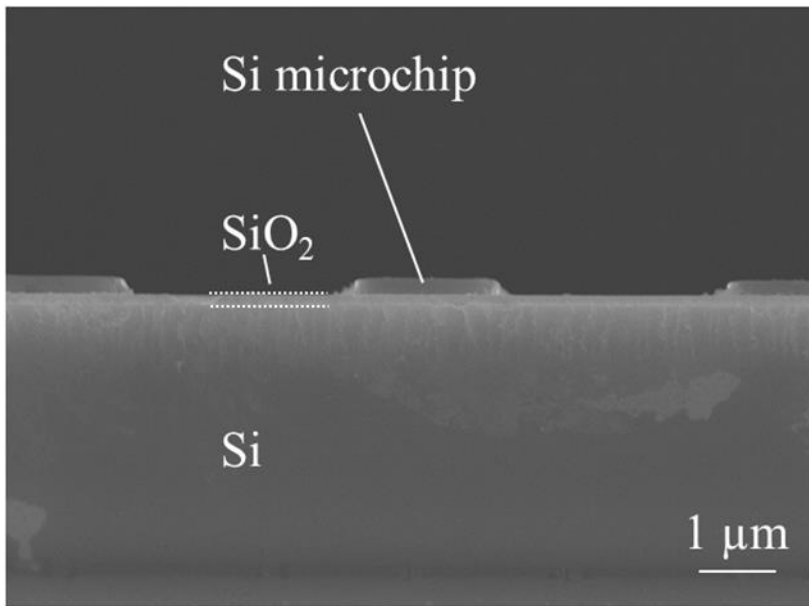
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5 Fig.1

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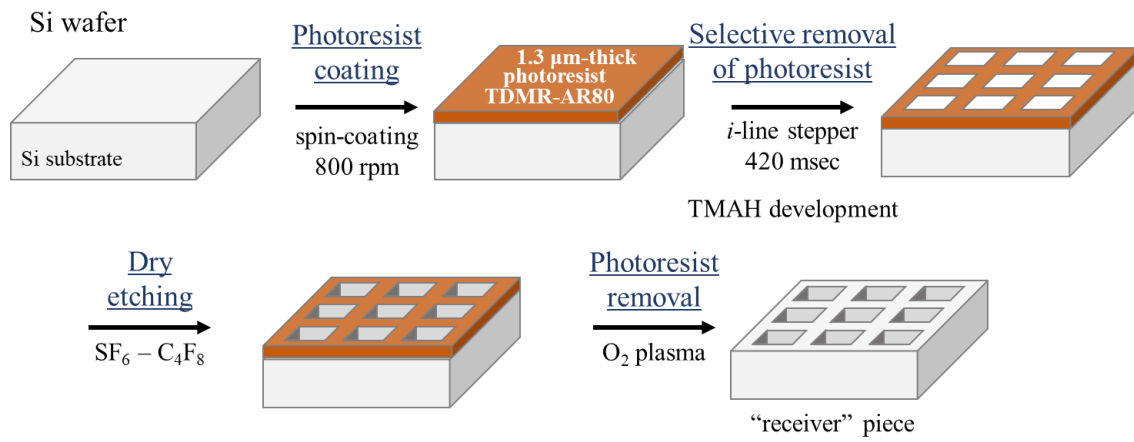
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4 Fig.2

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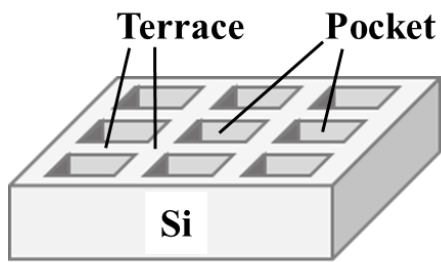
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4 Fig.3

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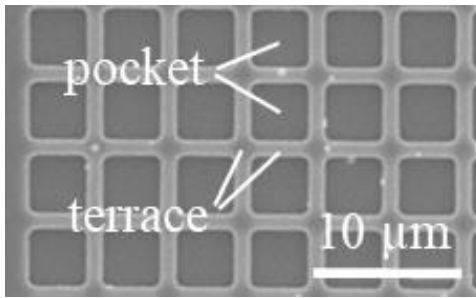
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4 Fig.4

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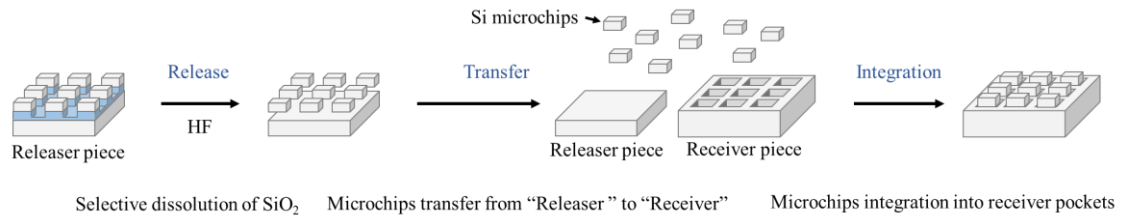
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4 Fig.5

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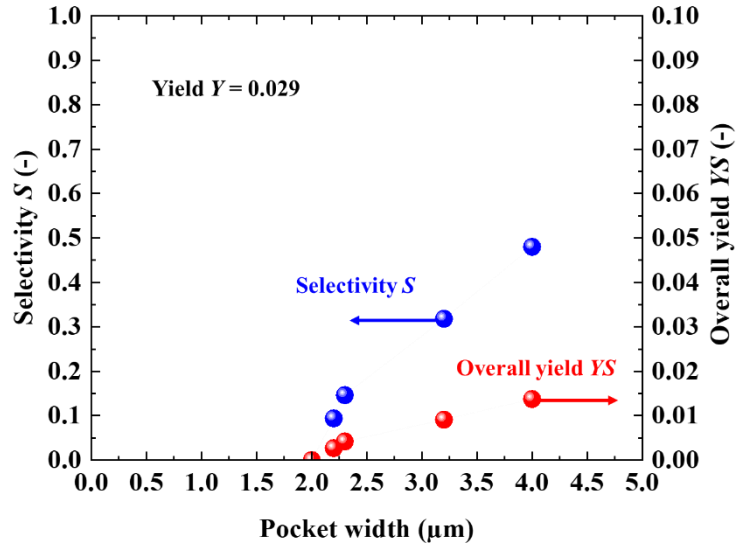
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4 Fig.6

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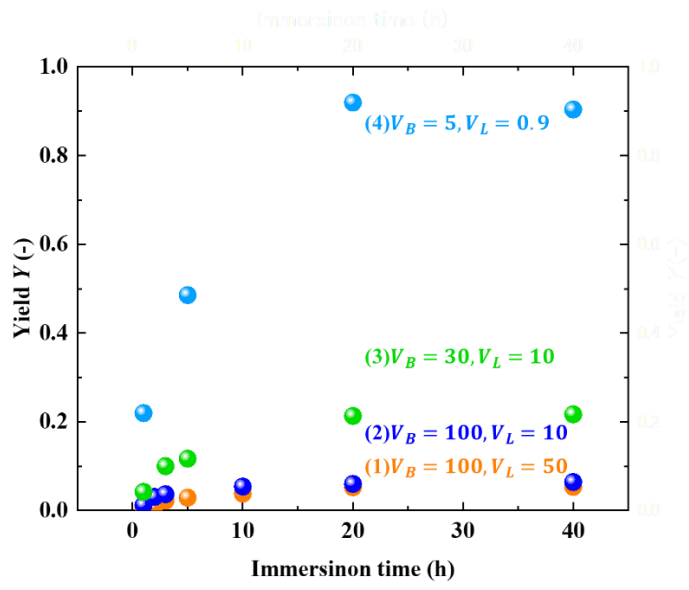
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4 Fig.7

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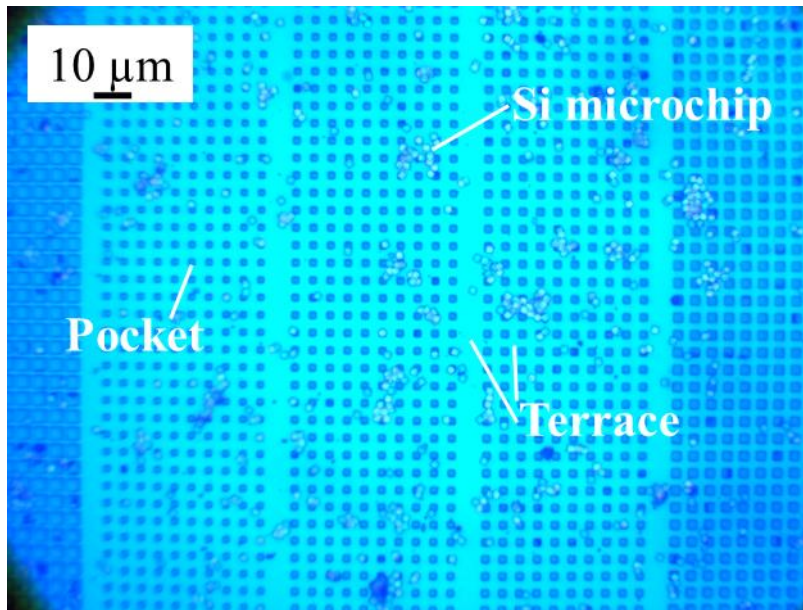
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4 Fig.8

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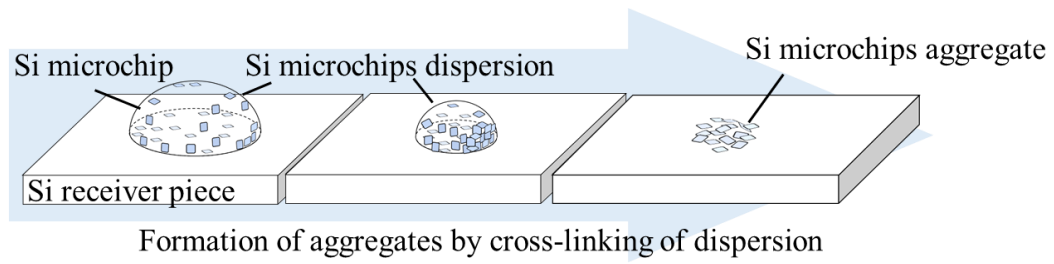
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4 Fig.9

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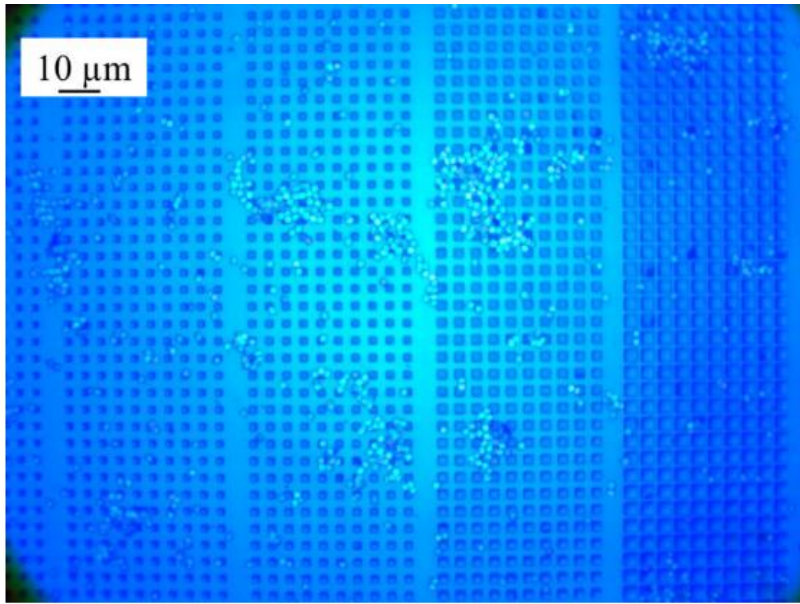
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4 Fig.10

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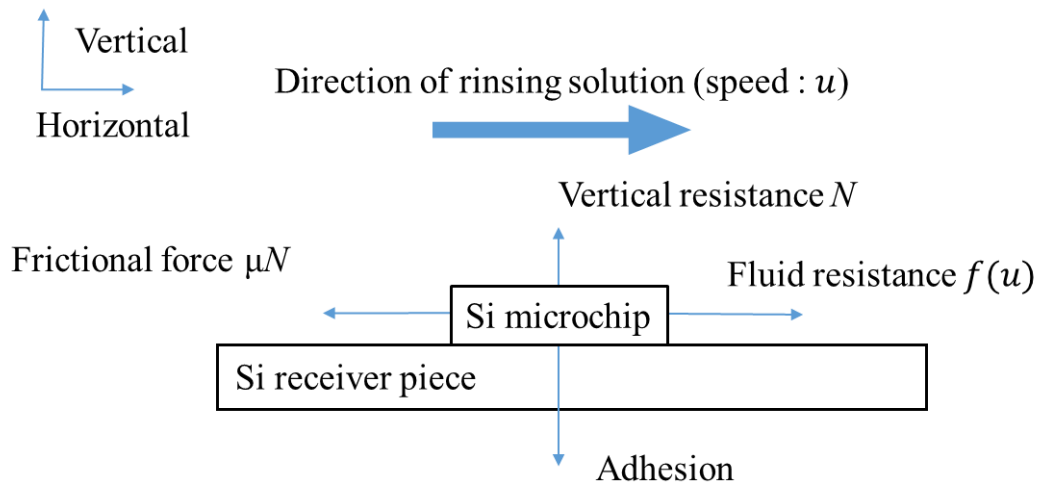
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4 Fig.11

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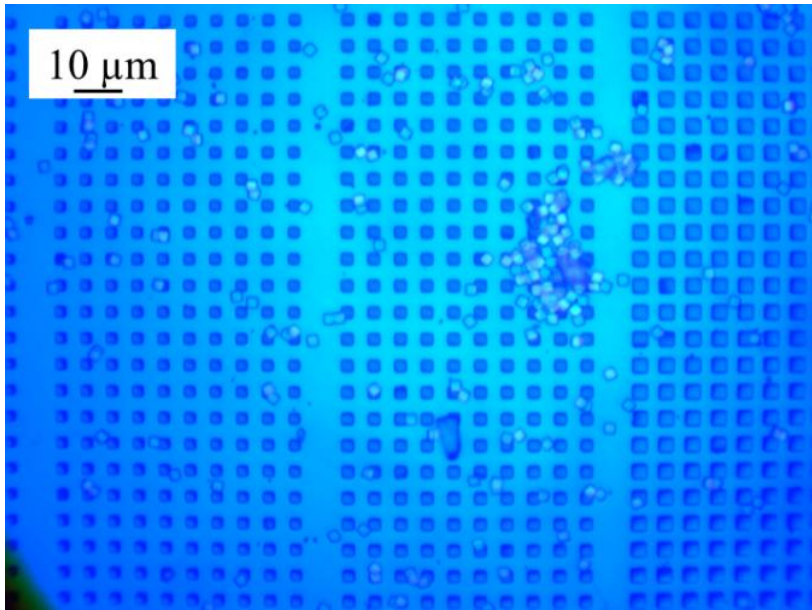
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4 Fig.12

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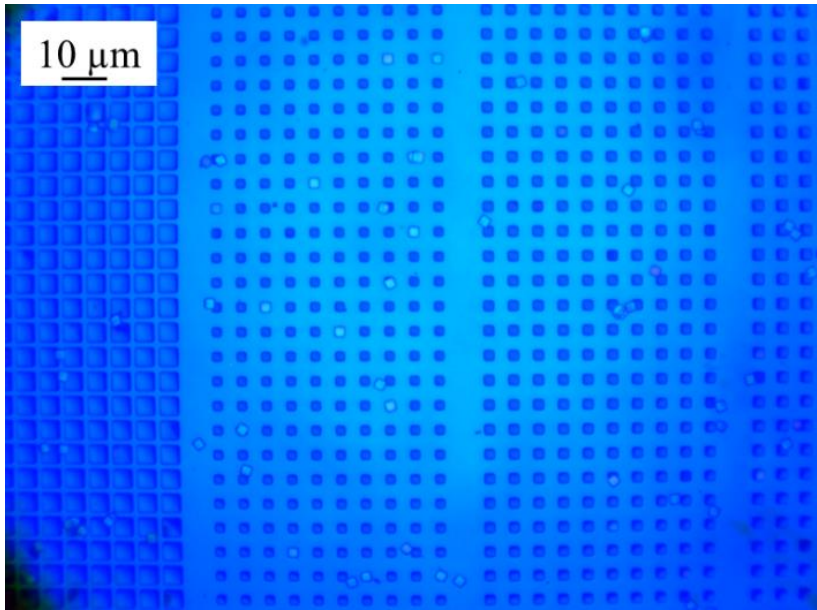
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4 Fig.13

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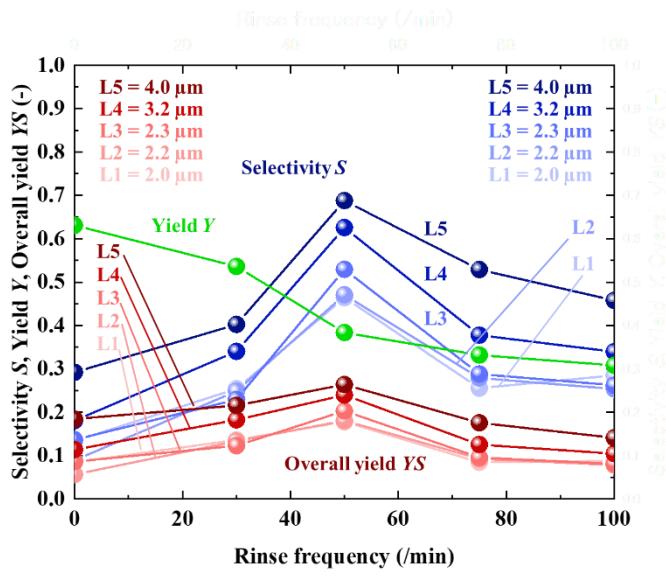
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4 Fig.14

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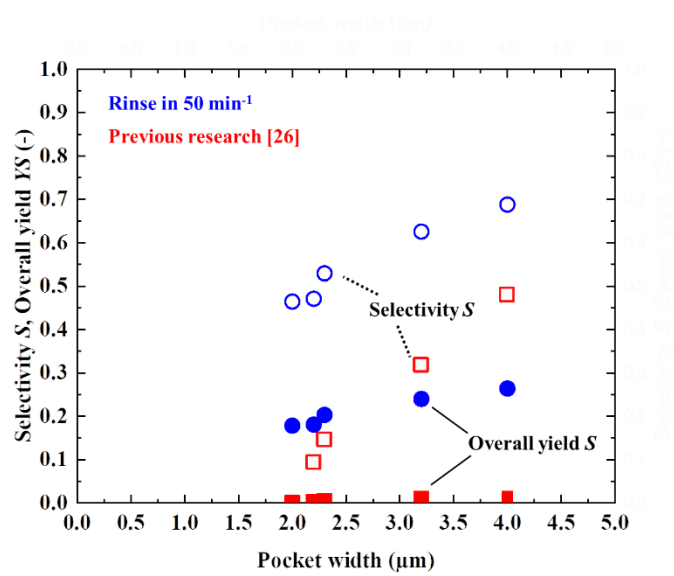
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4 Fig.15

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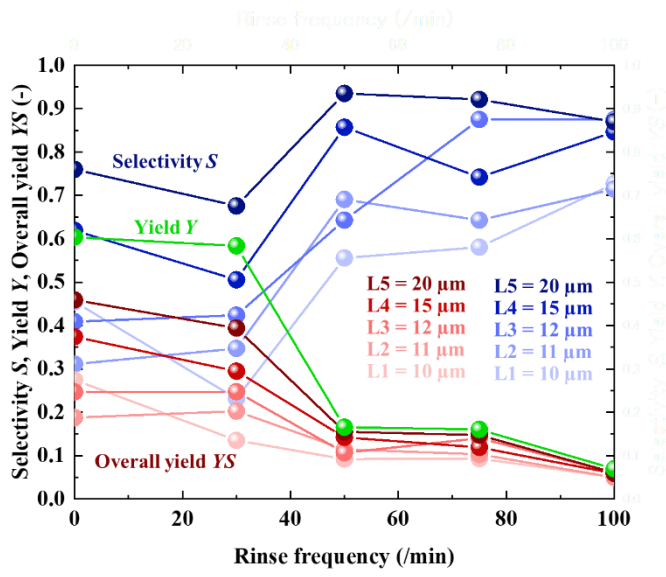
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4 Fig.16

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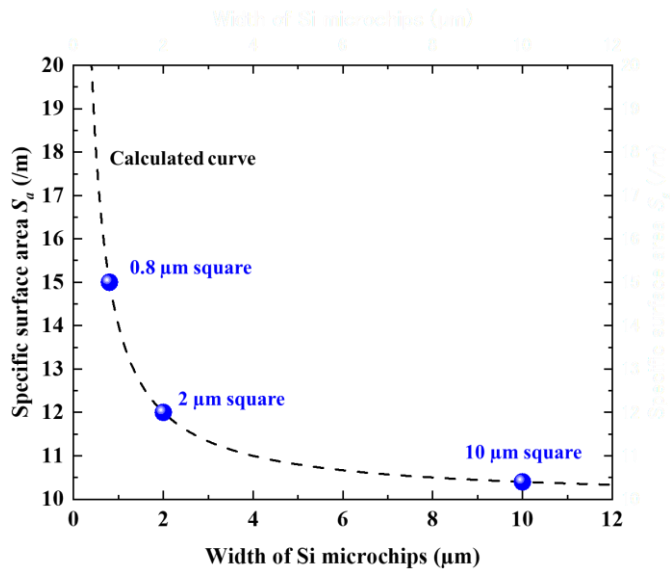
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4 Fig.17

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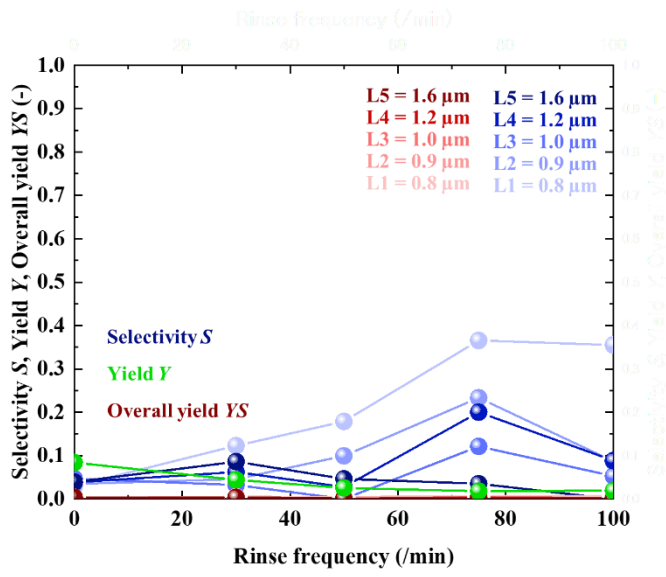
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4 Fig.18

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4 Fig.19

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