

1 **Small surface potential fluctuation near the valence band edge at nitrided** 2 **4H-SiC(0001)/SiO₂ interfaces**

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7 Interface states near the valence band edge at a nitrided 4H-SiC(0001)/SiO₂ interface
8 were investigated by the conductance, C - ψ_S , and high-low methods. Consistent en-
9 ergy distribution of the interface state density was extracted by the conductance and
10 C - ψ_S methods. The interface state density at $E_V + 0.2$ eV is $3.9 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$,
11 which is comparable to that at $E_C - 0.2$ eV. The standard deviation of the surface po-
12 tential fluctuation obtained by the conductance method is as small as 3–13 meV near
13 the valence band edge, which is significantly smaller than that near the conduction
14 band edge (~ 100 meV). This finding indicates that the scattering caused by the sur-
15 face potential fluctuation is much smaller in SiC p-channel metal-oxide-semiconductor
16 field-effect transistors (MOSFETs) than in n-channel MOSFETs, which would be one
17 of the reasons for the relatively high mobility in SiC p-channel MOSFETs.

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Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) are commercially available as high-performance power devices possessing low on-resistance beyond Si unipolar limit.^{1,2} In addition, they have attracted much attention for high-temperature complementary MOS (CMOS) integrated circuits (ICs) and monolithic power ICs.³⁻⁷ In the SiC MOS community, SiC/SiO₂ interface states near the conduction band edge (E_C) have been extensively investigated⁸⁻¹³ because the high-density interface states significantly decrease channel mobility in SiC power (n-channel) MOSFETs. As a result, an accurate energy distribution of the interface state density (D_{it}) near E_C at nitrided SiC/SiO₂ interfaces has been determined.^{14,15} On the other hand, studies on the interface states near the valence band edge (E_V), which affect mobility in SiC p-channel MOSFETs, have been still limited at the present stage.

So far, the energy distribution of D_{it} near E_V at nitrided SiC MOS interfaces has been extracted by the high-low method,^{16,17} $C-\psi_S$ method,¹⁸ and a method based on subthreshold characteristics of MOSFETs.¹⁹ However, the obtained D_{it} near E_V would not be very accurate due to a problem originating from the extraction process of each technique. It is known that at SiC/SiO₂ interfaces, the high-low method usually underestimates D_{it} near E_C because a significant part of the interface states can respond to the high probe frequencies, such as 100 k and 1 MHz,¹⁴ and the interface states have a large time constant dispersion.²⁰ As for the $C-\psi_S$ method, which can, in principle, detect all interface states, a small error in determining the surface potential at a given gate voltage causes a large underestimation or overestimation of D_{it} .²¹ In the case of the subthreshold-based method, although relatively accurate D_{it} can be extracted from subthreshold swings, it is difficult to determine the energy levels of the extracted D_{it} .

The conductance method is one of the most powerful techniques to characterize interface states because of its superior detection limit of D_{it} ($\sim 10^9$ cm⁻²eV⁻¹).²² In addition, this method can extract not only D_{it} but also the time constant of carrier emission from the interface states and standard deviation of the surface potential fluctuation. Recently, Y. Karamoto et al. applied this method to investigate the interface properties of a p-type SiC/SiO₂ structure formed by dry oxidation.²³ Therefore, in this study, the interface states near E_V at nitrided SiC/SiO₂ interfaces are investigated by the conductance method in addition to the high-low and $C-\psi_S$ methods. It turned out that the surface potential fluctuation near E_V is extremely small.

MOS capacitors were fabricated on a p-type epilayer grown on a p-type 4H-SiC (0001) substrate. The acceptor concentration of the epilayer was $1 \times 10^{15} \text{ cm}^{-3}$. Al⁺ implantation was conducted from the backside of the substrate at 300°C to form a p⁺ region with a density of $5 \times 10^{19} \text{ cm}^{-3}$, followed by post-implantation annealing at 1750°C for 20 min. The gate oxide was formed by dry oxidation at 1300°C for 20 min and subsequently annealed in NO²⁴ at 1250°C for 70 min, resulting in an oxide thickness of 37 nm. The backside ohmic electrodes were Ti/Al/Ni annealed at 1000°C. Finally, the gate electrodes were formed by Al deposition. Note that a correction process described in Ref. 23 and 25 was conducted in the conductance, high-low, and C - ψ_S methods to minimize the influence of the series resistance consisting of the p-type epilayer and substrate. The oxide capacitance used in all methods was extracted at a gate voltage of -10 V in the accumulation region.

Figure 1 shows the capacitance-voltage (C - V) characteristics for the fabricated p-type MOS capacitor, where the voltage sweep time was 100 s (sweep rate: 0.1 V/s). The ideal C - V curve is also shown for comparison. A frequency dispersion was observed due to the presence of interface states, the density of which is discussed later. The density of effective fixed charges was $+1.3 \times 10^{12} \text{ cm}^{-2}$, as extracted from the flatband voltage shift of -2.3 V .

Figure 2 depicts the interface-state conductance (G_{it}) as a function of the frequency (f) at various trap levels ($E_T - E_V$). Here, $E_T - E_V$ was determined using a high-frequency $1/(C_d + C_{it})^2 - \psi_S$ plot,¹¹ where C_d , C_{it} , and ψ_S are the depletion capacitance of a semiconductor, interface-state capacitance, and surface potential, respectively. Note that the frequency sweep time of G_{it} - f characteristics at each voltage was approximately 9 min. The peak conductance increases as $E_T - E_V$ decreases from 0.47 to 0.25 eV, reflecting an increase in D_{it} near E_V . The experimental G_{it} (symbols) were fitted well by the following equation:²²

$$\frac{G_{it}}{\omega} = q^2 S D_{it} \int_{-\infty}^{+\infty} \frac{\ln[1 + \{\omega \tau_{it} \exp(\eta)\}^2]}{2\omega \tau_{it} \exp(\eta)} \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{\eta^2}{2\sigma^2}\right) d\eta, \quad (1)$$

where ω is the angular frequency, q is the elementary charge, S is the gate electrode area, τ_{it} is the time constant of hole emission from the interface states, and σ is the standard deviation of the surface potential fluctuation. Here, D_{it} , τ_{it} , and σ are the fitting parameters. Note that a slight difference between the experimental and fitting results was observed at low frequencies (1 k–10 kHz), which may originate from near-interface traps in the oxide.^{23,26} τ_{it}

gives the capture cross-section of the interface states (σ_{it}), given by²⁷

$$\sigma_{it} = \frac{1}{\tau_{it} v_{th} N_V} \exp \left(\frac{E_T - E_V}{kT} \right), \quad (2)$$

where v_{th} is the thermal velocity of holes (1.2×10^7 cm/s at 300 K), N_V is the effective density of states in the valence band (2.2×10^{19} cm⁻³), k is the Boltzmann constant, and T is the absolute temperature. Figure 3(a) plots the time constant as a function of $E_T - E_V$. Note that the time constant generally become shorter for the interface states closer to the band edge because of fast response due to a smaller energy gap between the band edge and interface states. In fact, in p-type SiC MOS structures formed by dry oxidation, the time constant decreases near E_V .²³ However, the obtained time constant monotonically increases from 2.4×10^{-7} to 1.0×10^{-6} s when the trap level approaches E_V , corresponding to the shift of conductance peak to lower frequencies in Fig. 2. Since the time constant is determined by the trap level and capture cross-section of interface states, the different energy distribution of time constant between the as-oxidized and nitrided interfaces should be discussed taking account of the capture cross-section. Figure 3(b) plots the capture cross-section of interface states as a function of $E_T - E_V$. The energy distribution of the capture cross-section at the nitrided interface is stronger than that at the as-oxidized interface. Considering the different processes of gate oxide formation, NO annealing may cause a stronger energy distribution of capture cross-section of interface states, thereby the longer time constant near E_V at the nitrided interface.

Figure 4 shows the G_{it} - f curve fitting with various standard deviations of the surface potential fluctuation ($\sigma = 0.1, 0.5, 1$, and 4) at $E_T - E_V = 0.25$ eV. The calculated curves with $\sigma = 0.1$ and 0.5 fitted the experimental G_{it} - f curve well, and similar results were also obtained for the G_{it} - f curves at other $E_T - E_V$. In contrast, the calculated curves with $\sigma = 1$ and 4 distinctly showed broader peaks compared to the experimental results. Note that these results were obtained reproducibly for several MOS capacitors. Thus, the standard deviation of the surface potential fluctuation is determined to be in the range of 0.1 – 0.5 (3–13 meV) near the valence band edge at the nitrided interface. This surface potential fluctuation is much smaller than $\sigma = 4$ (about 100 meV) near the conduction band edge,^{11,28} indicating a relatively uniform surface potential near E_V . It has been reported that the σ near E_V is approximately 1.5 at the as-oxidized SiC/SiO₂ interface,²³ which is larger

than the σ near E_V of 0.1–0.5 at the nitrided interface. Since the density of effective fixed charges (Q_{eff}) at the as-oxidized interface ($+1.2 \times 10^{13} \text{ cm}^{-2}$) is much higher than that at the nitrided interface ($+1.3 \times 10^{12} \text{ cm}^{-2}$), the difference in σ near E_V between as-oxidized and nitrided interfaces may arise from the very different Q_{eff} depending on the final thermal treatment.

Figure 5 depicts the energy distribution of D_{it} near E_V extracted by the high-low, $C-\psi_S$, and conductance methods. The D_{it} near E_C extracted by the $C-\psi_S$ method¹⁴ is also shown in Fig. 5 for comparison. The D_{it} near E_V extracted by the high-low method is much lower than that extracted by the $C-\psi_S$ and conductance methods, indicating that the high-low method underestimates the D_{it} near E_V as expected. On the other hand, the $C-\psi_S$ and conductance methods extracted a similar D_{it} distribution near E_V . Moreover, this D_{it} distribution is close to that extracted from the subthreshold swings (SS) of SiC p-channel MOSFETs reported by the authors' group.¹⁹ Therefore, an accurate energy distribution of D_{it} near E_V could be obtained at the nitrided SiC/SiO₂ interface. It was found that the D_{it} near E_V exponentially increases from $2.8 \times 10^{11} (E_V + 0.5 \text{ eV})$ to $3.9 \times 10^{12} (E_V + 0.2 \text{ eV}) \text{ cm}^{-2}\text{eV}^{-1}$ when the trap level approach E_V . In addition, at 0.2 eV from the band edges, the D_{it} near E_V is comparable to that near E_C .

In SiC n-channel MOSFETs, the Hall mobility in the inversion layer ($\sim 100 \text{ cm}^2/\text{Vs}$) is only 10% of the bulk mobility ($1020 \text{ cm}^2/\text{Vs}$ ²⁵), whereas the drift mobility in Si MOSFETs is approximately 30% or higher of the bulk mobility.²⁹ The low drift mobility in SiC n-channel MOSFETs is likely attributed to strong Coulomb-like scattering.^{30–35} In contrast, the authors' group reported that such Coulomb-like scattering would not be significant in SiC p-channel MOSFETs.^{19,36} Since the Coulomb-limited mobility in Si MOSFETs is severely affected by the surface potential fluctuation and can be described as a universal line proportional to σ^{-2} ,³⁷ the present result supports that Coulomb-like scattering (or scattering caused by the surface potential fluctuation) is significantly stronger in SiC n-channel MOSFETs ($\sigma \approx 4$) but weaker in SiC p-channel MOSFETs ($\sigma = 0.1–0.5$). Note that one of the possible origins of the large surface potential fluctuation near E_C may be the conduction band fluctuation. The atomic-level roughness at the 4H-SiC(0001)/SiO₂ interface may induce conduction band fluctuation due to the peculiar stacking sequence of 4H-SiC but does not induce valence band fluctuation, which has been suggested by the first principle calculation.³⁸

In summary, the authors investigated 4H-SiC(0001)/SiO₂ interface states near E_V by the conductance, C - ψ_S , and high-low methods. The accurate energy distribution of D_{it} near E_V was obtained at the nitrided SiC/SiO₂ interface by the conductance and C - ψ_S methods. The D_{it} near E_V rises to $3.9 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ at $E_V + 0.2 \text{ eV}$, which is almost the same as that near E_C . The conductance method revealed that the standard deviation of the surface potential fluctuation is 3–13 meV near E_V , which is remarkably smaller than that near E_C (about 100 meV). It is expected that the small potential fluctuation near E_V gives little influence on the mobility of SiC p-channel MOSFETs, while the large potential fluctuation near E_C would be one of the reasons for the low mobility in SiC n-channel MOSFETs. In other words, SiC p-channel MOSFETs would exhibit a higher ratio of the mobility in the inversion layer to that in bulk SiC, compared to SiC n-channel MOSFETs. In order to discuss the scattering caused by the surface potential fluctuation, it is important to conduct MOS-Hall effect measurements for SiC p-channel MOSFETs with different surface potential fluctuations.

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DATA AVAILABILITY STATEMENT

The data that supports the findings of this study are available within the article.

AUTHOR DECLARATIONS

The authors have no conflicts to disclose.

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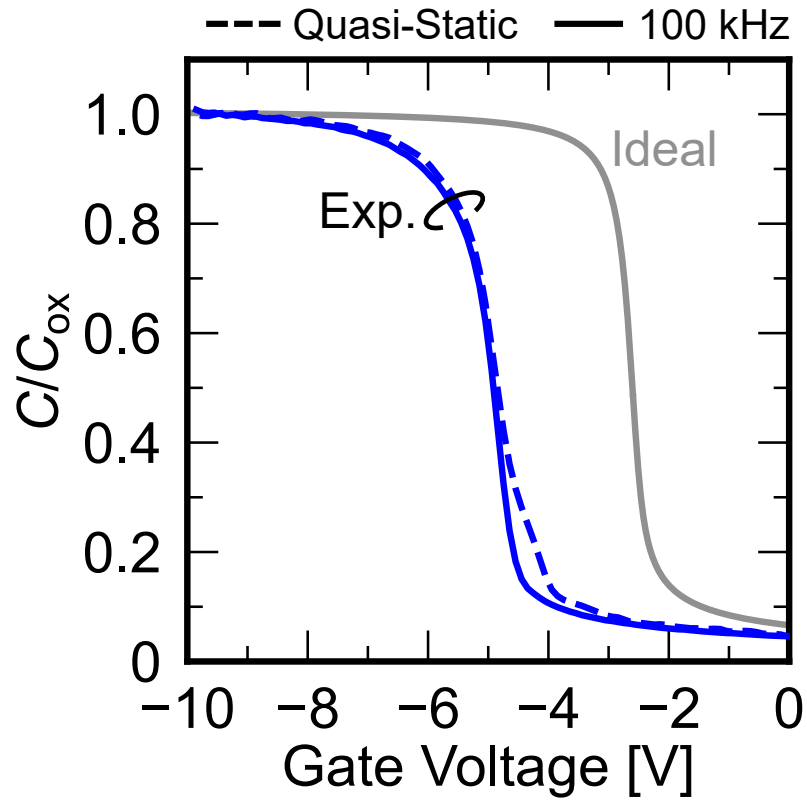


FIG. 1. Capacitance–voltage characteristics for the fabricated p-type SiC MOS capacitor.

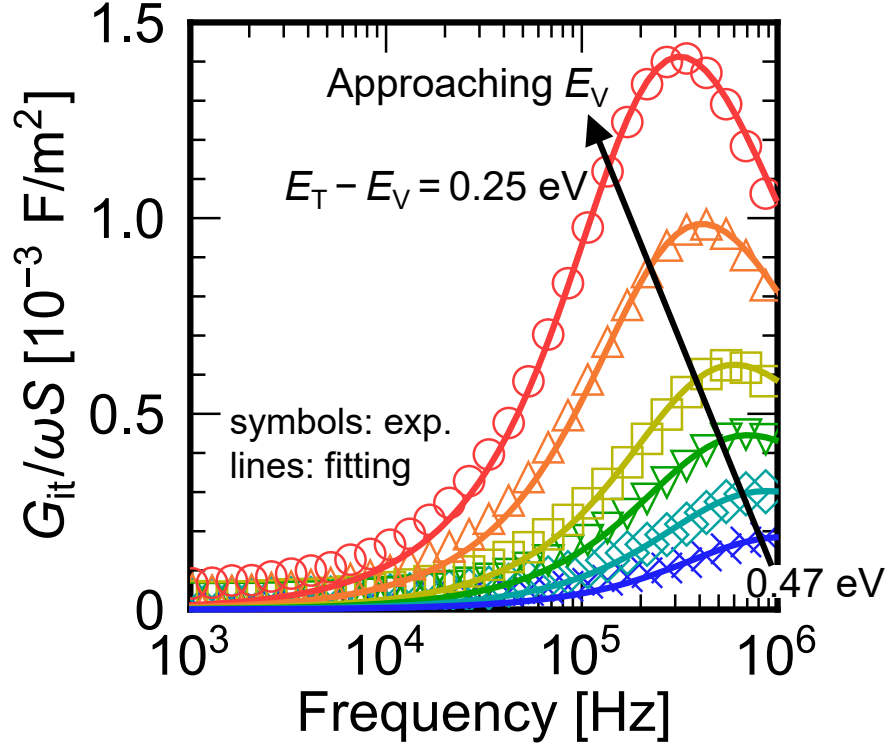


FIG. 2. Interface-state conductance–frequency (G_{it} – f) characteristics for the fabricated p-type SiC MOS capacitor at various trap levels ($E_T - E_V$). The symbols and lines denote the experimental and fitting results, respectively.

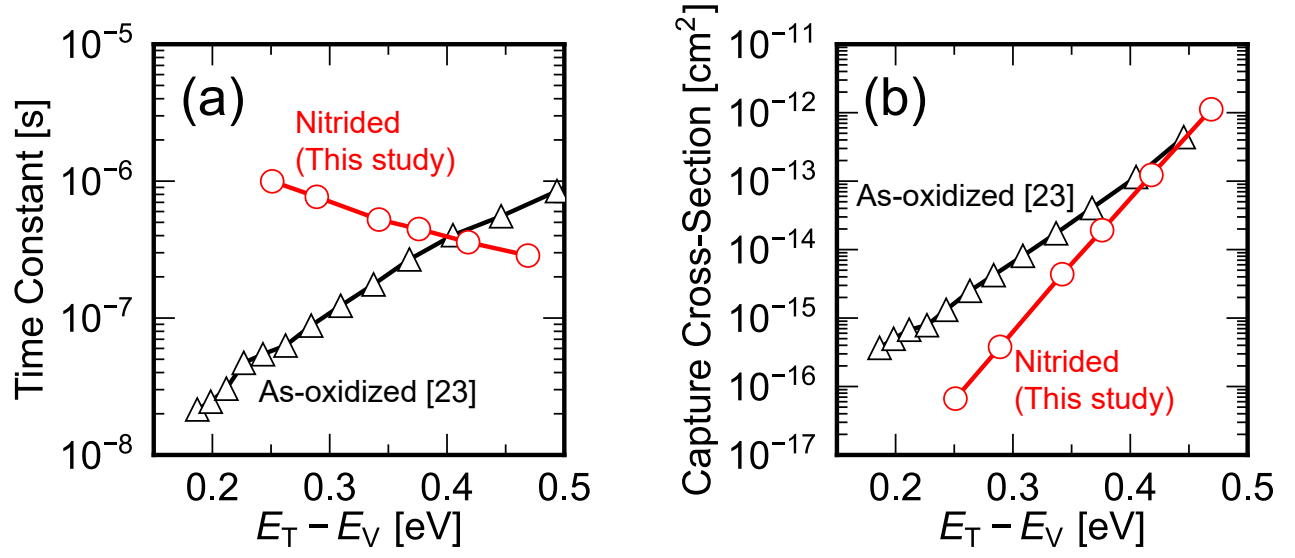


FIG. 3. (a) Time constant of hole emission from the interface states and (b) capture cross-section of the interface states near the valence band edge.

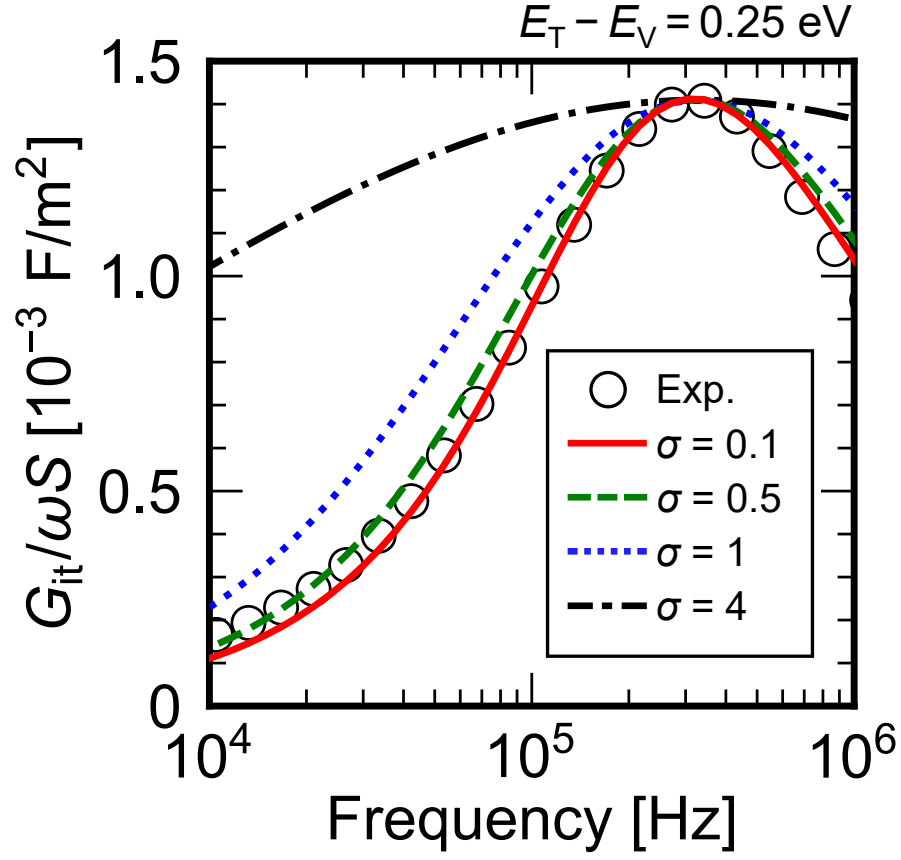


FIG. 4. Interface-state conductance–frequency (G_{it} – f) fitting results with various standard deviations of the surface potential fluctuation ($\sigma = 0.1, 0.5, 1$, and 4).

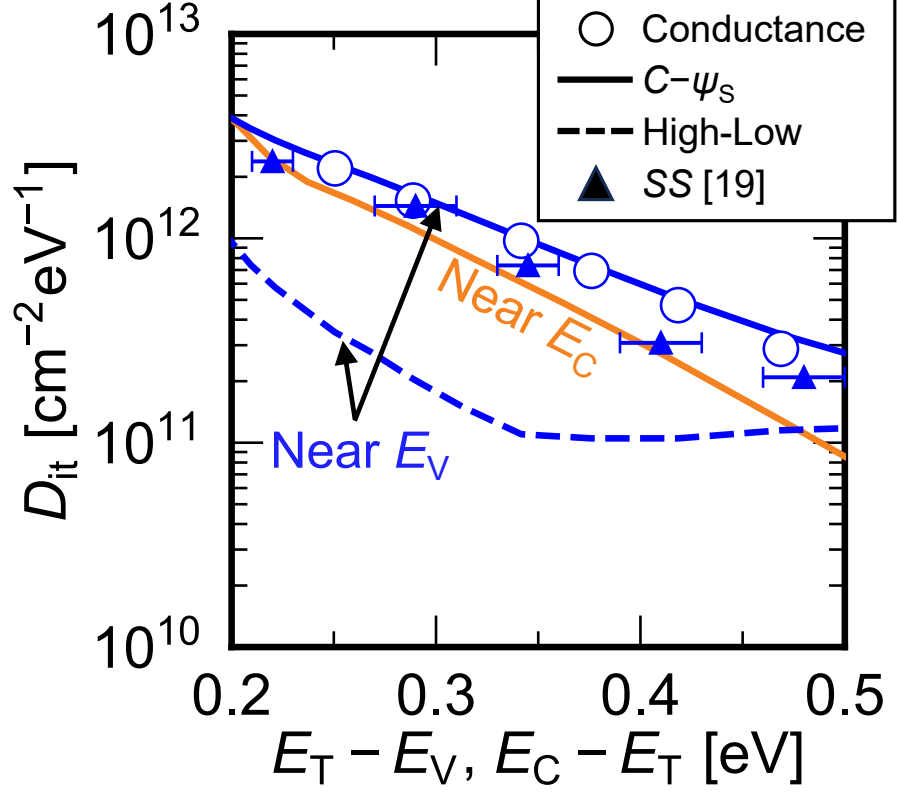


FIG. 5. Energy distribution of the interface state density (D_{it}) near the valence band edge (E_V) extracted by the high-low, $C-\psi_S$, and conductance methods. The energy distribution of D_{it} near the conduction band edge (E_C)¹⁴ is also shown for comparison.