

Analysis and Design of Radiation-Hardened Phase-Locked Loop

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Abstract

Technology scaling has driven the semiconductor industry for several decades. Scaling has resulted in faster and smaller semiconductor devices, however experienced an increase of radiation-induced errors in large scale integration (LSI) circuits. Phase-locked loops (PLLs) are embedded in LSI circuits for providing clocks to digital circuits. The radiation-induced errors on PLLs leads to whole LSI system's malfunction by change or lack of clock signals. To avoid malfunction on LSI systems, radiation-hardened PLLs (RH-PLLs) are necessary.

Radiation effect on PLL has to be examined prior to designing RH-PLL. The radiation effect on PLL depends on various factors, such as locations of radiation strikes, timings of radiation strikes, PLL performance parameters, and so on. Combinations of these factors cause many possibilities in the radiation effect. Investigation of all the possibilities leads to inefficiency in design cost and time. Thus, an analysis and models should be presented to systematically evaluate radiation effect on PLL.

This dissertation discusses an analysis of radiation effect on PLL and design of RH-PLL. The analysis of radiation effect on PLL provides categorization of radiation-induced errors for PLL's sub-circuits. The sub-circuits of PLLs are divided into digital sub-circuits and analog sub-circuits. In case of the digital sub-circuits, the radiation-induced errors for phase frequency detector (PFD), and Divider are categorized as incorrect pulse on UP/DN signals and deviation from reference clock, respectively. Voltage-controlled oscillator (VCO) and charge pump (CP) in the analog sub-circuits generate phase shift and voltage disturbance by radiation strikes. Also, the analysis identifies how the radiation-induced errors generate perturbation on PLL output clock. The radiation-induced errors causes two types of clock perturbation at PLL output, which are instant perturbation and gradual perturbation. The instant perturbation is attributed to the errors for the VCO and the CP and the gradual perturbation comes from the errors for the PFD and the Divider.

Based on the analysis, an analytical model and a behavioral model are presented to evaluate PLL's

vulnerability to radiation. The radiation vulnerability of PLL is evaluated using two metrics - phase displacement and recovery time. The analytical model is used to evaluate the phase displacement, which is a metric of the amount of the PLL clock perturbation. There are four equation sets in the analytical model, which are formulated from the categorized errors for the VCO, the CP, the PFD, and the Divider. The behavioral model enables to evaluate the recovery time, which is duration from clock perturbation caused by radiation strike to re-locking. The behavioral model is implemented with Verilog-A. To verify the presented models, their results were compared to the result by transistor-level simulation. In a PLL design, the discrepancies of the phase displacement and the recovery time were less than 0.56 radian and 80 ns, respectively. The behavior-based simulation attains to improve simulation speed, which is about 200 times faster than that of transistor-level simulation.

As a demonstration, a PLL designed in a 0.18 μm CMOS process was evaluated using the analytical model and the behavioral model. The evaluation results indicated the PFD as the most vulnerable part. A radiation strike at the PFD causes around 6 radian of the phase displacement and needs 800 ns to recover. This evaluation result was validated through an experimental testing, which was performed on a PLL fabricated in a 0.18 μm CMOS process with an alpha-particle source.

In this dissertation, an RH-PLL design that guarantee clock-perturbation immunity is proposed. The proposed technique can achieve an area-efficient RH-PLL due to the use of dual modular redundancy (DMR), in contrast to the triple modular redundancy (TMR) technique. The basic concept of the proposed RH-PLL is detecting errors and switching the output from one PLL having error to the other. Two detectors, which are clock detector and pulse detector, are developed to achieve high speed detection of the radiation-induced errors. The clock detector is for detecting errors originated from the analog sub-circuits and the pulse detector covers the errors coming from the digital sub-circuits. The proposed RH-PLL is fabricated in a 0.18 μm CMOS processes and verified by radiation-test. The clock perturbation immunity is confirmed in the experiment.

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Chapter 1

Introduction

1.1 Background

Large-scale integration (LSI) circuits are widely used for not only desktop environments but also space environments. In the space environment, radiation particles strike semiconductor devices such as transistors in LSI circuits, which leads to faults in the semiconductor devices. As a result, errors are induced in LSI circuits, which become the cause of malfunctions in electronics systems. Although the Earth and its immediate environment are protected by the atmosphere, the effects of radiation are not negligible and primary cosmic rays could create particles due to nuclear spallation reactions [1]. The created energetic particles, such as protons, neutrons, alpha particles, or other heavy ions, reach the Earth's surface. Neutrons are specifically addressed as the main concern that causes malfunctions in electronics systems because the energy spectrum of neutrons is very broad from a few electronvolts (eVs) to tera-electronvolts (TeV) even at sea level. The terrestrial neutron flux at sea level is about 20 neutrons/cm²/hour and that at 2000 m is five times higher than that at sea level [2]. The terrestrial particles could also generate radiation-induced errors in LSI circuits.

1.1.1 Radiation-Induced Errors: Single Events

A radiation strike of high-energy ionized particles on semiconductor devices such as transistors generates electron-hole pairs in their substrates. These free carriers are then injected into the sources or drains of the transistors. The charge injection causes transient perturbations on the corresponding node

voltage, which is called ‘single event (SE)’ or ‘soft error’.

There are two primary mechanisms by which ionizing radiation releases charge in a semiconductor device: direct ionization by the incident particle itself and indirect ionization by secondary particles created by nuclear reactions between the incident particle and the struck device [3]. Figure 1.1 outlines these mechanisms. As we can see from Figure 1.1 (a), direct ionization occurs when an energetic charged particle passes through semiconductor material. It then frees electron-hole pairs along its path as it loses energy. However, sources of indirect ionization are protons and neutrons. As high-energy protons or neutrons enter the semiconductor lattice, they may undergo collisions with the target nucleus and nuclear reactions occur. Reaction products can deposit energy along their paths by direct ionization. Since these particles are much heavier than the original protons or neutrons, they deposit higher charge densities as they travel as seen in Figure 1.1 (b). Once a nuclear reaction has occurred, the charge deposition by secondary charged particles is the same as that from a directly ionizing heavy ion strike.

SE can generally be divided into two modes – single-event transients (SETs) and single-event upsets (SEUs). SETs are transient voltage perturbations due to SE on a particular node (Figure 1.2 (a)). SETs in a logic circuit may be propagated through a logic chain and captured by storage elements that terminates the logic path, such as latches or registers. The captured SETs therefore lead to errors in logic circuits. SEUs are a low-to-high or high-to-low voltage transitions at storage elements in logic circuits and they also results in flips of stored data in memories, such as static random access memories (SRAMs) and dynamic random access memories (DRAMs) (Figure 1.2 (b)). It is clear that both SEUs and SETs may cause erroneous information over all electronics systems.

1.1.2 SE Effect in Technology Scaling

In early days of LSI circuits, designers do not need to be concerned about SEs. SEs have become an issue in LSI circuit design since the technology scaling was started. A demand for low-cost and high-speed LSI circuits causes the technology scaling. In the 1960s, the SEs in LSI circuits were recognized and reported for the first time [4]. Reference [4] notices that semiconductor devices are shrunk to concern about SEs. Despite this notice, technology scaling began with Moore’s law that is the number of transistors on integrated circuits (ICs) doubles approximately every two years. As a result, SE effect in LSI circuits become more critical as the years go by.

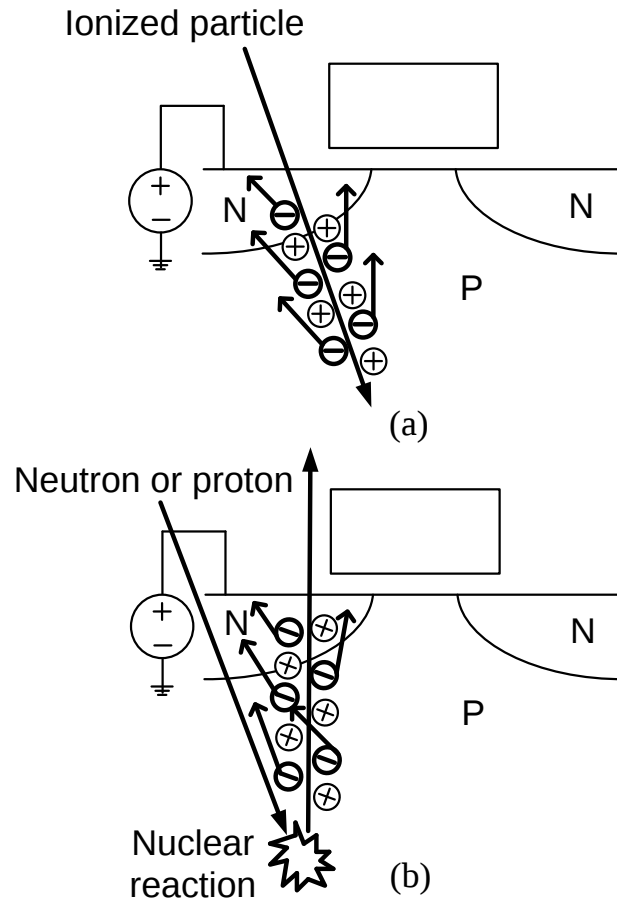


Figure 1.1: Mechanisms by (a) which ionized particle releases charge in semiconductor device (direct ionization) and that by (b) which proton or neutron generates electron-hole pairs by nuclear reaction (indirection ionization)

In the technology scaling, a decrease of nodal capacitance is the most important reason to aggravate SE effect. The decreased nodal capacitance results in an increase of radiation vulnerability by reducing ‘critical charge’, which is the minimum amount charge needed to change the state of a circuit node [5–7]. Reduction of the supply voltage also aggravate SE effect in LSI circuits [7, 8]. The technology scaling scenario keeps decreasing the supply voltage but constant of the threshold voltage. LSI circuits are operated in near-threshold voltage region. It means the amount of current in LSI circuits is not enough to cancel SE effect. Additionally, increasing the number of semiconductor devices per a chip leads to possibility of radiation strike that can creates errors [9, 10]. Reference [11] predicts soft error vulnerability increases about 40% per technology generation node. Therefore, the SE effect is considered as a critical problem in future LSI circuits.

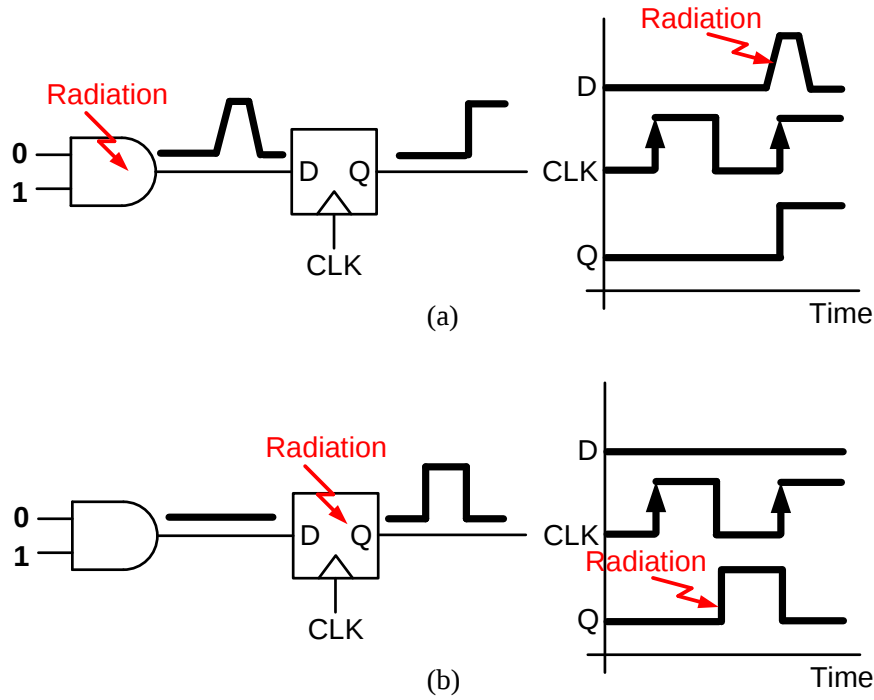


Figure 1.2: (a) SET at logic circuit is captured by storage element and (b) SEU at storage element causes data flip.

1.2 Motivation

Phase-locked loops (PLLs) are used for LSI circuits as a clock source. Figure 1.3 depicts a basic topology of PLLs consisting of a phase-frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO), and a divider. SEs lead to errors at sub-circuits composed of PLLs and they are observed as jitter at PLL output. This radiation-induced jitter is called ‘clock perturbation’ in this dissertation to distinguish it from the jitter caused by other sources. While SE on storage elements or logic elements only generates local errors, clock perturbation on PLLs propagates over all LSI circuits. This means radiation strikes on PLLs can induce malfunctions in complete electronics systems. Thus, radiation-hardened PLLs (RH-PLLs) are becoming more important.

1.2.1 Radiation Hardening by Process Technology

RH-PLLs have been reported since around 2000. The early RH-PLLs were designed with silicon on insulator (SOI) or silicon on sapphire (SOS) complementary metal-oxide-semiconductor (CMOS) technology [12] [13]. SOI and SOS were considered to be solutions to developing SE tolerant cir-

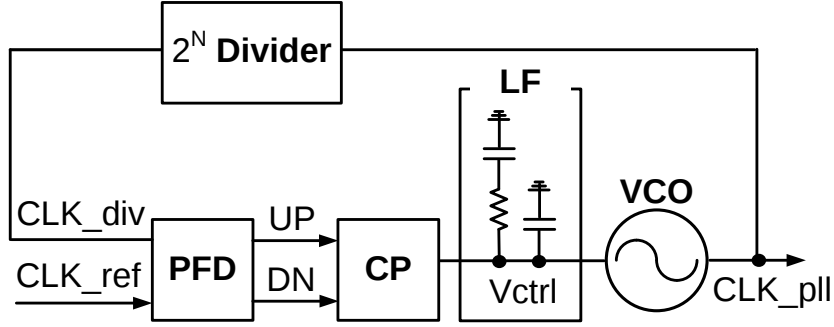


Figure 1.3: A basic topology of PLL

circuits [14–16]. However, design-based techniques are mainly required for radiation hardening for two reasons. The first reason is the high cost of the radiation-mitigated technologies [2]. Bulk CMOS technologies are still capturing a large proportion of the semiconductor industry due to their low manufacturing costs. The second reason is that the SE effect has only been alleviated on SOI and SOS technologies, but has not been completely solved [17, 18]. Almost all RH-PLLs reported after 2000 were achieved with design-based techniques even if they used the radiation-mitigated technologies [17, 19, 20]. Therefore, this dissertation focuses on radiation-hardened-by-design (RHBD) PLLs.

1.2.2 Radiation-Hardened-by-Design (RHBD) PLLs

The trade-off between cost and radiation-hardening should be considered in RHBD PLLs. A redundancy technique such as triple modular redundancy (TMR) is traditionally used for radiation-hardening. The redundancy technique is inefficient in power and area consumption because multiple replica circuits and a large voter are needed. The specifications of applications determine whether their design strategies will be oriented towards cost efficiency or high levels of reliability. Thus, the reported RHBD can be divided into two strategies - those for cost saving and those to attain high levels of reliability.

High-Reliability Strategies

High-reliability strategies completely protect PLLs from clock perturbations [21–24], where the easiest implementation is to adopt the TMR technique using three PLLs and a voter [23]. As previously mentioned, the TMR technique causes inefficiencies in area and power consumption. PLLs are achieved with radiation-hardened sub-circuits or components [21, 22, 24] to achieve efficiency.

Radiation-hardened digital components, especially inverters, NANDs, D-flipflops, had already been studied before necessity for RH-PLLs was recognized. Digital sub-circuits can be implemented with radiation-hardened digital components [22, 24]. However, protection for analog sub-circuits is unsolved. All-digital PLLs (ADPLLs) have been used as core PLLs [21]. Since all sub-circuits were composed of digital components, the TMR technique and radiation-hardened components were sufficient to accomplish RH-PLLs. Unfortunately, it is difficult to reduce jitter in non-radiation situations with ADPLLs. Thus, more design techniques are still required for various PLL structures.

Cost-Saving Strategies

The basic idea behind cost-saving strategies is to reduce the ‘recovery time’ from clock perturbations. Since PLLs are feedback systems, they return to locked conditions. The time from onset of clock perturbation to re-locking is called the ‘recovery time’. The time to recovery takes hundreds of clock cycles, which depends on several factors such as radiation environment and circuit design.

Partial-hardening techniques and a detection-correction technique have been reported [17, 25–28] to reduce the recovery time. The control voltage is monitored in the detection-correction technique [28]. Once a perturbation of the control voltage is detected, additional current sources charge or discharge capacitors of the LF referring to the detected the control voltage.

Partial-hardening is the most commonly used due to its simple design and efficiency in power and area overheads [17, 25–27]. The key idea behind the partial-hardening technique is to protect critical parts. It is, therefore, very important to find the critical parts in PLLs. The analog parts of VCOs and CPs have been addressed as critical parts through their simulation or experiment [17, 25–27, 29, 30]. However, the critical parts basically depend on PLL designs and processes. For example, the CP and its output node (V_{ctrl}) have been identified [25, 26] as critical parts. These PLLs have involved 700fF of LF capacitance. If the LF capacitance has a different value, disturbance on the V_{ctrl} would be changed. It means they have to repeat analysis to evaluate radiation vulnerability every time when they develop RH-PLLs. This brute-force analysis leads to inefficiency in design cost and time. Therefore, a method of systematically evaluating radiation effects is necessary.

There have been very few publications on methods of systematically evaluating radiation effects [31, 32]. A method of simulation was introduced that was a combination of behavioral models and transistor levels [31]. This work replaced sub-circuits of a PLL with behavioral models except for a

VCO. Radiation strikes at the VCO was only simulated and examined with a behavioral model of a PLL. However, it is still necessary to examine other sub-circuits, such as the CP, the PFD, and the divider. A generalized linear model to examine single transient propagation through PLLs has been proposed [32]. Main purpose is to be a performance indicator with respect to radiation hardening rather than to be an evaluation method. In addition, this model uses a first-order LF for modeling. Hence, examining radiation effects on PLLs having a second-order LF is remained.

1.3 Research Goal and Dissertation Overview

This dissertation has two research goals. The first goal is to present an analysis of radiation effect and models for evaluation of radiation vulnerability on PLLs. The evaluation of radiation vulnerability on PLLs should precede designing RH-PLLs. The radiation vulnerability on PLLs has many possibilities depending on various factors, such as locations of the radiation strikes, timings of radiation strikes, PLL performance parameters, and the deposition charge. All the possibilities have to be examined to evaluate the radiation vulnerability on PLLs. In conventional works, the most vulnerable parts were determined and protected to save the cost of RH-PLLs. Transistor-level simulations and experiments were used to evaluate radiation vulnerability and then determine the most vulnerable parts. However, investigating all the possibilities with transistor-level simulations and experiments causes inefficiency in design cost and time. Thus, an analysis and models should be presented to accomplish systematical evaluation of radiation vulnerability on PLLs. The second goal of this dissertation is proposal of an RH-PLL design to guarantee the high-reliability. The TMR technique has been used to design RH-PLL ensuring high-reliability. The issue of the TMR technique is area and power overhead in RH-PL design due to a large size of capacitors, which compose LFs. Since the LF may occupy over a half of the total PLL area, use of the TMR technique in PLL design leads to more serious area overhead than that in design using only transistors. Therefore, high-reliability design which is more area-efficient than the TMR-based RH-PLLs is necessary.

The following chapters discuss an analysis and modeling of radiation effect on PLL and an RH-PLL design to protect from radiation strike effect. Chapter 2 discuss a qualitative analysis of radiation effect on PLL. Radiation-induced errors for each sub-circuit and how the errors propagate to the PLL output clock is examined. As the examination result, categorization of radiation-induced errors is pro-

vided. Chapter 3 describes analytical modeling of phase displacement on PLL clock under radiation. The phase displacement is one metric of quantified radiation-induced clock perturbation. The analytical model of the phase displacement is formulated based on the categorized radiation-induced errors in Chapter 2. The result calculated by the model equation is verified through the comparison with the Simulation Program with Integrated Circuit Emphasis (SPICE) simulation result. Chapter 4 explains modeling of PLL's recovery behavior from radiation-induced perturbation. Behavioral models of radiation-induced errors are presented to evaluate the recovery time. Verilog-A is used to implement the behavioral model. Using the analytical model and the behavioral model, a conventional PLL design is evaluated. The evaluation result is validated through an experimental radiation test. Chapter 5 proposes an RH-PLL design that can ensure clock-perturbation immunity. This design is efficient in area consumption, compared to the TMR-based RH-PLL design. The proposed RH-PLL design is fabricated in a $0.18\ \mu\text{m}$ CMOS process and its measurement result is discussed. Finally, Chapter 6 summarizes the main contribution of this research work.

Chapter 2

Analysis of Radiation Effects on PLLs

2.1 Introduction

Radiation strikes leads to errors on PLLs. Types of the radiation-induced errors depends on locations of radiation strike and strike timings. Since PLL consists of several sub-circuits and deals with time-varying signals, the number of the error types is a large number that combine locations of radiation strike and strike timings. Thus, all possibilities of radiation strike should be examined and analyzed for categorization. Categorization enables to avoid investigation of all possibilities when radiation vulnerability on a PLL is evaluated. In addition, it is helpful to find the critical part on a PLL when a designer uses the partial-hardening technique to design a low-cost RH-PLL. The radiation-induced errors propagates to the PLL output and cause clock perturbation. Propagation mechanisms for categorized errors should be analyzed.

This chapter discusses the qualitative analysis of radiation-induced errors. The first part of this chapter describes the simulation set up for analysis. The second part presents types of radiation-induced errors and the categorization of the error types. Propagation mechanism of the errors to reach PLL output is identified based on the categorization. The results from analysis are used for modeling of vulnerability to radiation in a subsequent chapter.

Table 2.1: PLL performance characteristics during simulation.

Operating frequency range	30 – 520 MHz
Center frequency	400 MHz
Supply voltage	1.8 V
Cycle-to-cycle jitter	25 ps
Current consumption	1.8 mA (Average)

2.2 Simulation Set Up

A conventional low-jitter PLL designed with a $0.18\mu\text{m}$ CMOS process was used to examine the effects of radiation effect on PLLs. Figure 2.1 illustrates a PLL that was basically identical to that used by Maneatis [33] except that a 2^5 divider and a second-order LF were added. The LF consisted of $R = 10\text{ k}\Omega$, $C_1 = 18\text{ pF}$, and $C_2 = 1.8\text{ pF}$. The performance characteristics of the PLL are summarized in Table 2.1.

A transient current (I_{rad}) is used to emulate the injection charge caused by radiation strike. If an n^+ active region which may be a source or drain in an nMOSFET is being hit, electrons are collected into the n^+ source or drain. The current will thus be drawn from the node, which is called ‘nMOSFET-hit’ in this dissertation. Figure 2.2 (a) depicts a circuit simulation set-up of nMOSFET-hit using the transient current (I_{rad}). A current source to create the transient current (I_{rad}) is connected to the n^+ source or drain node which experiences a radiation strike. The transient current is modeled as follow [34, 35]:

$$I_{\text{rad}}(t) = \frac{2Q_{\text{DEP}}}{T\sqrt{\pi}} \sqrt{\frac{t}{T}} e^{-t/T} \quad (2.1)$$

where t is time, Q_{DEP} is deposited charge on the silicon when the radiation strike occurs, and T is a time constant that depends on the material, doping, and other factors. The value of T is 22 ps obtained from [36]. This model equation has been validated through experiments using silicon chips. Soft error rate (SER) of LSI circuits was predicted based on Equation (2.1) [34, 35]. The predicted result was compared to a experimental result that was obtained by proton-beam test [34, 35] and actual field test at high ground elevations [35]. The experimental result convinces the validation of Equation (2.1). Equation (2.1) has been used to study SE effect on LSI circuits [37–45]. Figure 2.2 (b) illustrates transient current curves of nMOSFET-hit when Q_{DEP} values are 50 fC, 100 fC, and 500fC, respectively. If a p^+ source or drain in a pMOSFET is being hit, holes are collected and hence the current will be

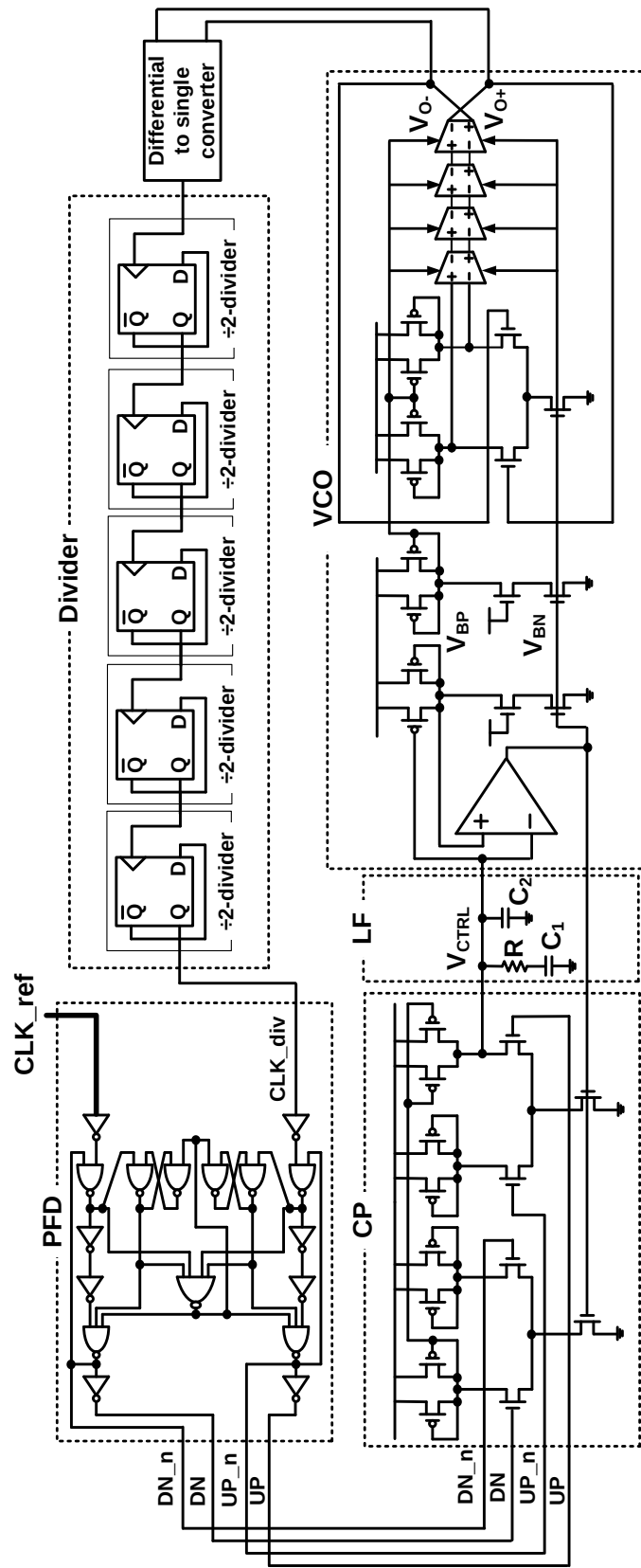


Figure 2.1: Schematic of conventional low-jitter PLL.

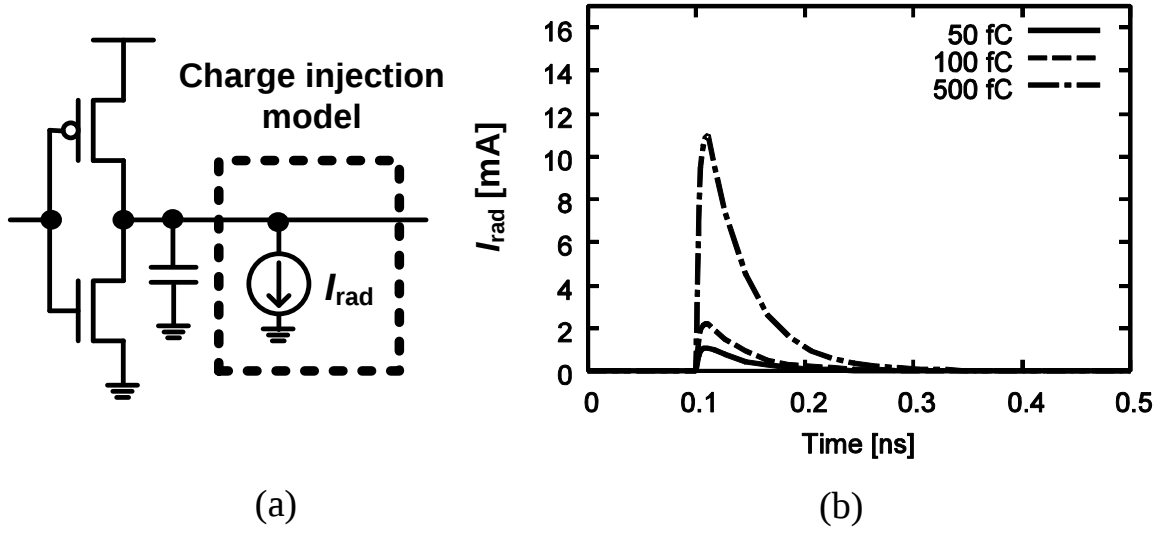


Figure 2.2: (a) Circuit simulation set-up of nMOSFET-hit using charge injection model (I_{rad}) and (b) transient current curves of nMOSFET-hit when Q_{DEP} values are 50 fC, 100 fC, and 500fC.

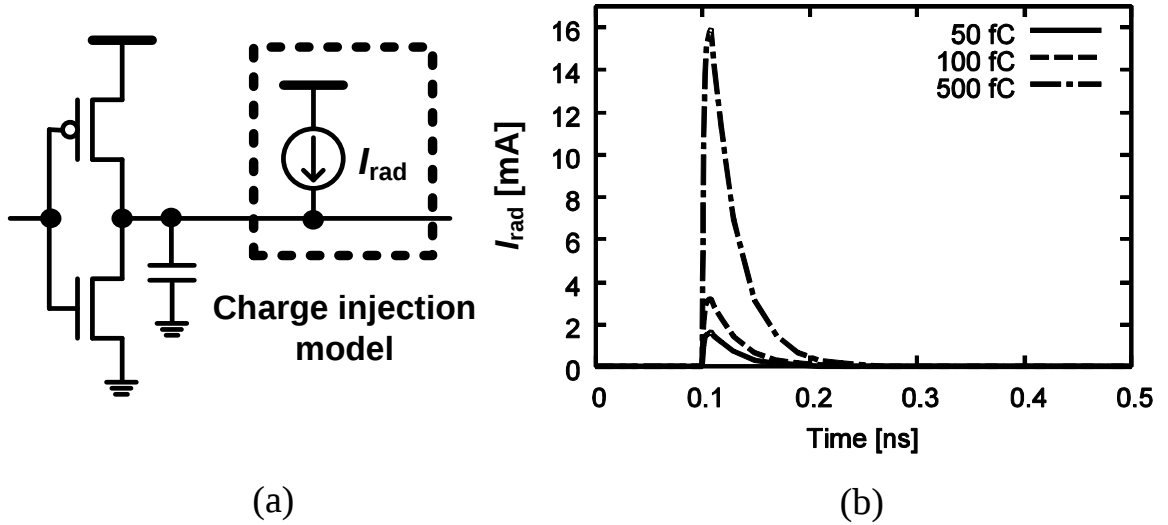


Figure 2.3: (a) Circuit simulation set-up of pMOSFET-hit using charge injection model (I_{rad}) and (b) transient current curves of pMOSFET-hit when Q_{DEP} values are 50 fC, 100 fC, and 500fC.

injected to the p^+ source node or drain node. The current injection is denoted ‘pMOSFET-hit’. The pMOSFET-hit is also modeled using Equation(2.1). Note that the time constant T value is smaller than that of the nMOSFET-hit as $T = 15$ ps [36]. Figure 2.3 shows a circuit simulation set-up of pMOSFET-hit using the charge injection model and transient current curves of nMOSFET-hit when Q_{DEP} values are 50 fC, 100 fC, and 500fC.

Table 2.2: Types of categorized errors.

Sub-circuits	Radiation-induced error types
VCO	Phase shift
CP	Voltage disturbance at control voltage (V_{ctrl})
PFD	Incorrect pulse
Divider	Perturbation of divided clock

2.3 Categorization of Radiation-Induced Errors

All radiation-strike possibilities were examined in this research. All cases of radiation strikes are combinations of when they occur and where they occur (locations and times). It was found that types of error signals could be categorized according to sub-circuits from the results of the examination. Even if there were many nodes in a sub-circuit, the same type of radiation-induced error was observed at the output of the sub-circuit regardless of which node the radiation strike occurred in. There are five general sub-circuits in PLLs, which are the voltage-controlled oscillator (VCO), charge pump (CP), loop filter (LF), phase frequency detector (PFD), and Divider. As the LF only consists of passive components such as capacitors and resistors, it cannot generate radiation-induced errors. Hence, the radiation-induced errors were categorized according to the other four sub-circuits, which are the VCO, CP, PFD, and divider. The types of categorized errors are summarized in Table 2.2.

This section discusses analysis of the categorized radiation-induced errors for each sub-circuit. The discussion is divided into that on digital sub-circuits and analog sub-circuits.

2.3.1 Radiation Strike at Analog Sub-Circuits

Voltage-Controlled Oscillator

The VCO generates a clock signal referring to the control voltage (V_{ctrl}) as its input. The clock signal experiences phase shift due to a SET. The phase shift in the VCO has a direct impact on the phase of the PLL output clock, as illustrated in Figure 2.4.

Figure 2.5 illustrates a transistor-level schematic of the VCO that is used for this analysis. The VCO design is based on the differential buffer delay stages with symmetric loads and replica-feedback biasing, as depicted in Figure 2.1 [33, 46]. One buffer delay stage has three nodes that may experience an SET. Two nodes are differential output nodes (V_{outn} and V_{outp}) and the other node is the source-

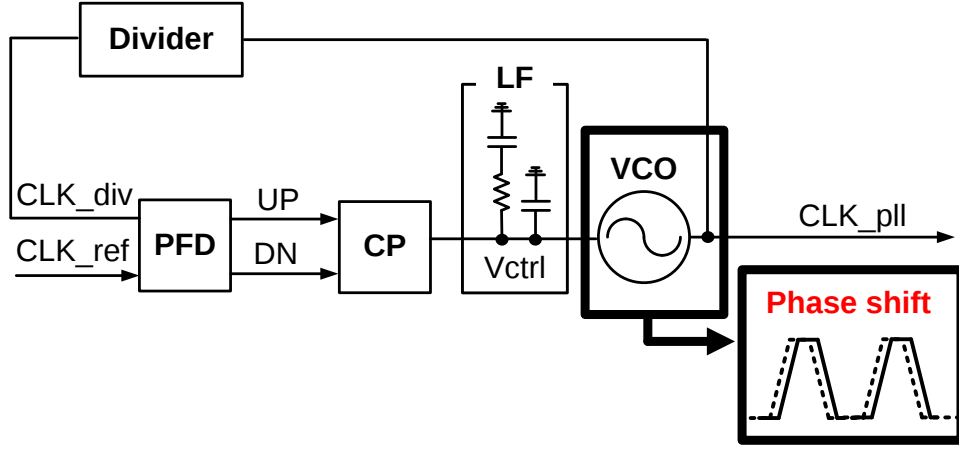


Figure 2.4: Phase shift caused by SET at VCO

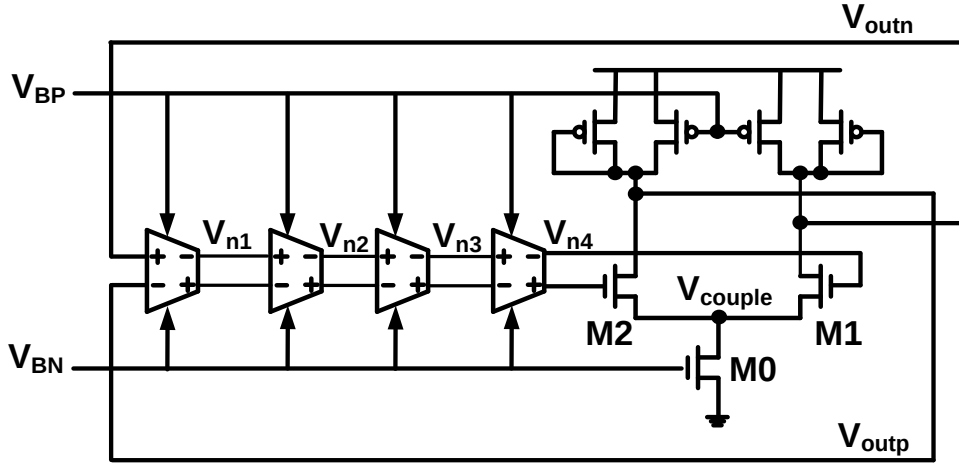


Figure 2.5: Transistor-level schematic of VCO.

coupled node (V_{couple}). While the V_{outn} and V_{outp} have a possibility to experience an nMOSFET-hit or a pMOSFET-hit, the V_{couple} is suffered from only nMOSFET-hit. For the VCO, nMOSFET-hit effect of 50 fC (Q_{DEP}) is demonstrated as a common condition. Figure 2.6 depicts waveforms when an nMOSFET-hit occurs at the V_{outn} and the V_{couple} , respectively. The nMOSFET-hit at the V_{couple} have no effect on the VCO output signal whereas nMOSFET-hit at the output node leads to a phase shift. Although V_{couple} has a voltage disturbance, nMOSFETs connected to the output nodes (M1 and M2) stay in the saturation region. Thus, the large resistances between the source and the drain of M1 and M2 shield the output nodes from the disturbance. The differential output nodes are the most vulnerable node, which is called ‘representative node’ of the VCO in this research work.

The vulnerability to a SET depends on not only locations but also timings of a radiation strike

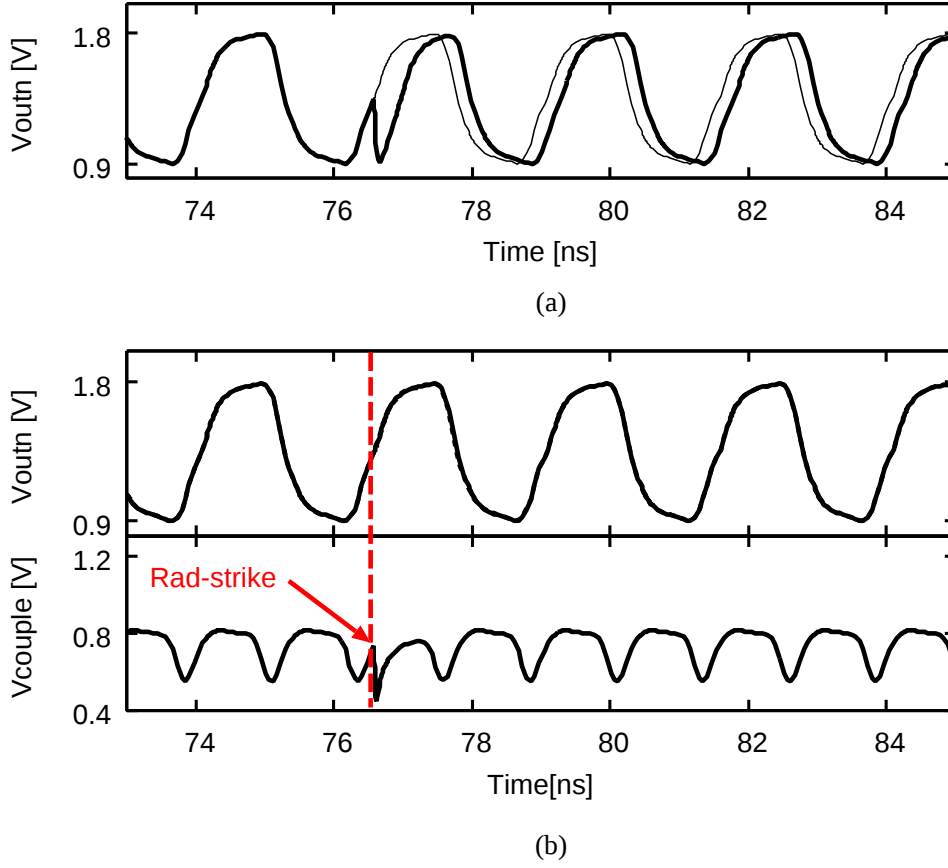


Figure 2.6: Waveforms when an nMOSFET-hit occurs at (a) the V_{outn} and (b) the V_{couple} .

because the VCO signal is time-varying. The VCO is simulated with a transient current that emulates charge injection by a radiation strike to identify the time dependency. The radiation strike is assumed to occur at the last stage of the VCO in the simulation. Figure 2.7 lists the time dependence of the SET in the clock signal on time. The SET occurs during transition of the clock signal in Figure 2.7 (a). Figure 2.7 (b) has another case when the SET occurs at saturated voltage swing. The results in Figure 2.7 (a) have a larger phase shift than those in Figure 2.7 (b). Hence, it can be seen that the clock on the VCO is more vulnerable to the SET during transition than that during saturated voltage swing.

Charge Pump

The CP produces the control voltage (V_{ctrl}) for the VCO. Since V_{ctrl} is a DC signal during the locked condition of the PLL, the vulnerability to a SET is independent of the time. Location-dependency of the SET vulnerability is only examined for the CP. Figure 2.8 illustrates the transistor-level schematic of the

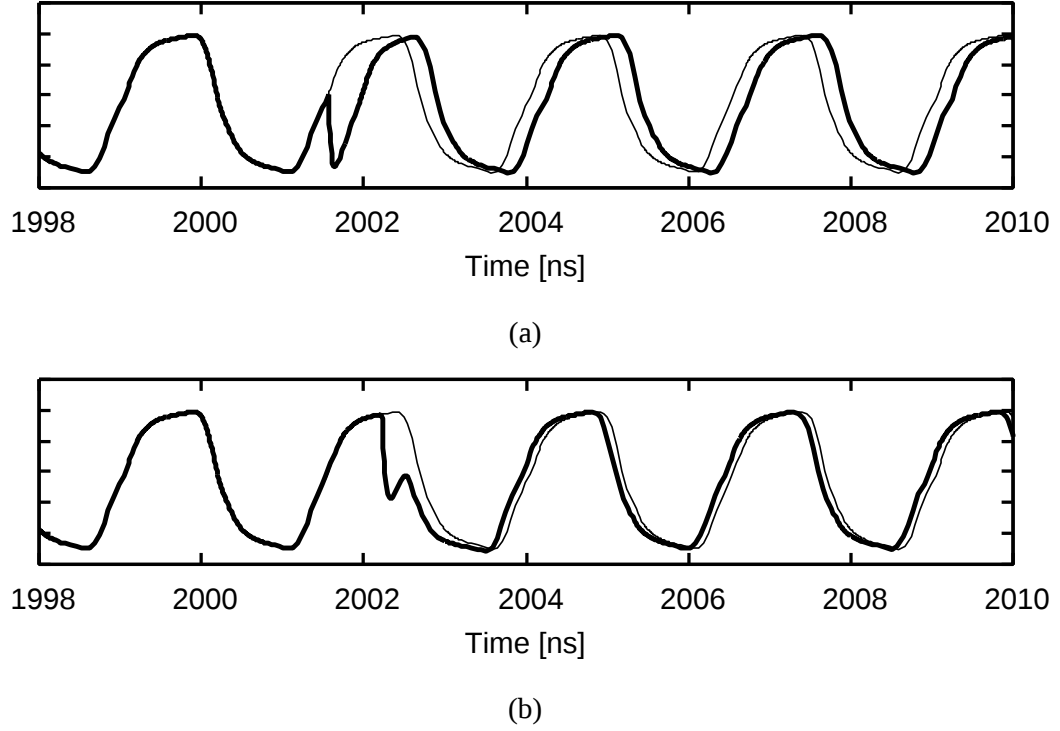


Figure 2.7: Dependence of SET in clock signal on time (a) when SET occurs during transition (b) when SET occurs at saturated voltage swing.

CP. Similar to the examination of the VCO, nMOSFET-hit effect for all nodes of the CP is demonstrated and 500 fC of Q_{DEP} is injected at the 2.01 microsecond. Figure 2.9 shows the CP output when an nMOSFET-hit occurs at $V_{3,\text{CP}}$ and $V_{4,\text{CP}}$ in Figure 2.8. A radiation strike such as the nMOSFET-hit produces an SET at each node of $V_{4,\text{CP}}$ and $V_{3,\text{CP}}$. Nevertheless, there is no effect on the CP output (V_{ctrl}). As the DN signal and UP signal are LOW in the locking condition, the NMOS transistor connected to the CP output (M5 in Figure 2.8) is being turned off. Thus, the SET at $V_{4,\text{CP}}$ and $V_{3,\text{CP}}$ cannot convey to the CP output (V_{ctrl}). By the same reason, the SET occurring the $V_{0,\text{CP}}$ and $V_{2,\text{CP}}$ has no impact on the CP output (V_{ctrl}). On the other hands, an SET at $V_{1,\text{CP}}$ and V_{ctrl} leads to a voltage disturbance at the CP output. Figure 2.10 depicts the CP output when an nMOSFET-hit occurs at $V_{1,\text{CP}}$ and V_{ctrl} in Figure 2.8. The SET at V_{ctrl} is the voltage disturbance of V_{ctrl} itself, as illustrated in Figure 2.10 (b). The SET at $V_{1,\text{CP}}$ turn on pMOSFETs connected to the CP output (M12 and M13), instantaneously. The drain current of the turned on M12 and M13 charges the capacitors of the LF and then V_{ctrl} experiences the voltage disturbance, as shown in Figure 2.10 (a). From this examination, it is identified that radiation-strike effect on the CP appears as the voltage disturbance on the output (V_{ctrl}).

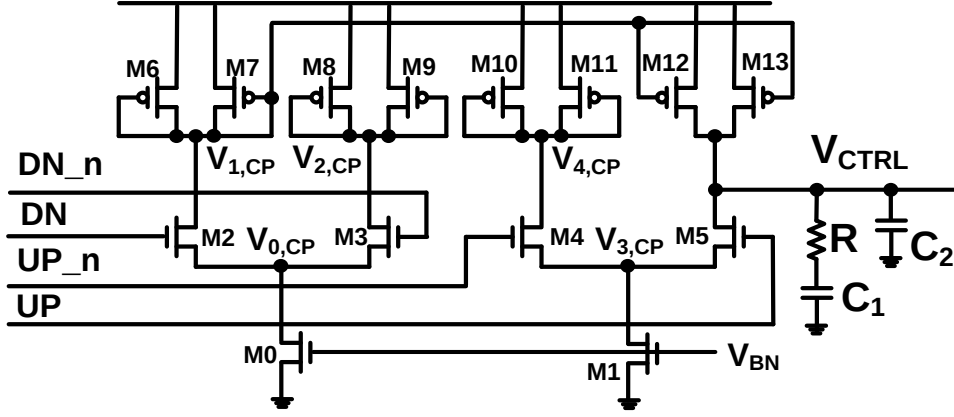


Figure 2.8: Transistor-level schematic of CP.

The representative node of the CP is V_{ctrl} .

This error signal at CP output, which is a voltage disturbance, is propagated to PLL output through the VCO. If the amount of disrupted voltage is ΔV on V_{ctrl} , the oscillation frequency of the VCO will be modulated by

$$\Delta f = K_{VCO} \Delta V, \quad (2.2)$$

where Δf is the amount of modulated frequency and K_{VCO} is the gain of the VCO. When SE occurs at the CP, the frequency modulation of the clock signal will be observed at PLL output, as shown in Figure 2.11.

2.3.2 Radiation Strike at Digital Sub-Circuits

D-Flipflops

Since the digital part of the PLL consisted of D-flipflops (D-FFs), D-FF errors by radiation strikes were first analyzed and are described in this section.

The error in D-FFs not only depends on the location of the radiation strike but also when it occurs because D-FFs deal with time-varying signals. The location and the time are divided into two types of D-latches in the D-FFs and two states of the input clock, as shown in Figure 2.12. If the state of the input clock (CLK_IN) is low, the master latch receives the input value through terminal 'D' while the slave latch cannot receive any input. In this case, the master latch is in a 'transparent state' and the slave latch is in a 'latch state'. When a radiation strike occurs at a latch that is in a 'transparent state',

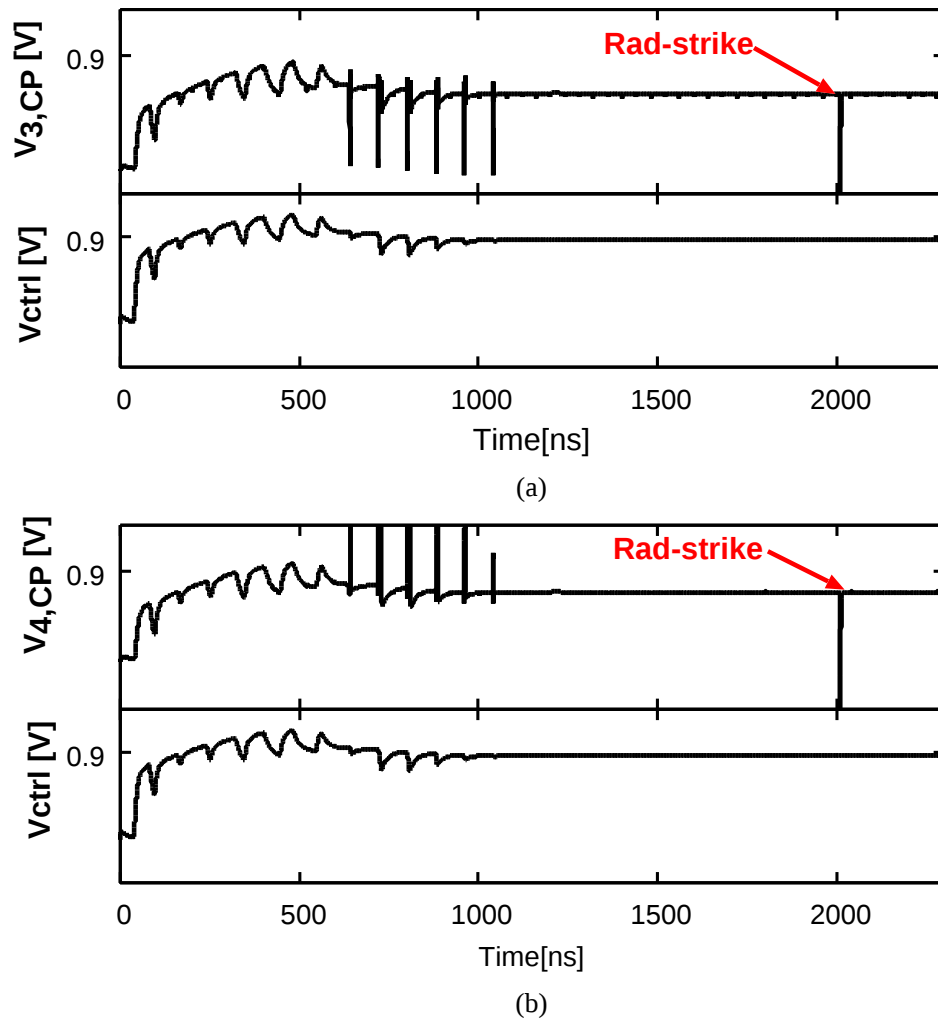


Figure 2.9: CP output when nMOSFET-hit occurs at (a) $V_{3,CP}$ and (b) $V_{4,CP}$ in Figure 2.8.

the latch experiences an SET. However, a latch in a 'latch state' experiences an SEU.

The SEU and SET that occurred in the D-FF are propagated to D-FF output and then affect error signals that occur at each digital sub-circuit. Not all SEU and SET are propagated to D-FF output. Figure 2.13 depicts the propagation mechanism for the SEU and SET that occur at the D-FF. When the SET or SEU occurs at the slave latch, these errors are observed at D-FF output. This is because the output of the slave latch is that of the D-FF. However, errors occurring at the master latch should pass through the slave latch. Flipped data in the master latch are conveyed to the slave latch in SEU because the slave latch is in a transparent state. The SET, on the other hand, is recovered before the slave latch is changed to a transparent state. Table 2.3 sums up the types of errors under the conditions of combined

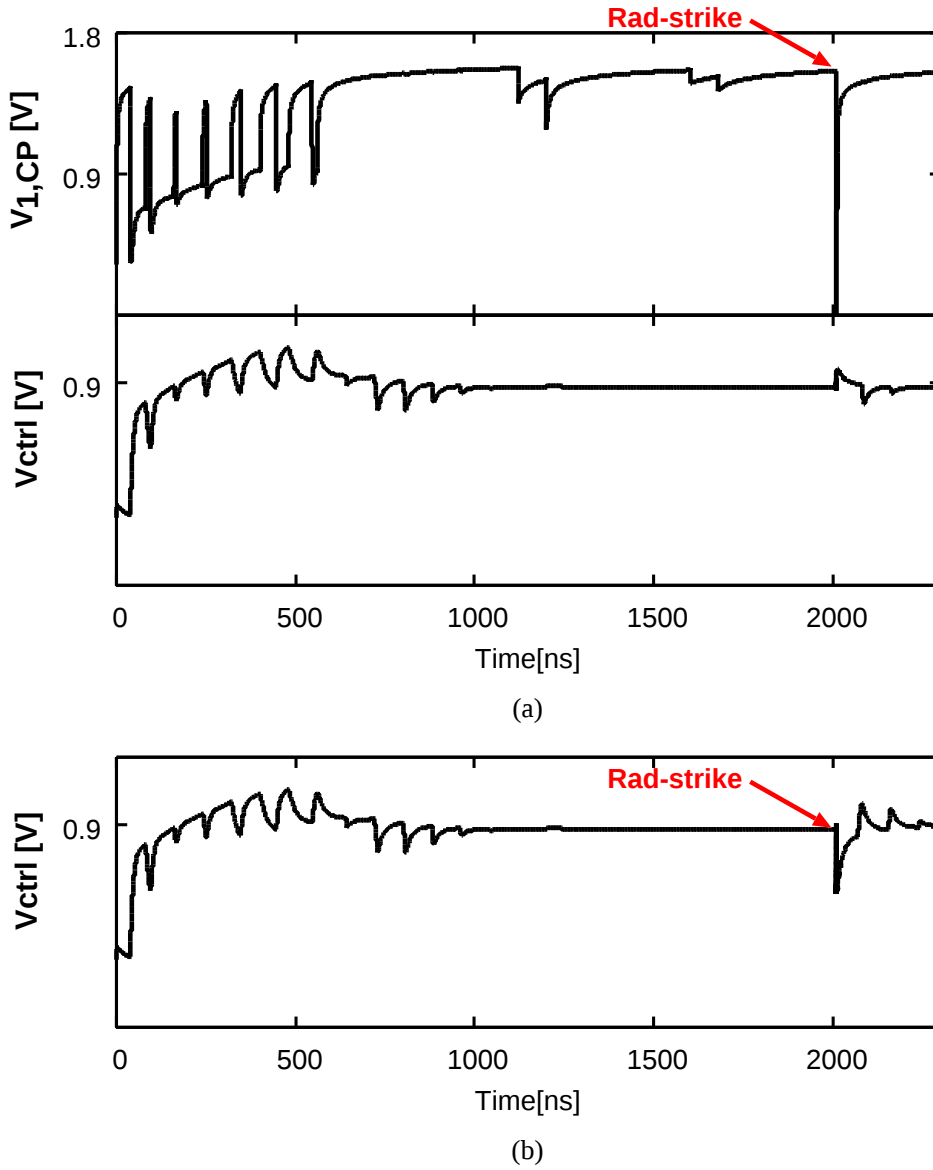


Figure 2.10: CP output when nMOSFET-hit occurs at (a) $V_{1,CP}$ and (b) V_{ctrl} in Figure 2.8.

locations (types of latches) and times (states of clock). As an example, Figure 2.14 illustrates an SEU and SET at D-FF output when a radiation strike occurs at the slave latch. The SEU appears during LOW of the clock state and the SEU appears during HIGH of that, as shown in Figure 2.13.

Although only the SE in two latches are mentioned here, the SET on the clock line also generates errors in the D-FF. The errors caused by the SET on the clock line depend on types of sub-circuits involving the D-FF. Thus, details of the SET effect on the clock line will be respectively discussed in

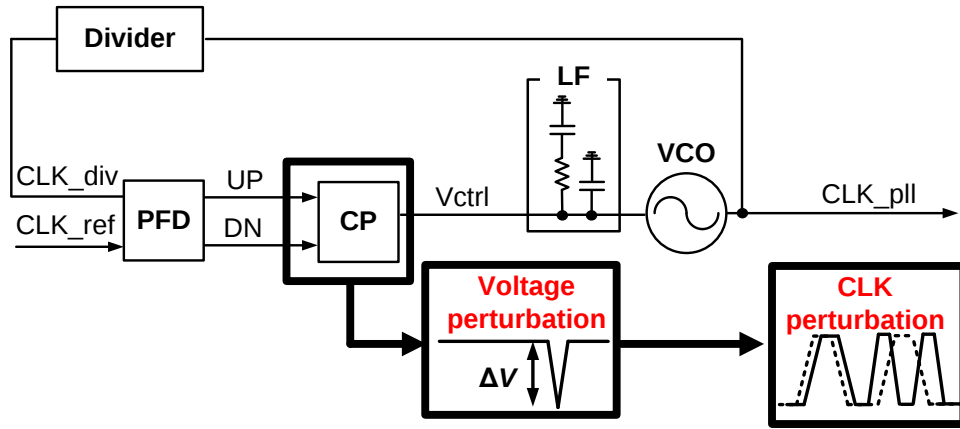


Figure 2.11: Voltage disturbance at CP output and its propagation to PLL output

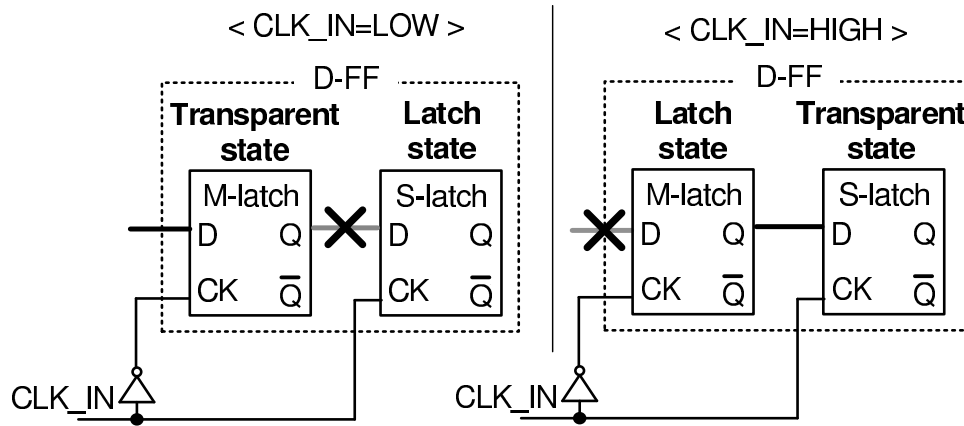


Figure 2.12: Error conditions in D-FF.

the subsections on the PFD and divider.

Phase-Frequency Detector

The PFD can be accomplished in various forms. Figure 2.15 (a) depicts the implementation of the PFD in this research. Its equivalent circuit in Figure 2.15 that (b) consists of two D-FFs and an AND gate has been employed in this part to facilitate an analysis. As previously mentioned, the two D-FFs in

Table 2.3: Categorized errors observed at D-FF's output.

	CLK_IN=LOW	CLK_IN=HIGH
Master latch	No failure	SEU
Slave latch	SEU	SET

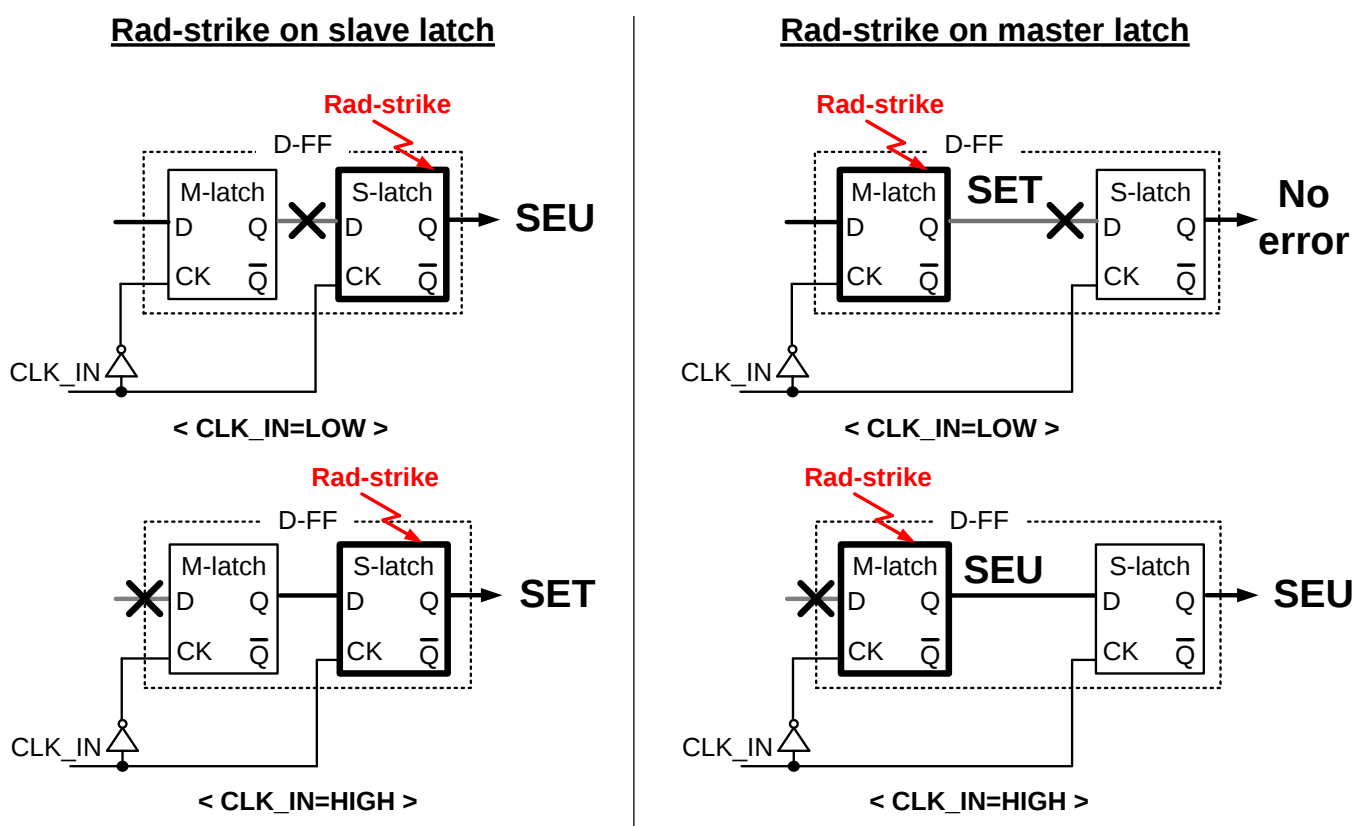


Figure 2.13: Propagation mechanism for SEU and SET occurring at D-FF.

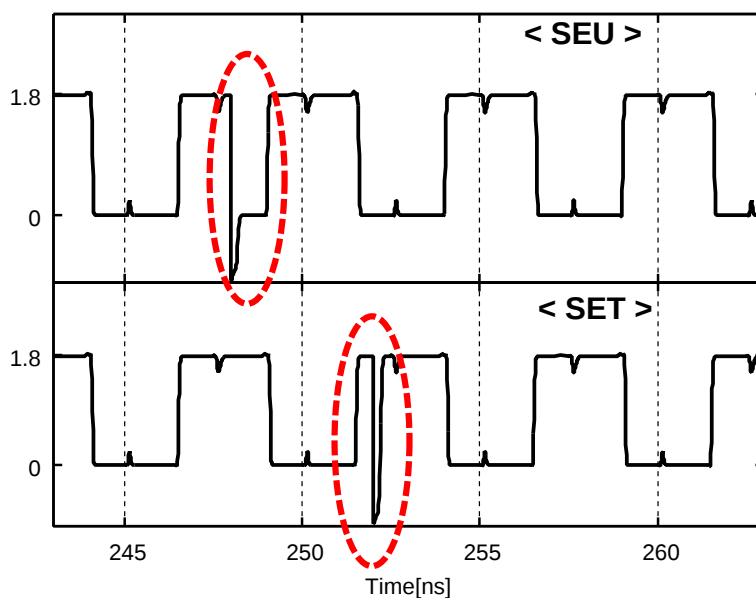


Figure 2.14: Example of SEU and SET when radiation strike occurs at slave latch.

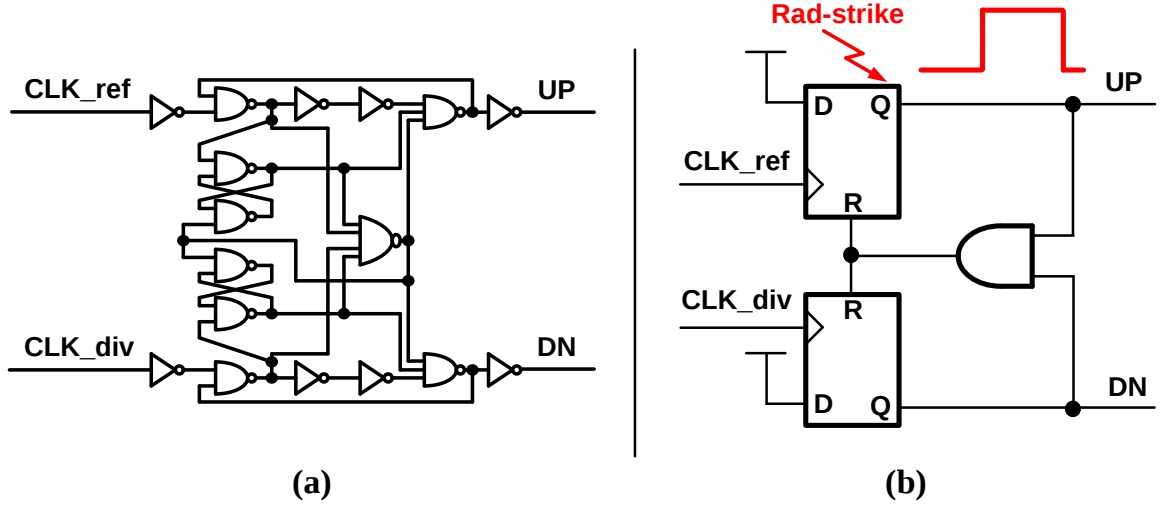


Figure 2.15: (a) Implementation of PFD in this research and (b) its simplified circuit.

the PFD can have a SET or SEU caused by a radiation strike. The SET or SEU results in a pulse on an UP or DN signal at PFD output even if the clock at the PLL's output (CLK_pll) is aligned with the reference clock (CLK_ref). If SE occurs at a D-FF that has generated an UP signal, the UP signal is activated. Similar to this, the other D-FF creates a pulse on the DN signal due to the SE. The activated UP and DN signals are called 'incorrect pulses'.

An incorrect pulse can be propagated to PLL output through the CP, LF, and VCO, as illustrated in Figure 2.16. The pulse width (t_{pul}) is the time to turn on the current source in the CP. A voltage disturbance on V_{ctrl} appears as a result and hence the oscillation frequency of the VCO is modulated. Thus, a wider incorrect pulse induces serious clock perturbations. The width of the incorrect pulse (t_{pul}) caused by the SEU is much wider than that of the SET. Figure 2.17 shows the simulated waveforms when SEU and SET occurred at the D-FF of the UP signal. The upset value of the D-FF is maintained until the subsequent clock edge appears in the case of an SEU and hence this leads to a wide pulse. The effect of the SET on clock perturbation is negligible because its pulse width (t_{pul}) is too narrow to turn on the CP.

SE in the clock line should be examined as well as SE in the latches. The clock inputs of D-FFs are respectively driven by the reference (CLK_ref) and divided clocks (CLK_div) shown in Figure 2.15. When SE occurs in the clock line, a SET is observed on the CLK_ref or CLK_div. Figure 2.18 illustrates a SET on the CLK_div. Since the D-FF that is in charge of the DN signal recognizes the SET as a rising signal, the DN signal is activated from the SET moment. The width of this DN signal is the

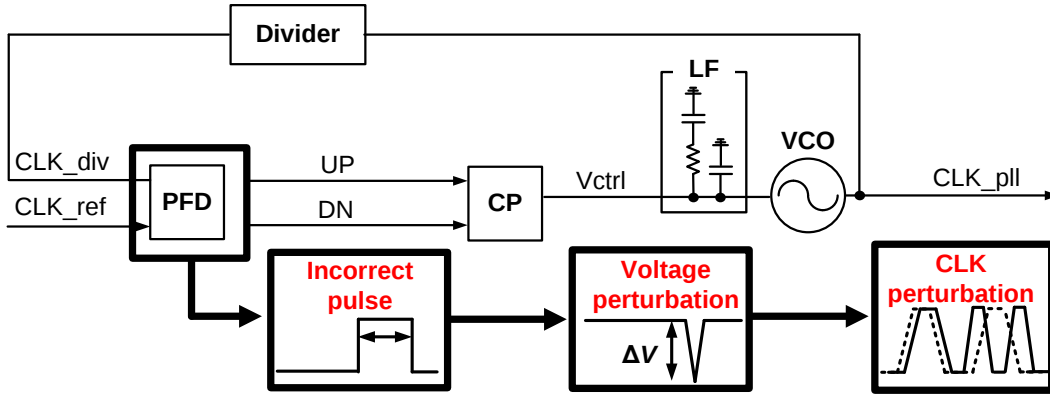


Figure 2.16: Propagation of incorrect pulse to PLL output.

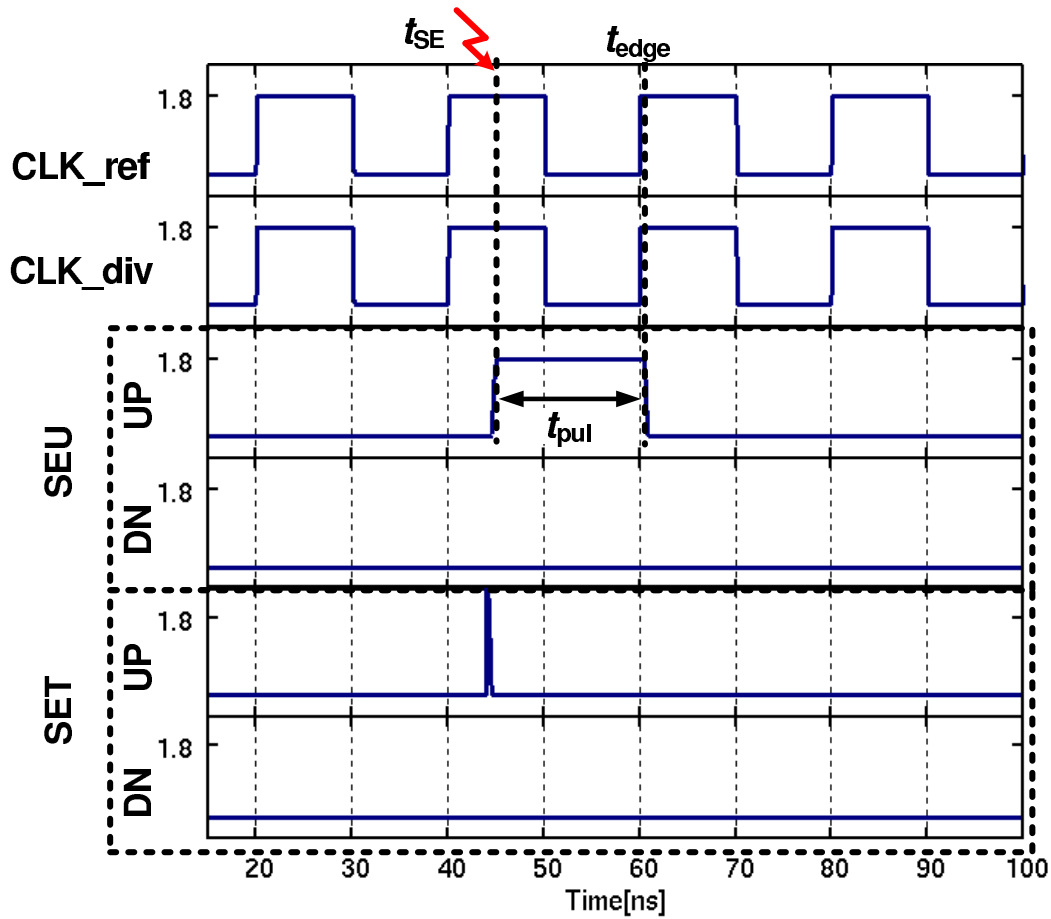


Figure 2.17: Example of SEU and SET when radiation strike occurs at PFD.

duration from the SET moment to the subsequent rising edge of the other clock input. The incorrect pulse maintained in Figure 2.18 until the rising edge of the **CLK_ref**. Consequently, the width of the

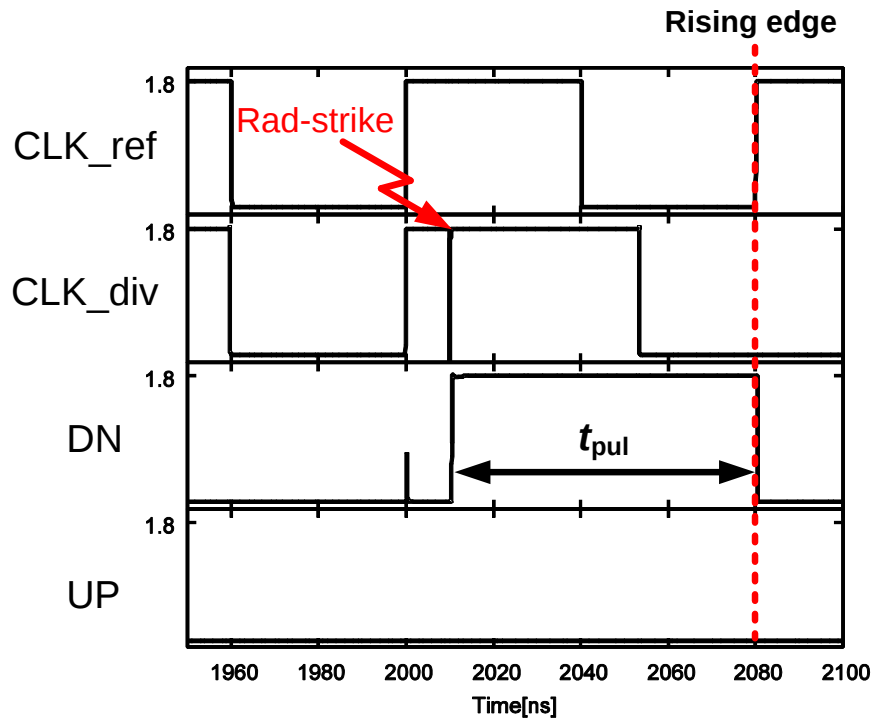


Figure 2.18: SET on divided clock (CLK_div).

incorrect pulse when the SET occurred in the clock line is identical with that when the SEU occurred at the latches.

Divider

The divider consists of an asynchronous cascade of unit dividers in which the frequency of the input clock is divided by two. Figure 3.13 has a general configuration for the divider and unit dividers, which is a D-FF with negative feedback connecting D input with complimentary Q output ($\bar{Q}$). The SEU in the latches leads to perturbation in the clock in which the PLL output clock (CLK_div) is divided although the PLL generates a locked clock. The SET at the clock line is examined for the divider together with the SET in the latches because the output of the unit divider is connected to the input of the subsequent unit divider. This means the SET in the latches is conveyed to the input of the subsequent unit divider. Similar to that of the PFD case, the SET in clock input is equivalent to the SEU in the subsequent latch.

The amount of clock perturbation at the divider depends on the locations of the SEs. If SE occurs at the closest unit divider to the PFD, large clock perturbation is observed at divider output. However, SE at the furthestmost unit divider produces small perturbation. As an example, Figure 2.20 has output

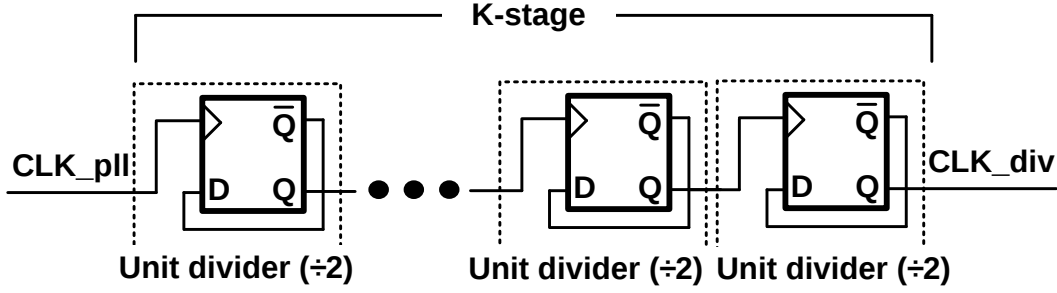


Figure 2.19: General configuration for divider consisting of unit dividers ($\div 2$).

clocks of a five-stage divider when an SEU occurs at the closest unit divider and at the furthestmost unit divider to the PFD.

The divided clock (CLK_div) that experiences clock perturbation is not aligned with the reference clock (CLK_ref) and hence the PFD creates an incorrect pulse at its output. The incorrect pulse passing through the CP, LF, and VCO finally results in the frequency of the VCO being modulated.

Passing through the CP, LF, and VCO, the radiation-induced error at the divider results finally in the frequency modulation of the VCO. Figure 2.21 shows the propagation of radiation-induced error occurring at the divider.

2.4 Radiation-Induced Clock Perturbation

The previous section discussed radiation-induced errors at all the sub-circuits and their propagation to PLL output. All radiation-induced errors were finally converted to clock perturbation at PLL output. The clock perturbation in the PLL could be categorized according to the locations of radiation strikes, which were in the analog (CP, LF, and VCO) and digital sub-circuits (Divider and PFD). Figure 2.22 shows examples of categorized clock perturbations when (a) radiation strikes occur at the PFD and (b) at the CP. An SEU occurs at the D-FF generating the DN signal in Figure 2.22 (a), and it causes an incorrect pulse on the DN signal. Figure 2.22 (b) shows a radiation strike occurring at a pMOSFET connected to a CP output node and the injection charge (Q_{DEP}) caused by the radiation strike is 500 fC. This radiation strike produces an SET, which is a transient voltage increase on the control voltage (V_{ctrl}). The PLL for examination (in Figure 2.1) has been designed such that an increase in V_{ctrl} reduces the VCO frequency. Thus, the clock periods in Figures 2.22 (a) and (b) become large after the radiation strike. Although both clock periods increase, their perturbation types are different. When radiation

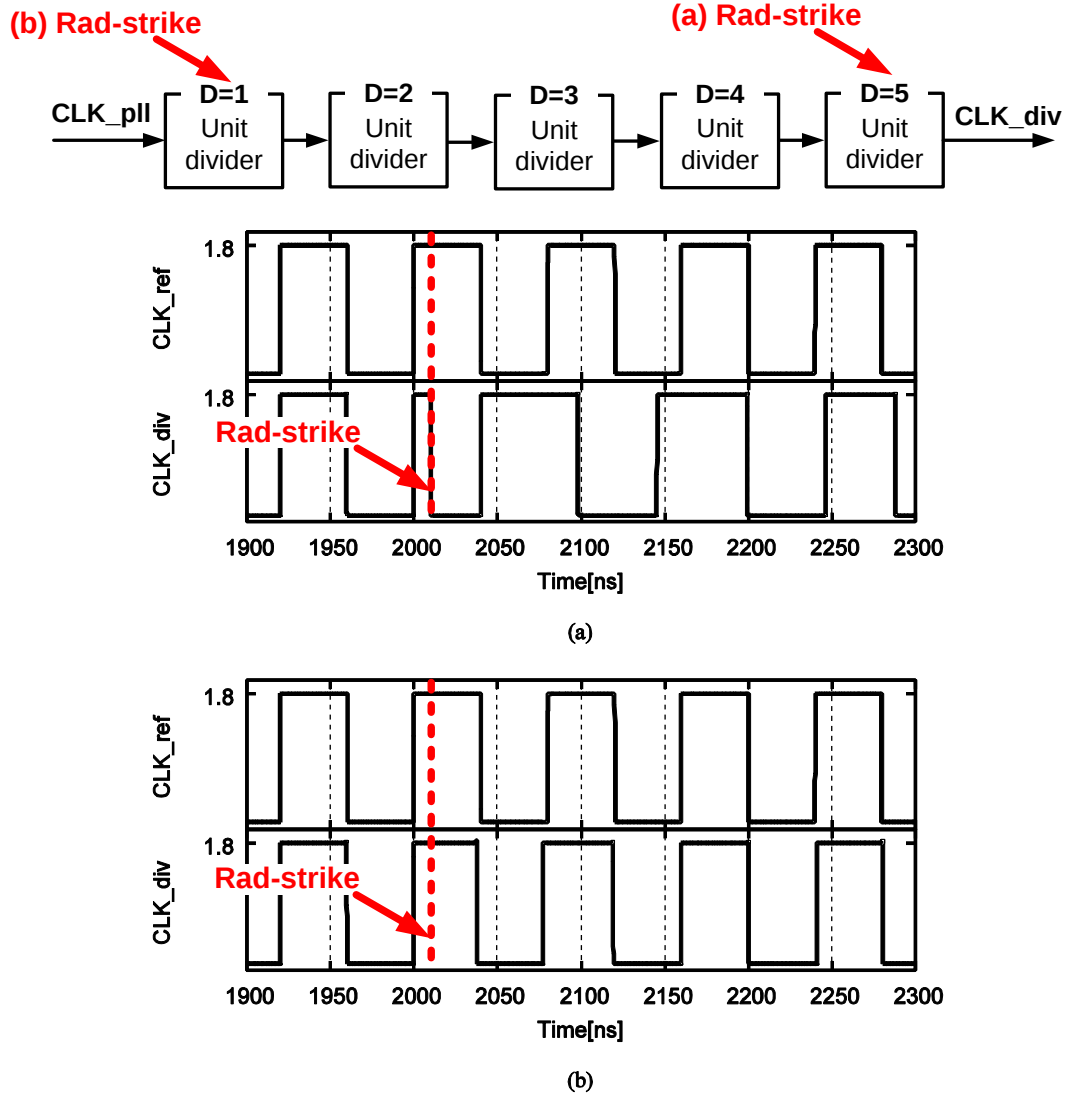


Figure 2.20: Clock perturbation at five-stage divider output (a) when SEU occurs at fifth unit divider and (b) SEU occurs at first unit divider from VCO.

strike occurs at the PFD, the PLL output clock is gradually perturbed, which is called ‘gradual perturbation’. However, a large deviation of the period is observed immediately by the SET at the CP output node (V_{ctrl}), which is called ‘instant perturbation’. These perturbation types are due to the difference in the propagation mechanism. Since the incorrect pulse that occurs at the PFD passes through the CP and LF, the clock perturbation caused by the incorrect pulse has large time constant characteristics. The radiation-induced error at the CP does not include the large time constant of the CP and LF and hence clock perturbation has small time-constant characteristics. Consequently, radiation strikes at the digital

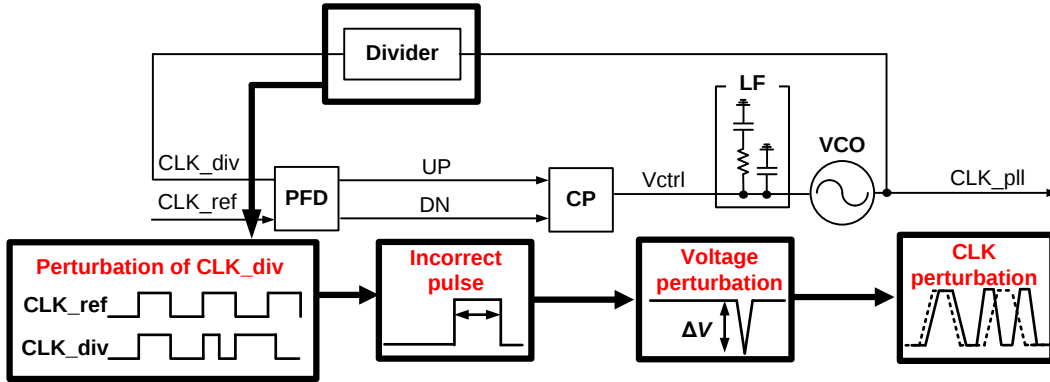


Figure 2.21: Propagation of perturbation in divided clock to PLL output.

sub-circuits and analog sub-circuits cause gradual perturbation in the former and instant perturbation in the latter.

Analog sub-circuits have been focused on in the demonstrated PLLs that have been designed as the critical nodes in almost all conventional works [17, 25–27, 29, 30]. This is because large amounts of clock perturbation appear immediately due to radiation strikes in analog sub-circuits. The gradual clock-perturbation in this demonstration using the PLL in Figure 2.1 eventually meets a large amount of clock perturbation (a 4 ns period) within 10 clock-cycles, which is the same amount of clock perturbation as that with instant clock-perturbation. It is not only possible for analog sub-circuits to become critical parts but also digital sub-circuits. Therefore, the vulnerability of digital sub-circuits to radiation should be considered as much as that of analog sub-circuits.

2.5 Summary

This chapter discussed qualitative analysis of radiation effect on PLL. Since radiation effect on PLL depends on locations of radiation strikes and timings of radiation strikes, all possibilities of the locations and timings were examined. Radiation-induced errors were classified according to sub-circuits of the VCO, CP, PFD, and divider based on the results of the examination. Each sub-circuit generated particular error signal caused by radiation strikes, as summarized in Table 2.2. Furthermore, it was analyzed how the categorized errors propagate to PLL output in order to lead to clock perturbation. Clock perturbations revealed different types of perturbations depending on the locations of radiation strike due to the large time constant of the LF. Radiation strikes at digital sub-circuit caused ‘gradual

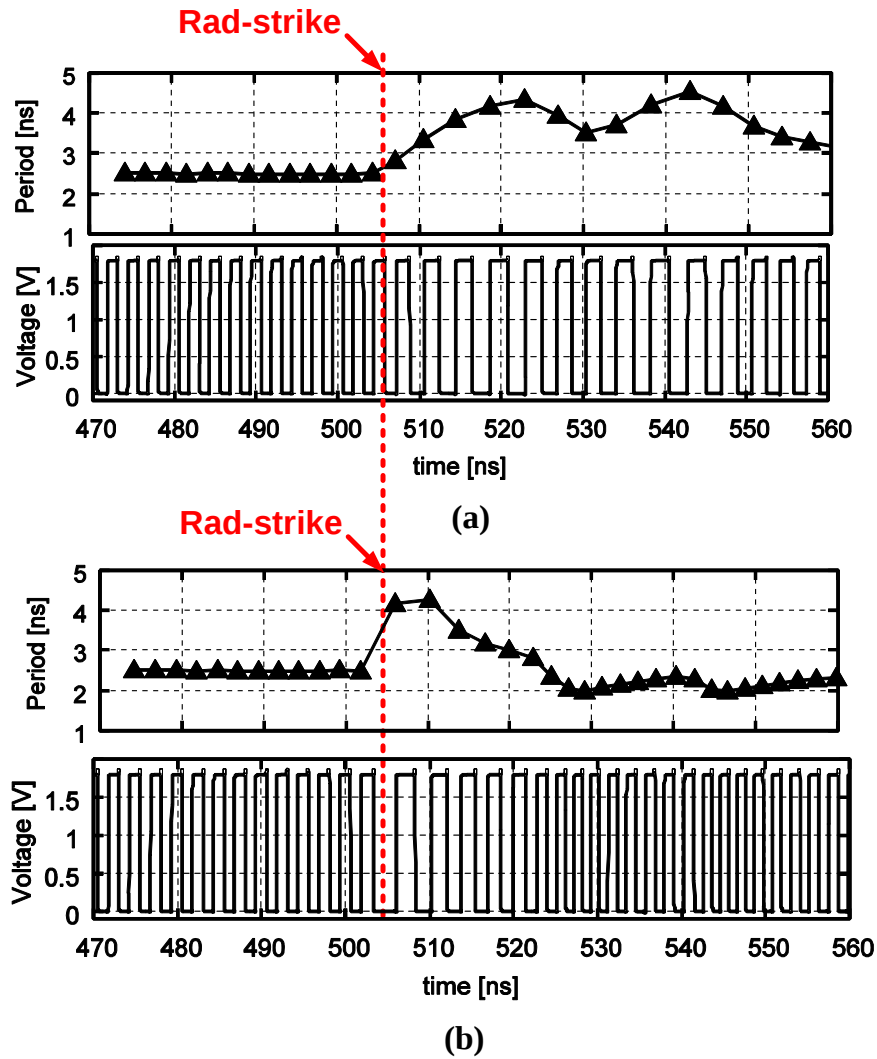


Figure 2.22: Results from SPICE simulations of clock perturbations due to (a) radiation strikes on digital and (b) analog part.

perturbation' and those at analog sub-circuits caused 'instant perturbation'. In addition, it is identified that gradual perturbation is as serious as instant perturbation in the amount of clock perturbation. Therefore, the vulnerability of not only analog sub-circuits but also the digital sub-circuit to radiation should be analyzed.

Chapter 3

Analytical Modeling of Clock Phase Displacement under Radiation

3.1 Introduction

This chapter discusses analytical modeling of phase displacement on PLL clock under radiation. Evaluation of radiation vulnerability on PLLs is a primitive work to design RH-PLLs. Especially, the evaluation is important for the partial hardening techniques to find the most vulnerable parts in PLLs. In conventional works, all possibilities of radiation strikes were examined with transistor-level simulation. The radiation strike possibilities depend on the deposition charge (Q_{DEP}) along with locations and timings of radiation strikes. Combinations of these three factors cause a brute-force analysis in the transistor-level simulation. Thus, an analytical model is necessary to achieve efficiency in evaluation of the radiation vulnerability. Chapter 2 accomplished to categorize radiation effect for locations and timings of radiation strikes. Based on the categorization, amount of radiation-induced clock perturbation is modeled in this chapter. The amount of radiation-induced clock perturbation is quantified as ‘phase displacement. This chapter presents an analytical model of phase displacement for sub-circuits of PLL.

This chapter begins with an introduction of the definition of the phase displacement. Then, modeling of phase displacement based on radiation-induced error analysis will be discussed. Model equations of the phase displacement are formulated based on the principle how the categorized radiation-induced errors propagate to the PLL output. It means the analytical model includes four model equations to

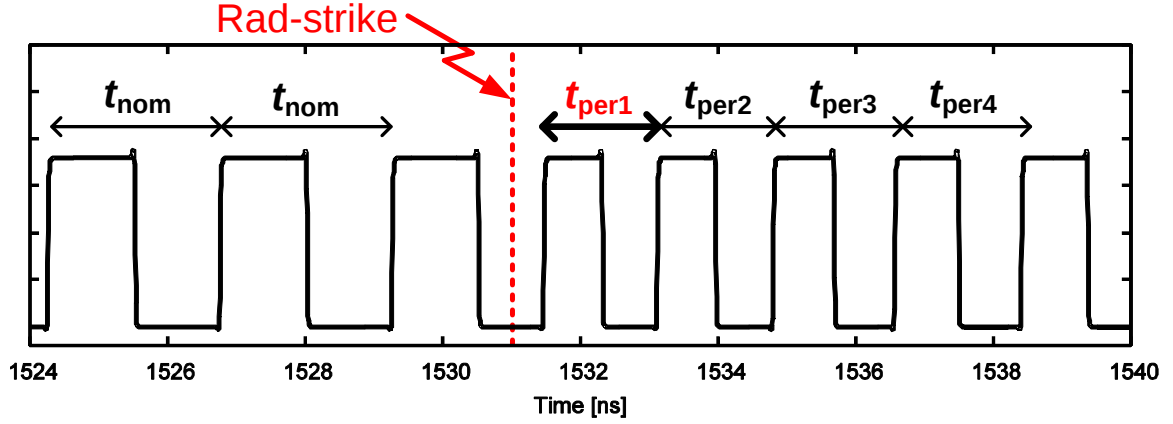


Figure 3.1: Definition of perturbed clock period (t_{per}) and nominal clock period (t_{nom}).

obtain the phase displacement for the VCO, the CP, the PFD and the Divider. The results from the model equations are verified through comparison with transistor-level simulation, such as SPICE.

3.2 Definition of Phase Displacement

The clock perturbation is quantified as the phase displacement ϕ_{disp} [30]. This is calculated from the time difference between the perturbed clock period (t_{per}) and the nominal clock period (t_{nom}) at the PLL output. This time difference is then normalized by t_{nom} and multiplied by 2π as follows:

$$\phi_{\text{disp}} = \frac{2\pi \cdot |t_{\text{nom}} - t_{\text{per}}|}{t_{\text{nom}}}. \quad (3.1)$$

The units of ϕ_{disp} are radian. Figure 3.1 shows an example of a clock perturbation caused by nMOSFET-hit at CP output. A nominal clock period (t_{nom}) and different perturbed clock periods for every clock cycle (t_{per1} , t_{per2} , and so on) are observed. Since the radiation strike leads to instant perturbation, t_{per1} has the maximum difference from the nominal clock period. This research work chooses the maximum perturbed period to calculate the ϕ_{disp} because the evaluation needs to consider the worst case of radiation vulnerability. In the case of Figure 3.1, the t_{per1} is substituted for the variable t_{per} in Equation (3.1). Modeling t_{per} is the main work to formulate model equations of phase displacement in the next section. The nominal clock period (t_{nom}) is a given value in a PLL design.

Table 3.1: PLL's performance parameters for demonstration.

Parameter	Value	Parameter	Value
Process	0.18 μm	V_{DD}	1.8 V
f_{nom}	400 MHz	VCO's stage (N)	5
V_{ctrl} in locked condition	0.9 V	K_{VCO}	883 MHz/V
C_1, C_2	18 pF, 1.8 pF	R	10 k Ω
Divider stage (K)	5	f_{ref}	12.5 MHz
I_{CP}	14 – 71 μA		

3.3 Modeling of Phase Displacement based on Categorization

This section discusses modeling phase displacement for sub-circuits of PLL, which are the categorization result in Section 2. Each part firstly explains error signal modeling for sub-circuits - the phase shift for the VCO, the voltage disturbance for the CP, the incorrect pulse for the PFD, and the divided clock perturbation for the the Divider. The model of the phase displacement is derived from this error signal model. The model equations are verified through comparison with SPICE simulation results. The verification was performed with the conventional low-jitter PLL designed with a 0.18 μm CMOS process, which has been introduced in the previous chapter. Its performance parameters are summarized in Table 3.1 and they will be used for formulating model equations in this section.

3.3.1 Radiation Strike at Analog Sub-Circuits

Voltage-Controlled Oscillator

The model equation of the phase displacement for the VCO is derived without use of Equation (3.1). To model the phase displacement for the VCO, the impulse sensitivity function (ISF) is used for the jitter and phase noise of ring oscillators [47]. In [47], the noise causing the jitter is modeled with the impulse current injected into a node of a ring oscillator. This model is similar to the radiation-strike models which are the nMOSFET-hit and pMOSFET-hit discussed in Chapter 2. Although the radiation-strike is modeled using exponential current, it can be assumed to be an impulse current because the time constant T in Equation (2.1) has a small value ($T=22$ ps in 0.18 μm CMOS process) compared with the period of the operating frequency. If the oscillation frequency of the VCO becomes high through technology scaling, the T value will also be reduced [36]. Thus, this assumption is reasonable

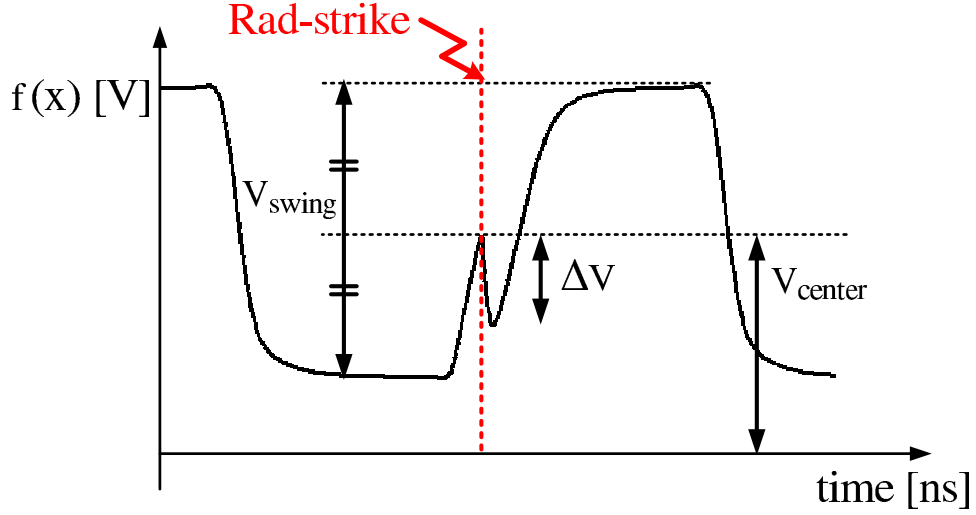


Figure 3.2: Waveform for ring oscillator when radiation-strike occurs.

regardless of increase in oscillation frequency through technology scaling.

The ISF ($\Gamma(x)$) is the time-varying proportionality constant and periodic in 2π . However, only the maximum value of the ISF ($\Gamma_{\max}$) is used as the time-invariant constant in this work in order to evaluate the worst case of ϕ_{disp} . The ISF has the maximum value when the current is injected at the center of transition. $\Gamma_{\max}$ can be derived from equations in [47] as

$$\Gamma_{\max} = \frac{\pi}{N\eta} \quad (3.2)$$

where N is the number of stages of the VCO, η is a proportionality constant, which is given as $\eta=0.9$ for the case of a differential ring oscillator [47]. Figure 3.2 shows the waveform when the ISF has the maximum value. The waveform was obtained by simulating a VCO composing the low-jitter PLL introduced in Chapter 2. Radiation-induced charge is injected the last stage of the VCO (V_{O+}), as depicted in Figure 3.3. In this differential VCO, the voltage swing is 0.9 V, which is from the supply voltage to the half of the supply voltage, and the common-mode voltage (V_{center}) is the center of the swing range ($= 1.35$ V). A charge of 50 fC is injected at the center of transition to emulate the maximum ISF and it leads to a voltage perturbation of the VCO waveform (ΔV).

In a specific ISF, ϕ_{disp} is proportional to the amount of voltage disturbance (ΔV) on the node having the SE. ΔV is determined by the deposition charge (Q_{DEP}) mentioned in Section 2.2 and by C_{node} , which

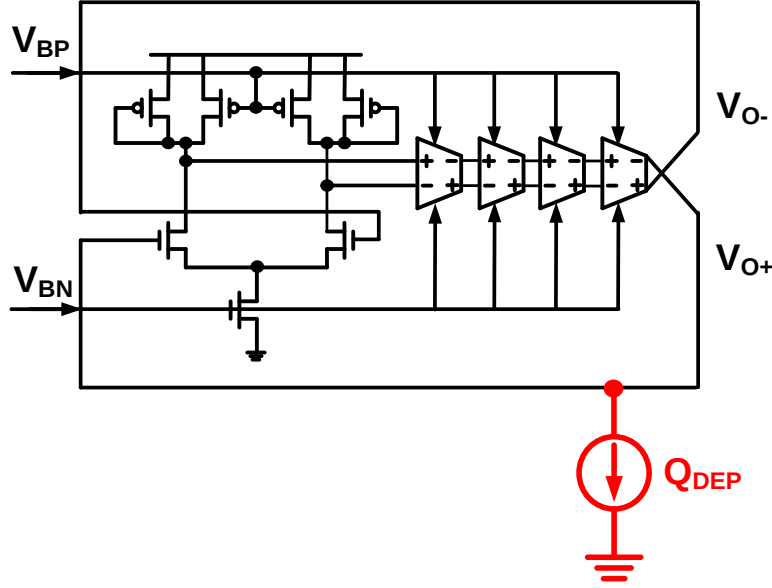


Figure 3.3: VCO schematic used to simulate radiation-induced charge injection.

is the effective capacitance on that node at the time of charge injection. Thus, ϕ_{disp} is expressed by

$$\phi_{\text{disp}} = \Gamma_{\text{max}} \frac{\Delta V}{V_{\text{swing}}} = \Gamma_{\text{max}} \frac{Q_{\text{DEP}}}{V_{\text{swing}} C_{\text{node}}} \quad (3.3)$$

where V_{swing} is the voltage swing across the capacitor. The dominant input parameter to evaluate the phase displacement is the amount of deposition charge (Q_{DEP}) when the radiation strike at the VCO. The other parameters in Equation (3.3), which are V_{swing} , C_{node} , and Γ_{max} , has given values in a PLL design. Equation (3.3) should be considered under a condition originated from the cut-in voltage of the pn-junction. If a node voltage drops by nMOSFET-hit below the substrate voltage, the pn-junction between that node and the substrate enters the forward-bias condition. Then, the node voltage does not drop anymore even if a larger amount of charge is injected into the node. Because the cut-in voltage is 0.7 V, ΔV maintains a constant value coming from $V_{\text{center}} - \Delta V = -0.7$ V. It means that ϕ_{disp} also has a constant value when ΔV is larger than $V_{\text{center}} + 0.7$. The model equation of ϕ_{disp} in this condition is expressed by

$$\phi_{\text{disp}} = \Gamma_{\text{max}} \frac{(V_{\text{center}} + 0.7)}{V_{\text{swing}}}. \quad (3.4)$$

To verify model equations (3.3) and (3.4), phase displacement calculated with model equations is compared to that obtained from transistor-level simulation. Figure 3.4 illustrates the comparison result

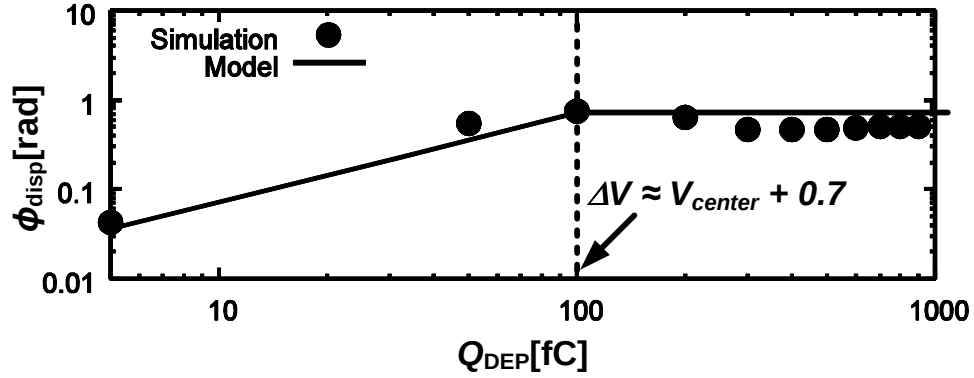


Figure 3.4: Simulation results of ϕ_{disp} and trend-lines calculated using (3.3) versus Q_{DEP} .

between the model equations and the simulation. As the input parameter, Q_{DEP} is swept from 5 fC to almost 1000 fC. The other parameters use values given in Table 3.1. Since ΔV meets the limitation caused by the cut-in voltage at around 100 fC of Q_{DEP} , Equation (3.4) is used to calculate ϕ_{disp} beyond 100 fC. The comparison indicates that the maximum difference is 0.26 radian at 300 fC of Q_{DEP} . The difference of ϕ_{disp} can be converted to that of the perturbed clock period (t_{per}) using Equation (3.1). The discrepancy in t_{per} is less than 105 ps under the condition, which is 2.5 ns of the nominal clock period.

Charge Pump

The radiation strike at the CP leads to voltage perturbation on the control voltage (V_{ctrl}), which is the CP output node voltage. Since the control voltage (V_{ctrl}) is a DC signal unlike the signal on the VCO, it is unnecessary to consider the time of the radiation strike. The voltage perturbation on V_{ctrl} (ΔV) can be calculated using

$$\Delta V = \frac{Q_{\text{DEP}}}{C_2}. \quad (3.5)$$

The LF capacitance of C_2 represents the node capacitance of the CP output because it is large enough compared with the parasitic capacitance of transistors connected to the V_{ctrl} node. Note that C_1 has little impact on ΔV owing to the resistor R of the LF. This resistor R prevents instantaneous current flow caused by the charge injection.

The voltage disturbance of the V_{ctrl} modulates the frequency of the VCO with the relationship $\Delta f = K_{\text{VCO}}\Delta V$. Using (2.2), the perturbed frequency (f_{per}) is given by

$$f_{\text{per}} = f_{\text{nom}} \pm K_{\text{VCO}}\Delta V \quad (3.6)$$

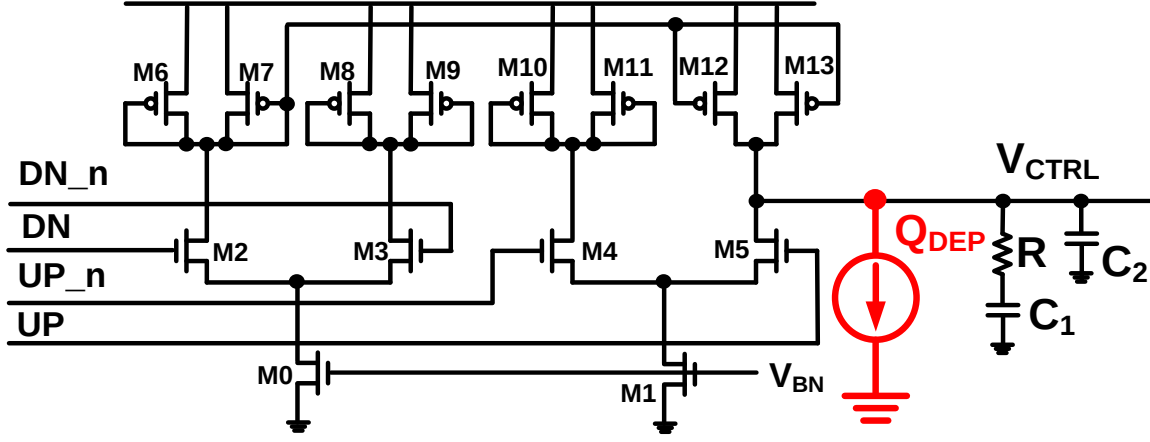


Figure 3.5: Schematic of CP used to simulate radiation-induced charge injection.

where f_{nom} is the nominal frequency of the VCO in the PLL-locking condition. Since the t_{per} of Equation (3.1) is the inverse of f_{per} , ϕ_{disp} can be re-expressed as

$$\phi_{\text{disp}} = \frac{2\pi \cdot |t_{\text{nom}} - 1/f_{\text{per}}|}{f_{\text{nom}}} \quad (3.7)$$

$$= \frac{2\pi \cdot |t_{\text{nom}} - 1/(f_{\text{nom}} \pm K_{\text{VCO}}\Delta V)|}{f_{\text{nom}}} \quad (3.8)$$

$$= \frac{2\pi \cdot |t_{\text{nom}} - 1/(f_{\text{nom}} \pm K_{\text{VCO}}Q_{\text{DEP}}/C_2)|}{t_{\text{nom}}}. \quad (3.9)$$

The dominant input parameter in Equation (3.9) is the same as the VCO, which is the amount of deposition charge (Q_{DEP}). The other parameters in Equation (3.9), which are t_{nom} , f_{nom} , C_2 , and K_{VCO} , has given values in a PLL design.

For a demonstration, various Q_{DEP} values are injected at the representative node discussed in Chapter 2. Figure 3.5 indicates the representative node, which is the CP output node. Figure 3.6 depicts phase displacement values obtained by the simulation and by Equation (3.9). Equation (3.9) was calculated using the parameter values given in Table 3.1. The phase displacement ϕ_{disp} in Figure 3.6 does not experience saturation at a large Q_{DEP} because C_2 is large enough to avoid voltage clipping. The discrepancy between the results obtained from Equation (3.9) and from simulation is less than 0.3 radian. The discrepancy can be expressed in terms of t_{per} because the model equation of ϕ_{disp} is derived from t_{per} . The maximum difference between t_{per} values obtained from Equation (3.6) and from simulation is 116 ps.

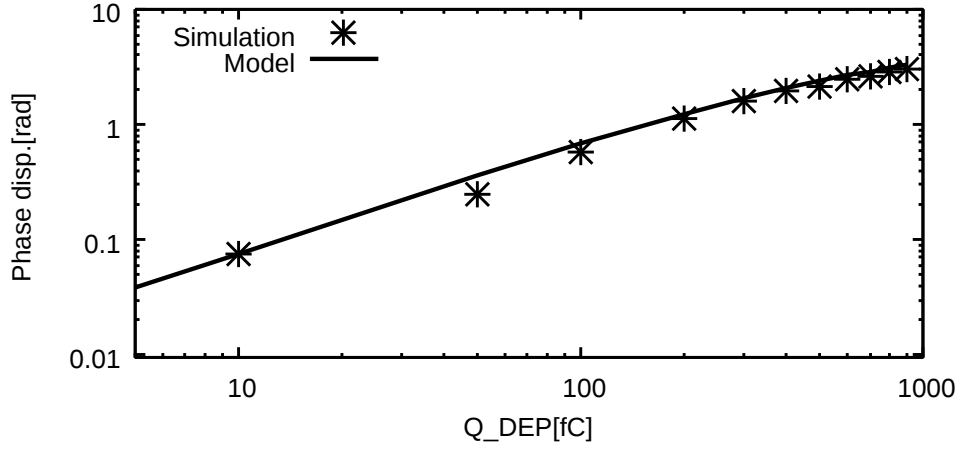


Figure 3.6: Simulation results of ϕ_{disp} and the trend-line calculated using (3.9) versus Q_{DEP} .

3.3.2 Radiation Strike at Digital Sub-Circuits

Phase-Frequency Detector

The PFD creates two consecutive incorrect pulses as a result of a radiation strike. In the basic principle of the PLL, one activated signal would lead to the other output signal of the PFD for a return to the locking condition. For example, if the UP signal is activated, the DN signal is generated in the subsequent clock cycle of the reference clock. Nevertheless, two consecutive incorrect pulses are observed as a particular feature of a radiation-induced error. Figure 3.7 illustrates the mechanism of the occurrence of the two consecutive pulses. When an SEU occurs at the D-FF generating the DN signal (DN D-FF), an incorrect pulse appears on the DN signal, as shown in Figure 3.7 (a). In a nominal condition, the PFD would compare ‘edge1’ on the reference clock (CLK_div) with ‘edge2’ on the divided clock (CLK_div). However, ‘edge2’ is compared with ‘edge3’ because the ‘edge1’ is used to reset the D-FFs in the PFD. As a result, the PFD recognizes that CLK_div leads CLK_ref even if the actual situation is opposite. Similar to the DN signal, the UP signal has two consecutive pulses as result of an SEU.

The amount of the phase displacement is a function of the width of incorrect pulse (t_{pul}). The voltage disturbance on V_{ctrl} (ΔV) is attributed to activation of the DN signal or the UP signal. Wider pulse on the DN signal or the UP signal produces a large ΔV . The ΔV is proportional to VCO’s frequency modulation, which causes the perturbed clock period (t_{per}). Hence, the width of incorrect pulse (t_{pul}) should be firstly modeled. Modeling t_{pul} is divided into two cases - UP signal modeling

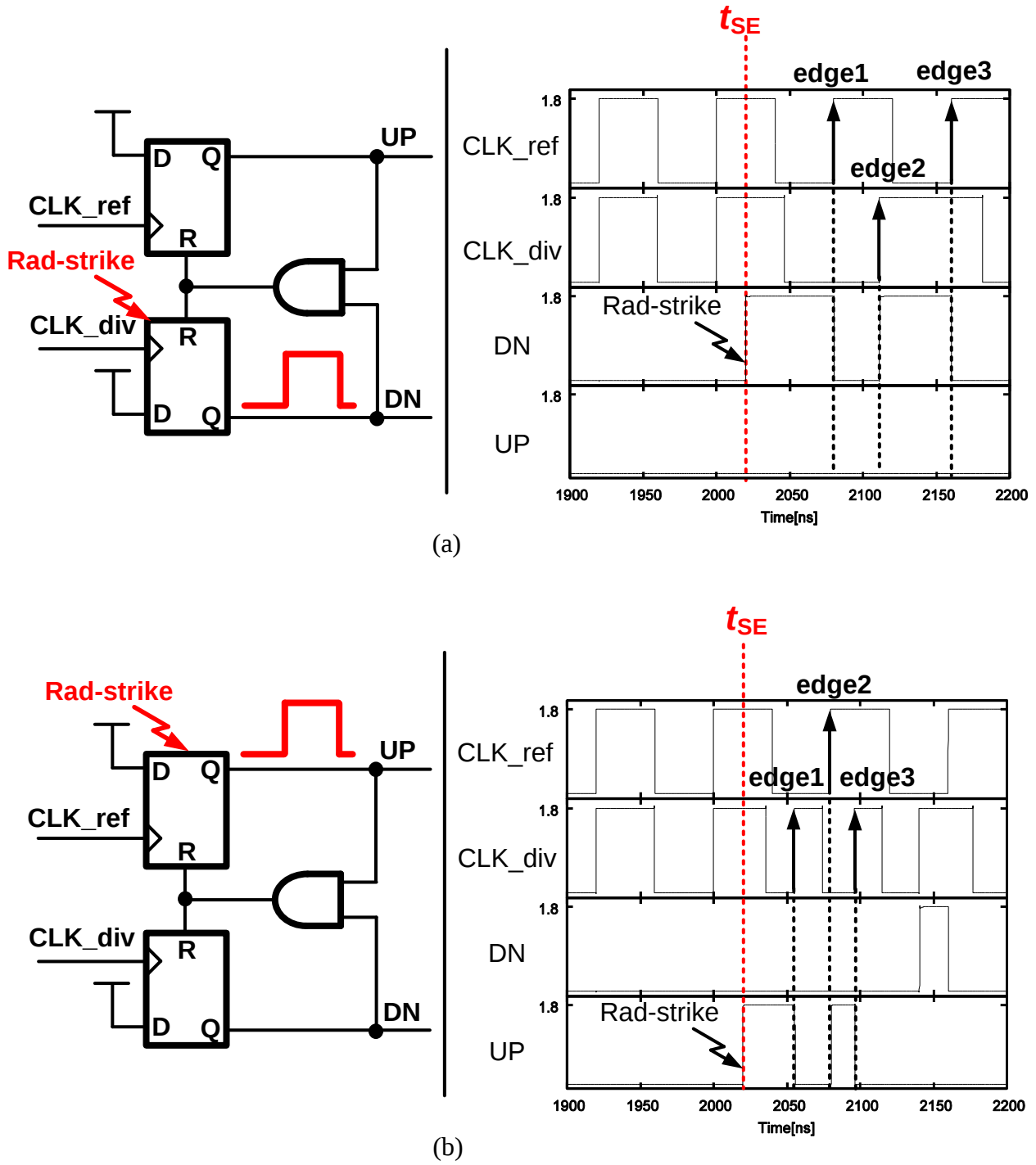


Figure 3.7: Mechanism of occurrence of two consecutive pulses when a radiation strike hits the D-FF for (a) the DN signal and (b) the UP signal.

and DN signal modeling. As mentioned above, radiation strikes at the PFD leads to two consecutive pulses. In case of the DN signal, the time to charge the LF is the sum of pulse widths of the first pulse and the second pulse. The width of the first pulse (t_{pul1}) is the duration from a timing of a radiation strike (t_{SE}) to the next rising edge of the reference clock (t_{edge1}), as shown in Figure 3.7 (a). The width of the first pulse (t_{pul2}) is the duration from ‘edge2’ (t_{edge2}) to ‘edge3’ (t_{edge3}), as shown in Figure 3.7 (a). The width of incorrect pulse (t_{puldn}) to produce ΔV can be approximated by the duration from t_{SE} to t_{edge3} , which is expressed as

$$\text{DN signal : } t_{pul} = t_{edge1} - t_{SE} + t_{ref}, \quad (3.10)$$

where t_{ref} is the period of the reference clock. Actually, t_{pul} in Equation (3.10) is overestimated because it includes the non-activation time between the first pulse and the second pulse. The control voltage V_{ctrl} decreases during the non-activation time although the current sources are turned off. Figure 3.7 shows the mechanism of decreasing V_{ctrl} during the non-activation time. The resistor R in Figure 3.8 (a) prevents current flow from the CP to the C_1 , almost all of the current charges C_2 during the activation of the first pulse. The potentials between two terminals of the resistor R are difference. For this reason, the charges in C_2 go to C_1 after the current source are turning off, as shown in Figure 3.8 (a). This phenomenon causes the decrease of V_{ctrl} during the non-activation time, as indicated in Figure 3.8 (c). Nevertheless, the overestimation of t_{pul} can give an acceptable result due to a limited range of change of V_{ctrl} . The limited range of change of V_{ctrl} ensures that the transistors implement the current sources of the CP are turned on. The limited range reduces the discrepancy caused by the overestimation from the actual result. The model of the UP signal width (t_{pulup}) uses also an approximation for simplicity. The width of the first UP pulse has the maximum value when ‘edge1’ in Figure 3.7 (b) comes close to ‘edge1’. Since the UP signal is activated, ‘edge1’ cannot lag behind ‘edge2’ of the reference clock. In UP signal modeling, the second pulse is ignore. Due to the activation of the UP signal, ‘edge3’ comes close to ‘edge2’. It means the second pulse has a quite narrow width compare to that of the first pulse. Thus, the width of the UP signal t_{pulup} can be calculated by

$$\text{UP signal : } t_{pul} = t_{edge2} - t_{SE}. \quad (3.11)$$

In Equation (3.10) and (3.11), the both parameters t_{edge1} and t_{edge2} address the same timing, which is

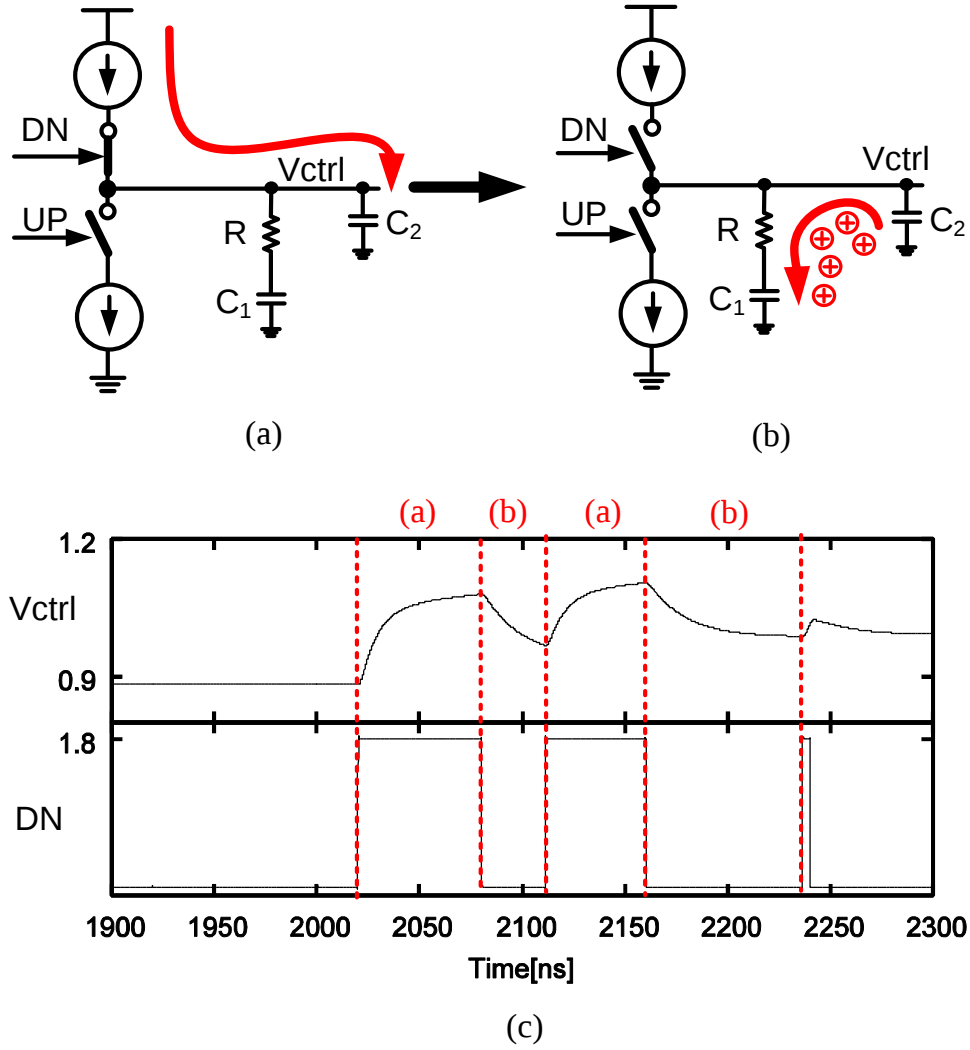


Figure 3.8: Conceptual charge movement (a) during activation of incorrect pulse and (b) after incorrect pulse disappears. (c) Change of V_{ctrl} .

the first rising edge on the reference clock appearing after t_{SE} .

The next step is modeling the voltage disturbance (ΔV) as a function of the width of the incorrect pulse (t_{pul}). The step-function response of the LF is the voltage disturbance. The step function is the current created by the current sources of the CP and its width is t_{pul} . In the frequency domain, the

voltage disturbance (ΔV) can be expressed by

$$\Delta V(s) = I_{CP}(s) \left\{ \left(R + \frac{1}{sC_1} \right) \parallel \frac{1}{sC_2} \right\} \quad (3.12)$$

$$= I_{CP} \frac{(1 - e^{st_{pul}})}{s} \left\{ \left(R + \frac{1}{sC_1} \right) \parallel \frac{1}{sC_2} \right\}, \quad (3.13)$$

where $I_{CP}(s)$ is the step function created by the current source of the CP and t_{pul} can be t_{pul} . The voltage disturbance ($\Delta V(t)$) in the time domain can be obtained after performing the inverse Laplace transform as follows:

$$V_{ctrl} \leq V_{ctrl,min}: \quad \Delta V(t_{pul}) = V_{ctrl,lock} - V_{ctrl,min} \quad (3.14)$$

$$V_{ctrl,min} < V_{ctrl} < V_{ctrl,max}: \quad \Delta V(t_{pul}) = \frac{I_{CP}}{C_1 + C_2} \left\{ t_{pul} + \frac{C_1^2 R}{C_1 + C_2} \left(1 - e^{-\frac{C_1 + C_2}{C_1 C_2 R} t_{pul}} \right) \right\} \quad (3.15)$$

$$V_{ctrl} \geq V_{ctrl,max}: \quad \Delta V(t_{pul}) = V_{ctrl,max} - V_{ctrl,lock}, \quad (3.16)$$

$$(3.17)$$

where $V_{ctrl,min}$ and $V_{ctrl,max}$ are the boundaries of the limited range of V_{ctrl} , $V_{ctrl,lock}$ is the control voltage in the locking condition. The pulse width (t_{pul}) is determined by the input parameter t_{SE} . The other parameter values are given from designed PLLs.

The final step is deriving the model equation of the phase displacement using Equation (3.1). The model equation of the phase displacement has been already obtained as a function of ΔV in the previous section, which is Equation (3.8). Using Equation (3.8), the model equation of the phase displacement when a radiation strike occurs at the PFD as follows:

$$\phi_{disp} = \frac{2\pi \cdot |t_{nom} - 1/(f_{nom} \pm K_{VCO} \Delta V(t_{pul}))|}{t_{nom}}. \quad (3.18)$$

The input parameters of Equation (3.18) are the timing of the radiation strike (t_{SE}), types of D-FFs (UP D-FF or DN D-FF), and the deposition charge Q_{DEP} . Note that Equation (3.18) is not proportional to Q_{DEP} unlike the phase displacement originated from the analog sub-circuits. The deposition charge Q_{DEP} is used to check whether the radiation strike induces an SEU in D-FFs or not. The minimum charge to create SEUs in D-FFs is called critical charge (Q_{crit}). The critical charge Q_{crit} can be found with the transistor-level simulation. If the deposition charge Q_{DEP} is smaller than Q_{crit} , there is no phase

Table 3.2: Characteristic table of SR latch.

S	R	Q	$\overline{Q}$
1	1	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
0	0	1	1

displacement on the PLL.

To verify the model presented in this section, radiation-induced charge of $Q_{\text{DEP}} = 50$ fC is injected into a node in which the latch is in charge of the DN signal (DN latch), as illustrated in Figure 3.9. 50 fC of Q_{DEP} is larger than Q_{crit} in the PLL designed with $0.18 \mu\text{m}$ CMOS process. Since the phase displacement depends on the input parameter t_{SE} , various values are used for t_{SE} . As mentioned above, the width of the incorrect pulse is the duration between t_{SE} and the first rising edge on the reference clock appearing after t_{SE} . It means the t_{SE} should span 0 to t_{ref} in a clock cycle. In this verification, t_{ref} is 80 ns as the frequency of the reference clock is 12.5 MHz. However, a radiation strike occurring in the second half of the t_{ref} has no impact on the PFD output due to the characteristics of the SR latch of the PFD. The SR latch is depicted in the red square of Figure 3.9. The reset input (R in Figure 3.9) is equivalent to the reference clock (CLK_ref) and the set input (S in Figure 3.9) maintains HIGH. Figure 3.10 depicts the input and output waveforms of the DN latch. In Figure 3.10, we can see that the reset input is LOW during the second half of the t_{ref} . When the reset input is LOW and the set input is HIGH, the SR-latch outputs are forced as $Q=0$ and $\overline{Q}=1$ in Table 3.2. The outputs of the SR latch has no SEU even though a radiation strike occurs at the SR latch. Therefore, the t_{SE} is swept during the first half of t_{ref} . Figure 3.11 depicts a comparison of ϕ_{disp} obtained by SPICE simulation and Equations (3.18) for several t_{SE} values. The results in Figure 3.11 show saturated ϕ_{disp} for every t_{SE} . This is because ΔV reaches the boundaries of the limited range of V_{ctrl} . In case of the DN signal, the discrepancy between the result of SPICE simulation and that of the model equations is less than 0.331 radian. The maximum difference between t_{per} values obtained from Equation (3.18) and from simulation is 132 ps. The UP signal discrepancy of the ϕ_{disp} is less than 0.178 radian and that of the t_{per} is less than 20 ps.

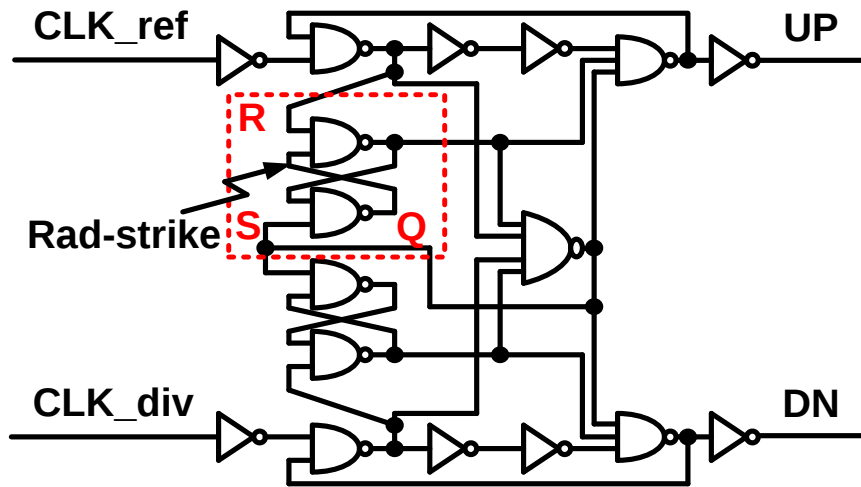


Figure 3.9: PFD schematic used to simulate radiation-induced charge injection.

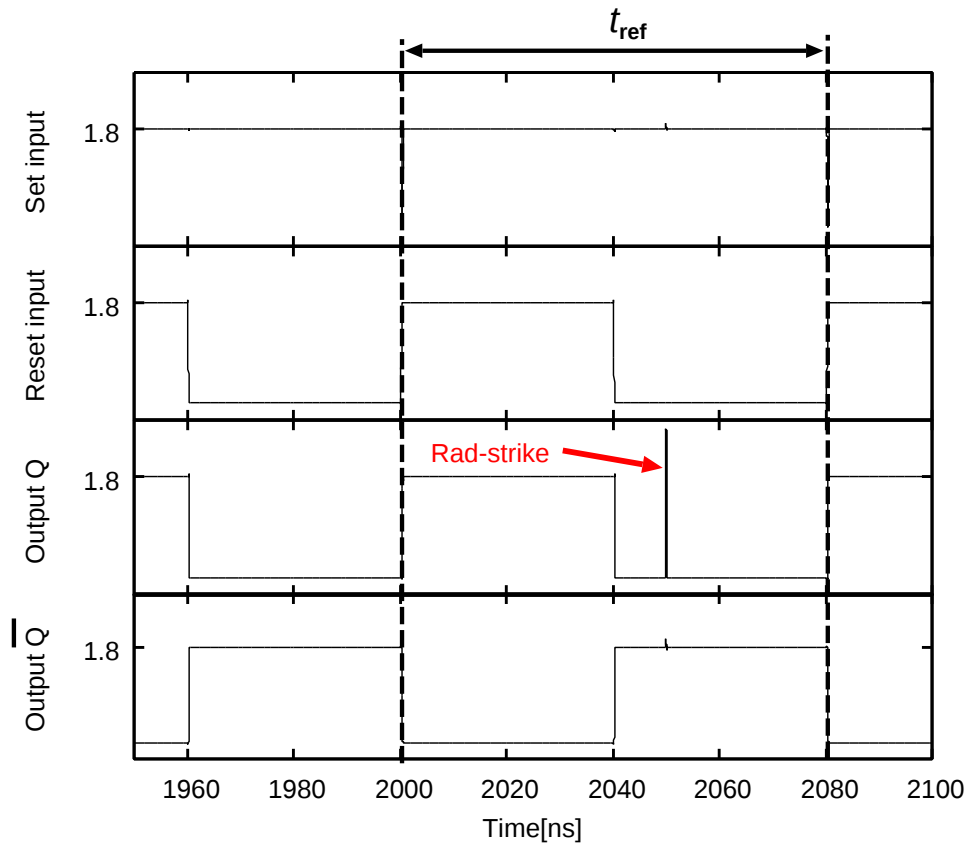


Figure 3.10: Inputs and output of the DN latch when a radiation strike arises at a time of the second half of the t_{ref} .

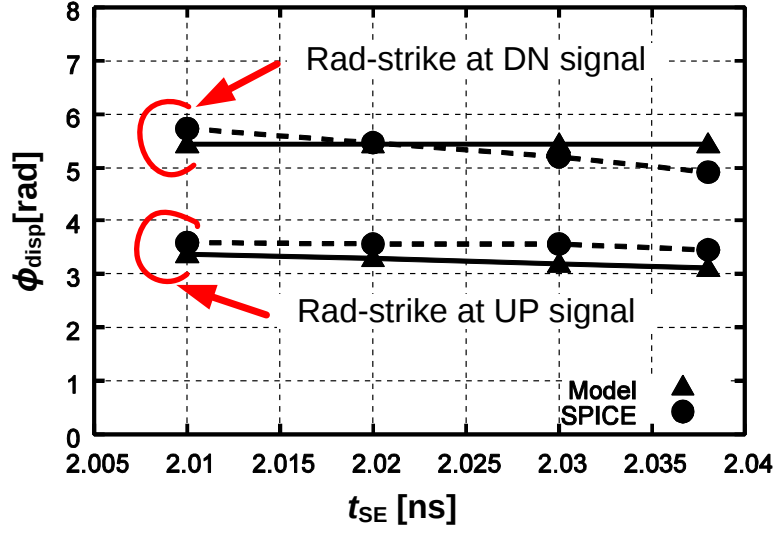


Figure 3.11: Comparison of ϕ_{disp} obtained by SPICE simulation and Equation (3.18).

Divider

The clock at the divider's output (CLK_div) should be identical to the reference clock (CLK_ref) in the locking condition. An SEU (or SET) at D-FF generates a perturbation of CLK_div, which turns out to be at variance with the CLK_ref. Owing to the difference in periods between CLK_ref and CLK_div, the UP or DN signal at the PFD's output has an incorrect pulse.

In the divider, the perturbed period caused by an SE ($t_{per,div}$) depends on the order of the unit divider and on the types of errors occurring in the D-FF (SEU or SET). As mentioned in the previous chapter, a unit divider that is closer to the PFD generates the larger perturbation on CLK_div when a radiation strike occurs. SETs are equivalent to SEUs in the subsequent stage of the unit divider. The perturbed period on the divided clock $t_{per,div}$ for all cases have been examined through the transistor-level simulation. The perturbed period of $t_{per,div}$ can be summarized as

$$\text{SEU :} \quad t_{per,div} = t_{nom}(2^K - 2^{D-1}) \quad (3.19)$$

$$\text{SET :} \quad t_{per,div} = t_{nom}(2^K - 2^D) \quad (3.20)$$

$$\text{No failure :} \quad t_{per,div} = t_{nom}2^K, \quad (3.21)$$

where K is the total number of unit dividers and D denotes the order of the unit divider. If a unit divider is $D = 1$, it is the first stage of the divider chain. The final stage of the divider chain is expressed as

$D = K$. As denoted in (3.1), t_{nom} is the period of the PLL output clock in the locking condition and $t_{\text{nom}}2^K$ is identical to t_{ref} . Since the PFD detects the phase difference between CLK_div and CLK_ref, the pulse width at the PFD output (t_{pul}) can be calculated by subtracting $t_{\text{nom}}2^K$ from Equations (3.19), (3.20), and (3.21), as follows:

$$\text{SEU :} \quad t_{\text{pul}} = t_{\text{nom}}2^{D-1} \quad (3.22)$$

$$\text{SET :} \quad t_{\text{pul}} = t_{\text{nom}}2^D \quad (3.23)$$

$$\text{No failure :} \quad t_{\text{pul}} = 0. \quad (3.24)$$

The pulse caused by the divided clock's perturbation is propagated to the PLL output through the CP, LF, and VCO. Its propagation mechanism is identical to the incorrect pulse owing to a radiation strike at the PFD. The results from Equations (3.22), (3.23), and (3.24) are applied to Equation (3.15) are applied to Equation (3.15) to ΔV at CP output. Then, the phase displacement ϕ_{disp} can be found using the obtained ΔV and Equation (3.18). The input parameters in this model are the unit divider suffering from a radiation strike (D) and the deposition charge Q_{DEP} . The deposition charge Q_{DEP} is used to check whether the radiation strike induces an SEU in D-FFs or not.

Figure 3.12 shows comparison of ϕ_{disp} obtained from SPICE simulation and model calculation to verify this model. The radiation-induced charge Q_{DEP} of 50 fC is injected during the LOW clock state of unit dividers to induce an SEU. Figure 3.13 illustrates the circuit diagram of the 5-stage divider with the charge-injected node. The difference of ϕ_{disp} between the result of the SPICE simulation and that of the model is less than 0.56 radian. The maximum discrepancy of the t_{per} is 220 ps.

3.4 Summary

This chapter presented an analytical model of phase displacement on PLL clock under radiation. The phase displacement was defined to quantify the radiation-induced clock perturbation. The definition of the phase displacement is based on the difference between the perturbed clock period and the nominal clock period at PLL output. The analytical model to calculate the phase displacement were divided into four parts, which are radiation strikes occurs at the VCO, the CP, the PFD, and the Divider. The input parameters are the deposition charge, the locations and the timings of radiation strikes. For the analog sub-circuits (the VCO and the CP), the dominant input parameter is the deposition charge.

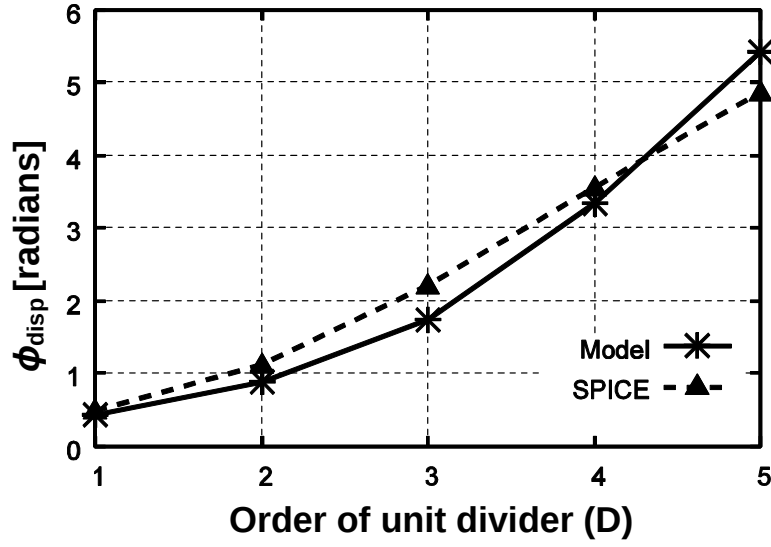


Figure 3.12: Results of SPICE simulation and model calculation when an SEU occurs at each unit divider.

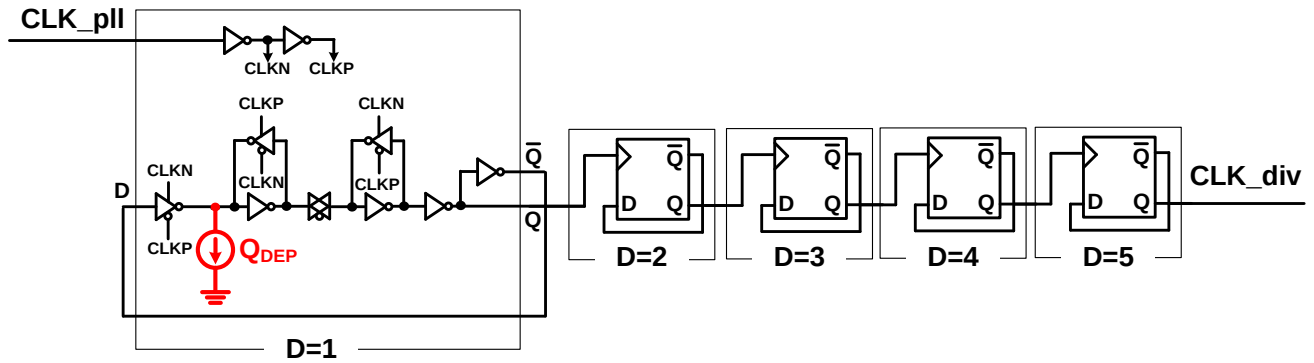


Figure 3.13: Circuit diagram of the 5-stage divider with charge injection.

The phase displacement is almost proportional to the deposition charge. The digital sub-circuits (the PFD and the Divider) is mainly affected by the locations and the timings of radiation strikes. The deposition charge is only used to check whether it is larger than the critical charge. The critical charge is the minimum charge to cause SEUs in storage elements such as D-FFs. In the PFD, the locations of radiation strikes (DN D-FF or UP D-FF) have impact on the phase displacement along with the timings of radiation strikes. In the Divider, the dominant input parameter is the locations of radiation strikes, which is the unit divider suffering from radiation strikes (D). These input parameters of the analytical model is summarized in Table 3.3. To verify the analytical model, the phase displacement from the analytical model was compared to that from transistor-level simulation. The difference of the perturbed

Table 3.3: Input parameters of analytical model for sub-circuits hit by radiation strikes.

Sub-circuits	Input parameters
VCO	Q_{DEP}
CP	Q_{DEP}
PFD	t_{SE} , UP D-FF or DN D-FF, Q_{DEP}
Divider	D , Q_{DEP}

clock periods between the two results was less than 220 ps in 2.5 ns of the nominal clock period. The maximum discrepancy in the phase displacement was 0.56 radian.

Chapter 4

Behavioral Modeling to Evaluate Clock Recovery Time under Radiation

4.1 Introduction

This chapter discusses modeling of PLL's recovery behavior from radiation-induced perturbation. Evaluation of recovery time from a perturbation is also important in RH-PLL design because the basic concept of the cost-saving techniques is to reduce the recovery time. The analytical model presented in Chapter 3 provides phase displacement as its result. However, a model equation for the recovery time leads to high complexity. Because the recovery time is related to the locking characteristics, the model equation should be developed based on the transfer function of the whole PLL. PLL has at least second-order transfer function, which is caused by the VCO and the LF. A conventional LF design consists of two capacitors and one resistor. In this case, the PLL has third-order transfer function. Thus, simulation-based evaluation is more efficient for the analysis of recovery time. As mentioned in previous chapters, transistor-level simulations lead to the brute-force analysis and takes long analysis time. For these reasons, use of behavioral model is an adequate choice to evaluate the recovery time.

The first part of this chapter describes the definition of the recovery time. The second part explains behavioral modeling of PLLs recovery characteristics from radiation-induced perturbation. The analysis results found in Chapter 2 and Chapter 3 are embedded in behavioral models. The behavioral model is implemented with Verilog-A. The third part demonstrates a conventional PLL to evaluate vulnerability to radiation using the analytical and behavioral models. The demonstration gives phase

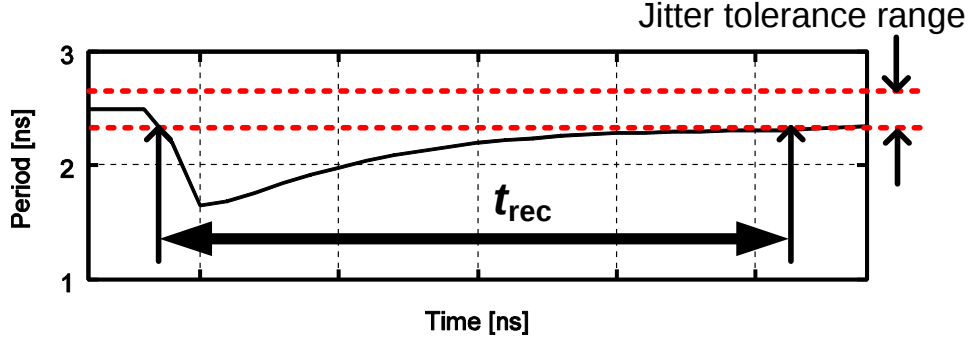


Figure 4.1: Definition of the recovery time (t_{rec}).

displacement and recovery time of the conventional PLL. The final part validates the evaluation results with experimental testing of radiation. The PLL is fabricated in a $0.18 \mu\text{m}$ CMOS process for the radiation test.

4.2 Definition of Recovery Time

Recovery time (t_{rec}) is the duration from the onset of clock perturbation to re-locking. To calculate t_{rec} in practice, it is important to define the clock-perturbation onset and re-locking. In PLL operation, an erroneous clock cycle means a clock cycle that violates the jitter specifications of a target application. Thus, the onset of the clock perturbation can be defined as the time when a clock cycle is observed to violate the jitter specifications. Similarly, the re-locking moment is when the clock cycle returns to within the jitter specification. Figure 4.1 is a conceptual graph to explain the definition of the recovery time. It shows a deviation in the PLL clock periods caused by a radiation strike (solid line) and also shows the jitter tolerance range (broken line). The duration between the crossing points of the solid and broken lines is the t_{rec} .

4.3 Behavioral Modeling of Radiation-Induced Errors

Figure 4.2 illustrates the concept of the behavioral model to simulate radiation strikes on PLLs. The PFD experiences a radiation strike as an example of the behavioral model. PLL behavioral models consist of sub-circuit behavioral models. The behavioral model of radiation-induced errors, which is called ‘error behavioral model’ in this work, is embedded into the sub-circuit behavioral models. The

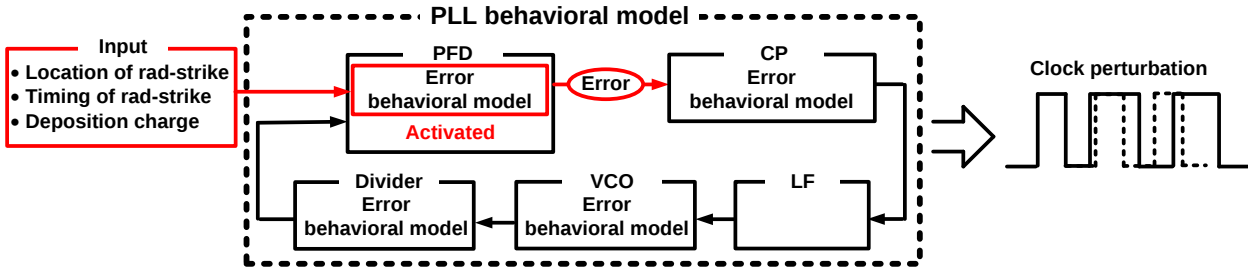


Figure 4.2: Concept of behavioral model of radiation-induced error using an example. The example is a case of a radiation strike occurring at the PFD.

Table 4.1: Inputs and output of error behavioral model.

Sub-circuits	Inputs	Outputs
VCO	$\phi_{\text{disp}}(Q_{\text{DEP}})$ using Equation (3.3) and (3.4)	Phase shift
CP	$I_{\text{rad}}(Q_{\text{DEP}}, t)$ using Equation (2.1)	Voltage disturbance
PFD	t_{SE} & D-FF suffering from radiation strike	Incorrect pulse
Divider	t_{SE} & unit divider suffering from radiation strike	Perturbation on divided clock

error behavioral model needs input parameter values to create errors as its output. The PLL behavioral models generate perturbed clocks due to the errors created by the error behavioral model. If the input parameters of the error behavioral model have no value, the PLL behavioral model is simulated in non-radiation condition. Table 4.1 shows the input parameters of the error behavioral model for each sub-circuit and their outputs. In this section, behavioral models are implemented with Verilog-A [48]. The PLL behavioral model used in this section is modeled based on the conventional low-jitter PLL described in Chapters 2 and 3.

4.3.1 Implementation using Verilog-A

Voltage-Controlled Oscillator

Radiation-strikes at the VCO were found to lead to phase shift, which was discussed in Chapter 2. The behavioral model of radiation-induced errors is expressed by phase shift, as shown in Figure 4.3. The broken lines indicate the phase-shifted signal that the VCO generates. The amount of phase shift is denoted by ϕ_{disp} and can be calculated from three design parameters and Q_{DEP} , as given by Equation (3.3).

The model in Listing 4.1 was used to implement the behavior of the VCO and radiation-induced

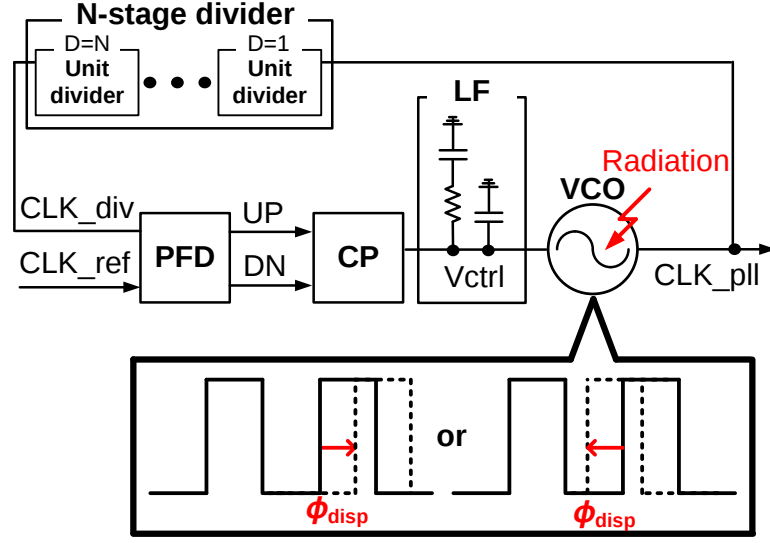


Figure 4.3: Behavioral model for radiation-induced errors occurring at VCO.

phase shift. The VCO gain (K_{VCO}) and linear range of the VCO were extracted from SPICE simulation to implement the behavior of the VCO. The conventional low-jitter PLL mentioned in Chapters 2 and 3 was used for the SPICE simulation. The linear range was from 0.3 to 1.34 V in the control voltage (V_{ctrl}) and K_{VCO} was -883 MHz/V . The VCO frequency in the linear range is computed as

$$f(t) = K_{VCO} V_{in}(t) + f_c, \quad (4.1)$$

where $V_{in}(t)$ means the control voltage (V_{ctrl}) and f_c is the center frequency that is set up as a constant. Using Equation (4.1), the VCO output voltage to create a waveform is defined as

$$v_{out,vco} = \sin\left(2\pi \int_0^t f(\tau) d\tau + \phi_{shift}\right), \quad (4.2)$$

where ϕ_{shift} denotes the amount of phase shift. The final waveform at VCO output is rectangular, has a small amount of transition time. That arises at the zero-crossing moment of $v_{out,vco}$. The initial value of ϕ_{shift} is zero but it has some other value due to noises such as that from radiation strikes. The remaining routine reveals phase displacement after checking whether a radiation strike has occurred at the VCO or not. The amount of radiation-induced phase displacement can be calculated by Equations (3.3) and (3.4).

Listing 4.1: VCO and radiation-induced phase shift

```

'include "discipline.h"
'include "constants.h"

module vco(vin, vout, vstart);
input vin;      output vout, vstart;
electrical vin, vout, vstart;
parameter real center_freq=0, center_freq2=883.0M;
parameter real K_vco1 = -883.0M, K_vco2 = -335.0M;
parameter real vlogic_high = 5, vlogic_low = 0;
parameter real tdel = 0 from [0: inf), trise = 1p from [0: inf), tfall = 1p from [0: inf);
parameter real vth1=1.34, vth2=0.3, vth3=0.01;
parameter real t_disturb = 2u, phi_dis = 0;
real freq, vout_val, sig, phi, t_strike, t0, t;
integer disturb, strike;
// Compute VCO frequency in linear range
analog begin
  if (V(vin) >= vth1) begin
    freq = 0;
  end else if (V(vin) >= vth2) begin
    freq = center_freq + K_vco1*(V(vin)-vth1);
  end else if (V(vin) >= vth3) begin
    freq = center_freq2 + K_vco2*(V(vin)-vth2);
  end else begin
    freq = 0;
  end
  // Generate output waveform of VCO
  sig = sin(2.0*3.141592654*freq, 0-1e-14) + phi);
  // Generate rectangular waveform & check whether radiation strike occurs or not
  @(cross(sig, 0, 0.01p)) begin
    vout_val = (sig > 0.0)? vlogic_high : vlogic_low;
    t0 = t;
    t = $abstime;
    if (disturb && sig > 0.0) begin
      t_strike = $abstime + (t - t0) / 4 * 3;
    end
  end
  // Reveal phase displacement at radiation strike
  @(timer(t_disturb))
    disturb = 1;
  @(timer(t_strike)) begin
    if (disturb) begin
      phi = phi_dis;
      disturb = 0;
      strike = 1;
    end
  end
  V(vout) <+ transition(vout_val, tdel, trise, tfall);
end
endmodule

```

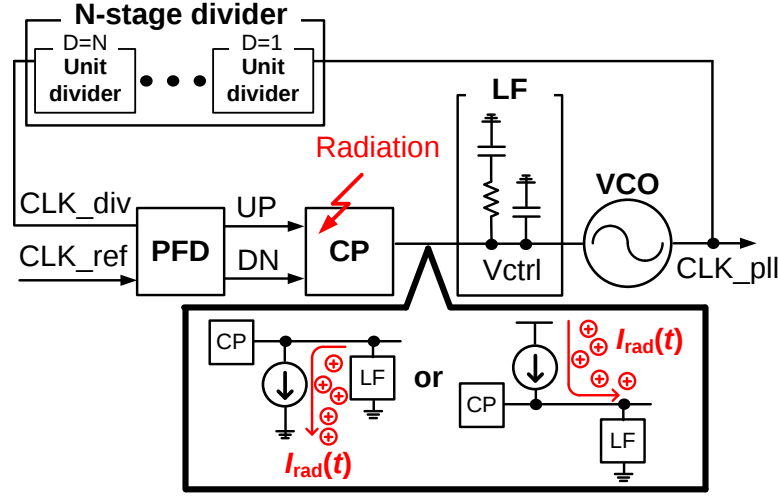


Figure 4.4: Behavioral model for radiation-induced errors occurring at CP.

Charge Pump

A radiation strike at the CP causes voltage disturbance on V_{ctrl} due to charge injection. The behavioral model is a time-variant current-source ($I_{rad}(t)$) that is equivalent to charge injection. The injected charge (Q_{DEP}) mainly determines the amount of I_{rad} , as shown in Equation (2.1).

The model in Listing 4.2 was used to implement the behavior of the CP. The radiation-induced error at the CP, which is charge injection, is modeled with an exponential current source at the circuit level. The CP is simply modeled with two current sources to charge and discharge the LF. These current sources are characterized by look-up tables that are extracted from SPICE simulation to improve the accuracy of the model. The control voltage (V_{ctrl}) in the structure of the conventional low-jitter PLL adjusts the amount of CP current through feedback. The look-up table describes the dependence between V_{ctrl} and CP current. Once the UP signal or the DN signal is driven as CP input, the model in Listing 4.2 selects one of two look-up tables. The activated UP signal calls the look-up table to characterize discharge because the K_{VCO} is negative in this model. The DN signal calls the other look-up table to charge the LF. In addition, the LF that is connected to CP output is modeled at the circuit level.

Phase-Frequency Detector

The radiation-induced error at the PFD is an incorrect pulse on the UP signal or DN signal illustrated in Figure 4.5. The incorrect pulses are attributed to SEUs on D-FFs that comprise the PFD. A data flip is applied to one of two D-FFs in the behavioral model to generate an UP signal or a DN signal. The

Listing 4.2: Behavioral model of CP

```

include "discipline.h"
include "constants.h"

module charge_pump(siginc, sigdec, vout, vsrc);
input siginc, sigdec;
inout vout, vsrc;
electrical siginc, sigdec, vout, vsrc;
parameter real vtrans = 2.5;
parameter real tdel=0 from [0:inf), trise=1n from (0:inf), tfall=1n from (0:inf);
parameter string inmos_model = "./inmos.data", ipmos_model = "./ipmos.data";
integer i_state;
real iamp;
// Function to check input signal – none signal or UP signal or DN signal
analog function integer i_mult;
input inc, dec, vtrans;
real inc, dec, vtrans;
integer inc_high, dec_high;

begin
    inc_high = inc > vtrans;
    dec_high = dec > vtrans;
    i_mult = 0;
    if (inc_high == dec_high) begin
        i_mult = 0;
    end else if (inc_high) begin
        i_mult = -1;
    end else if (dec_high) begin
        i_mult = 1;
    end
end
endfunction

analog begin
    // Select whether CP charges or discharges depending on 'inc' and 'dec' variable
    @ ( initial_step ) begin
        i_state = i_mult (V(siginc), V(sigdec), vtrans);
    end
    @ (cross(V(siginc) - vtrans, 0)) begin
        i_state = i_mult (V(siginc), V(sigdec), vtrans);
    end
    @ (cross(V(sigdec) - vtrans, 0)) begin
        i_state = i_mult (V(siginc), V(sigdec), vtrans);
    end
    // Generate CP current referring to look-up table
    if (i_state == 0) begin
        iamp = 0.0;
    end else if (i_state == 1) begin
        iamp = $table_model(V(vout), ipmos_model, "3L");
    end else if (i_state == -1) begin
        iamp = $table_model(V(vout), inmos_model, "3L");
    end
    I(vsrc, vout) <+ iamp * transition ( i_state, tdel, trise, tfall );
end
endmodule

```

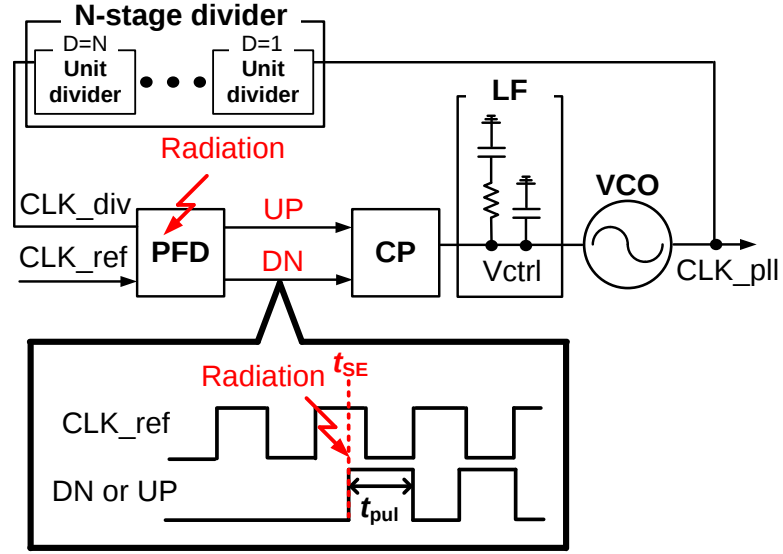


Figure 4.5: Behavioral model for radiation-induced error occurring at PFD.

time information for the radiation strike is also necessary. The time when the radiation strike occurs is denoted by t_{SE} , as shown in Figure 4.5. The behavioral model produces a data flip at t_{SE} . The data flip leads to an incorrect pulse and the incorrect pulse remains until the subsequent rising edge of the reference clock (CLK_ref) or the divided clock (CLK_div). Then, the behavioral model of the whole PLL computes the error response caused by the incorrect pulse.

The model in Listing 4.3 implements the behavior of the PFD and the radiation-induced data flip. The behavioral model of the PFD is divided into three parts. The first part triggers flags when a rising edge occurs at its inputs, which are the reference and divided clocks. The state of the relation between the two inputs is defined in the second part as

- CLK_ref leads CLK_div
- CLK_div leads CLK_ref
- CLK_ref and CLK_div are the same.

Finally, the behavioral model generates an UP signal or a DN signal using the state defined in the second part. The behavioral model of the radiation-induced data flip receives two input parameters, which are 't_disturb' and 'striked_FF' in Listing 4.3. Input parameter 't_disturb' has a value of t_{SE} and the 'striked_FF' value selects a D-FF suffering from a radiation strike.

Listing 4.3: PFD and radiation-induced data flip

```

#include "discipline .h"
#include "constants.h"
#define behind 0
#define same 1
#define ahead 2 // Note: 'ahead' means that 'vin_if' is ahead of 'vin_lo'

module pfd(vin_if, vin_lo, sigout_inc, sigout_dec);
input vin_if, vin_lo; output sigout_inc, sigout_dec;
electrical vin_if, vin_lo, sigout_inc, sigout_dec;
parameter real vlogic_high = 5, vlogic_low = 0, vtrans = 2.5, t_disturb = 2u;
parameter real tdel = 0 from [0: inf), trise = 1p from (0: inf), tfall = 1p from (0: inf);
parameter integer striked_FF = 0; // 0: lo, 1: if
integer tpos_on_if, tpos_on_lo, state; real sigout_inc_val, sigout_dec_val;
// Initialize module && detect rising edge of reference clock and divided clock
analog begin
    @ ( initial_step ) begin
        sigout_inc_val = 0, sigout_dec_val = 0;
        state = 'same;
    end
    tpos_on_if = 0;
    @ ( cross(V(vin_if) - vtrans, +1,1p) ) tpos_on_if = 1;
    tpos_on_lo = 0;
    @ ( cross(V(vin_lo) - vtrans, +1,1p) ) tpos_on_lo = 1;
// Radiation-induced data flip
    @(timer(t_disturb)) begin
        if (striked_FF == 0) begin // Hit on LO
            if (tpos_on_lo == 0) tpos_on_lo = 1;
            else if (tpos_on_lo == 1) tpos_on_lo = 0;
        end if (striked_FF == 1) begin // Hit on IF
            if (tpos_on_if == 0) tpos_on_if = 1;
            else if (tpos_on_if == 1) tpos_on_if = 0;
        end
    end
// Define state between reference clock and divided clock
    if (tpos_on_if && tpos_on_lo) state = 'same;
    else if (tpos_on_if) begin
        if (state == 'behind) state = 'same;
        else if (state == 'same) state = 'ahead;
    end else if (tpos_on_lo) begin
        if (state == 'ahead) state = 'same;
        else if (state == 'same) state = 'behind;
    end
// Generate UP or DN signal
    if (tpos_on_if || tpos_on_lo) begin
        if (state == 'ahead) begin
            sigout_inc_val = vlogic_low, sigout_dec_val = vlogic_high;
        end else if (state == 'same) begin
            sigout_inc_val = vlogic_low, sigout_dec_val = vlogic_low;
        end else if (state == 'behind) begin
            sigout_inc_val = vlogic_high, sigout_dec_val = vlogic_low;
        end
    end
    V(sigout_inc) <+ transition( sigout_inc_val, tdel, trise, tfall );
    V(sigout_dec) <+ transition( sigout_dec_val, tdel, trise, tfall );
end
endmodule

```

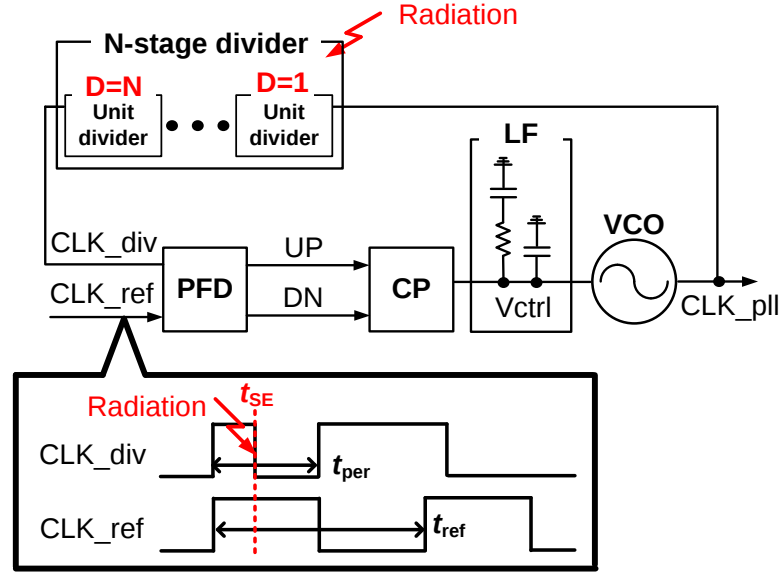


Figure 4.6: Behavioral model for radiation-induced errors occurring at divider.

Divider

The radiation-induced error of the divider is clock perturbation on the divided clock (CLK_div), as shown in Figure 4.6. The clock perturbation on CLK_div also originated from a data-flip (i.e., an SEU) on the unit divider similar to that in the PFD case. Thus, the behavioral model for radiation-induced errors has two inputs - the time when a radiation strike occurs (t_{SE}) and its location. The location of the radiation strike is in order of the unit divider, which is denoted 'D'. The location for an SET is assumed to be in a higher order of the unit divider ($D+1$) because an SET at a unit divider is equivalent to an SEU at its next unit divider according to Equations (3.19), (3.20), and (3.21).

The model in Listing 4.4 is used to implement the behavior of the unit divider and radiation-induced data flips. The behavioral model of the unit divider has two parts as well as the initialization part. The first part detects the rising edge of the input clock and the second part generates the output clock. The state of the output clock is reversed from HIGH (or LOW) to LOW (or HIGH) and is synchronized with the rising edge of the input clock. The behavioral model of radiation-induced data flips has one input parameter in terms of the time which is ' $t_disturb$ '. The location information determines the unit divider that has suffered a radiation strike that has an input parameter value of t_{SE} .

Listing 4.4: Unit divider and radiation-induced data flip

```

#include "discipline.h"
#include "constants.h"

module divider_2(vin, vout);
input vin;
output vout;
electrical vin, vout;
parameter integer divide=2;
parameter real vtrans = 2.5;
parameter real v_hi = 5.0;
parameter real v_lo = 0;
parameter real tdel=0 from [0: inf );
parameter real trise=1p from [0: inf );
parameter real tfall =1p from [0: inf );
parameter real t_disturb = 2u;

integer count;
real sigout;
integer state;
// Initialize module
analog begin
    @ ( initial_step ) begin
        count = divide/2 ;
        state = -1;
    end
// Detect rising edge of input clock
    @ (cross(V(vin) - vtrans, 1,0.01n)) begin
        count = count - 1;
        if (count == 0) begin
            state = -1 * state;
            count = divide/2;
        end
    end
// Radiation-induced data flip
    @ (timer(t_disturb)) begin
        state = -1 * state;
    end
// Generate output clock divided by 2
    if (state == -1)
        sigout = v_lo;
    else if (state == 1)
        sigout = v_hi;

    V(vout) <+ transition (sigout, tdel, trise, tfall );
end
endmodule

```

4.3.2 Simulation Results

This section discusses simulation results from the behavioral model that was implemented with Verilog-A to verify the model.

Transient Characteristics of Control Voltage (V_{ctrl})

To verify the PLL and error behavioral models, the transient voltage on V_{ctrl} from the Verilog-A simulation are compared to that from the SPICE simulation. The transient voltage on V_{ctrl} shows continuously the whole PLL operation from start up to locking. Characteristics of the PLL after an error occurs also can be examined through observing the transient voltage on V_{ctrl} .

Figures 4.7 (a) and (b) illustrate the transient characteristics of control voltage when a Q_{DEP} of 50 and 500 fC was injected into the CP output node. The simulation emulated a radiation particle hitting an nMOSFET connected to the CP output node. Free electrons caused by the radiation strike are collected in the drain of the hit nMOSFET that is CP output. The control voltage V_{ctrl} decreased instantaneously and the PLL converged toward locking conditions. The transient voltage on the V_{ctrl} shows recovery characteristics from the voltage disturbance to re-locking. The results of Verilog-A simulation have a good agreement with those of SPICE simulation for both low Q_{DEP} (50 fC) and high Q_{DEP} (500 fC).

Figures 4.8 (a) and (b) depict the transient characteristics of control voltage when an SEU occurs at an (a) UP D-FF and a (b) DN D-FF of the PFD. The SEU arises after 10 ns of a reference clock's rising edge. The SEU occurring at the D-FF activates an UP signal or a DN signal, which is the incorrect pulse. When the incorrect pulse appears on the UP signal, the V_{ctrl} decreases, as illustrated in Figures 4.8 (a). This is because K_{VCO} is a negative value. An incorrect pulse on the DN signal causes an increase of the V_{ctrl} , as illustrated in Figures 4.8 (b). Due to the huge amount of voltage perturbation, it takes longer time to re-lock than the case of a radiation strike at the CP. The results of Verilog-A simulation are consistent with those at the SPICE simulation.

Figure 4.9 illustrates the transient characteristics of control voltage when an SEU occurs at the last stage of the unit divider chain ($D = 5$). Since the clock perturbation at the divided clock only activates the DN signal, the V_{ctrl} increases. The amount of voltage perturbation is smaller than that of an SEU occurring at DN D-FF. The result of Verilog-A simulation has a good agreement with that of SPICE simulation. From Figures 4.7, 4.8, and 4.9, the level of the behavioral model's accuracy is confirmed.

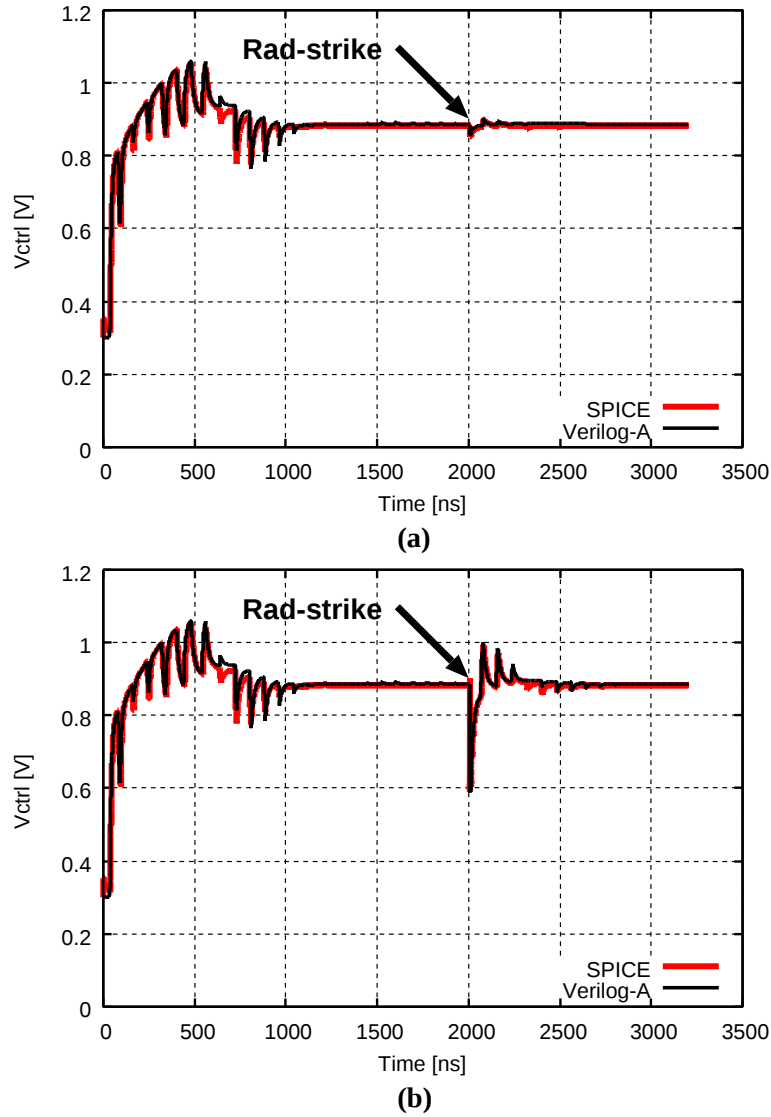


Figure 4.7: Transient voltage on control voltage when Q_{DEP} of (a) 50 fC and (b) 500 fC was injected into CP output node.

Recovery Time

Figure 4.10 shows the recovery time computed with Verilog-A and SPICE simulations when a radiation strike occurs at the CP. In both Verilog-A and SPICE simulations, charges are injected into the CP output node, which is the representative node. The locations of radiation strikes are determined as the representative node, as discussed in Chapter 3. Since the CP handles the DC signal, it is unnecessary to consider the timing of the radiation strikes. Thus, the Q_{DEP} is swept in these simulations.

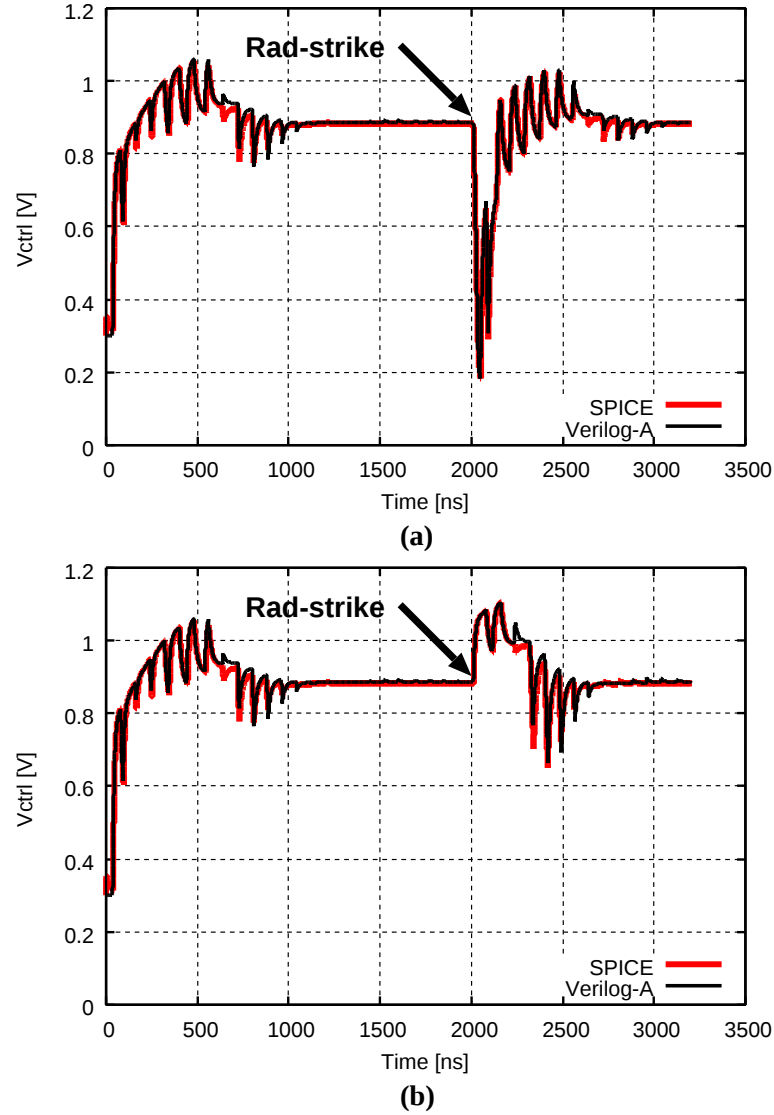


Figure 4.8: Transient characteristics of control voltage when SEU occurs at (a) UP D-FF and (b) DN D-FF of PFD.

Figures 4.11 depicts the recovery time obtained by Verilog-A and SPICE simulations when a radiation strike occurs at the PFD. For SPICE simulation, 50 fC of Q_{DEP} is injected, which is a larger value than the critical charge. The recovery time is examined for both the locations of radiation strike - UP D-FF and DN D-FF. The timings of radiation strikes are swept during the first half of the reference clock. 2.01 us in Figures 4.10 is the time after 10 ns of a reference clock's rising edge (2.0 us).

Figures 4.12 depicts the recovery time obtained by Verilog-A and SPICE simulations when a radiation strike occurs at the Divider. 50 fC of Q_{DEP} is injected into unit dividers in SPICE simulation. The

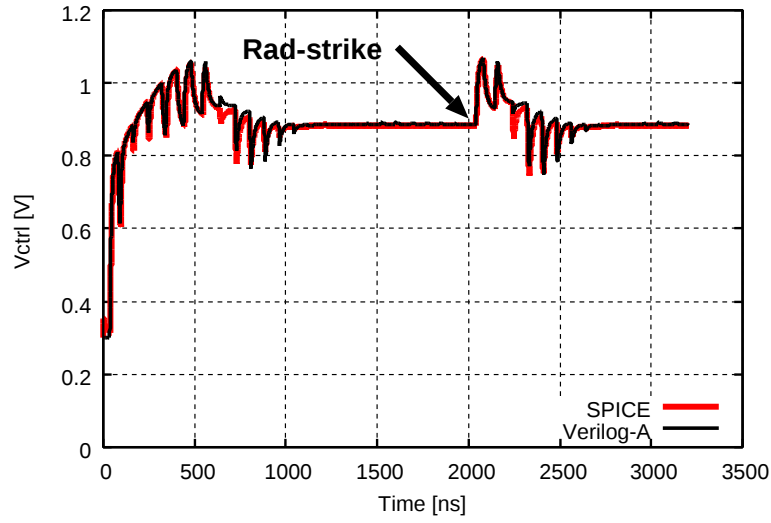


Figure 4.9: Transient characteristics of control voltage when SEU occurs at the last stage of unit divider chain ($D=5$).

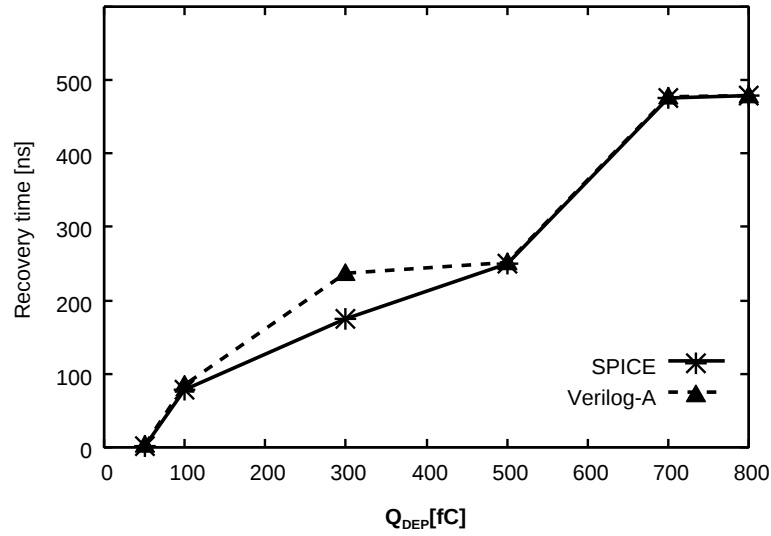


Figure 4.10: Comparison of recovery time between transistor-level and behavioral-model simulations when CP had radiation-induced errors.

recovery time is simulated for every unit divider of the 5-stages divider chain from $D = 1$ to $D = 5$. The timings of radiation strikes have almost no impact on the recovery time.

Jitter specifications to determine the recovery time were 5% cycle-to-cycle jitter. A nominal clock period (t_{rec}) is 2.5 ns. Thus, the clock is recovered if the PLL clock period returns to a range of 2.375 ~ 2.625 ns. The results from the behavioral model and transistor-level simulations had almost the same trend in all the figures. The discrepancy between the result from the SPICE simulation and that from

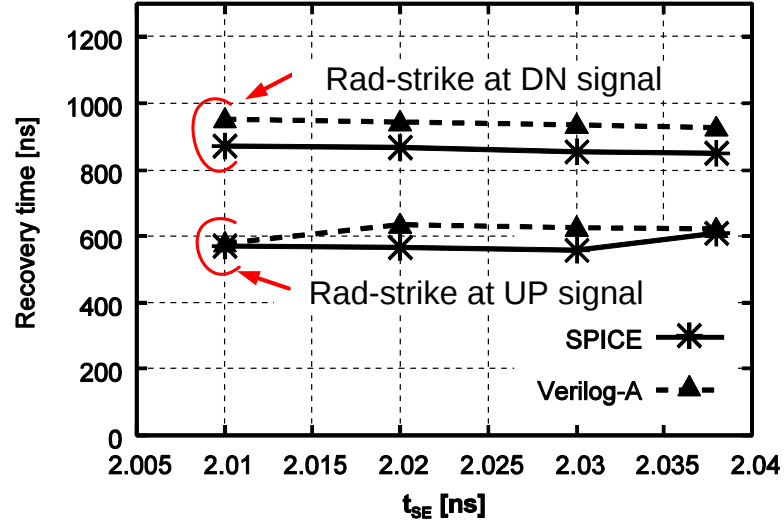


Figure 4.11: Comparison of recovery time between transistor-level and behavioral-model simulations when PFD had radiation-induced errors.

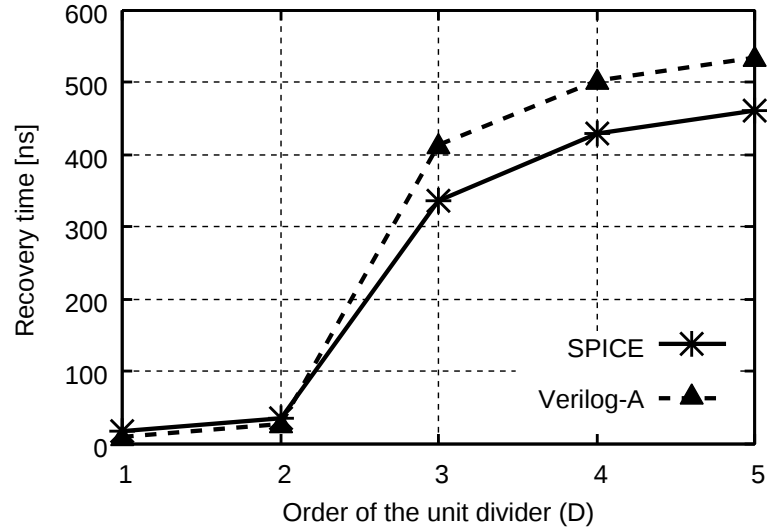


Figure 4.12: Comparison of recovery time between transistor-level and behavioral model simulations when divider had radiation-induced errors.

the Verilog-A simulation is less than about 80 ns. This discrepancy is reasonable considering that the recovery time is several hundreds nanosecond.

The main advantage of the behavioral model is simulation speed. The transient analysis in the transistor-level simulation solved equations for the whole PLL that includes a huge number of components at every time step. Furthermore, the transient analysis need to be performed until the PLL

is re-locked to examine the recovery time. It takes a long time to obtain the recovery time in the transistor-level simulation. When the recovery time was evaluated, the case of radiation strikes occurring at the PFD needed the the largest number of data (8 data points). To obtain a set of recovery time values in Figures 4.11, the simulation took one and half hours of CPU time in transistor-level simulation. However, the behavioral-model simulation took only about 27 seconds of CPU time. The behavioral model in this research accelerated simulation that was about 200 times faster than that of transistor-level simulation in CPU time.

4.4 Evaluation of PLL's Vulnerability to Radiation

This section discusses the evaluation of PLL's vulnerability to radiation based on the behavioral model that was implemented. Figure 4.13 plots the phase displacement (ϕ_{disp}) caused by radiation-induced errors for sub-circuits. The phase displacement values in Figure 4.13 are the results obtained from the behavioral-model simulation discussed in Section 4.3. As was discussed by using Equations (3.3) and (3.9), ϕ_{disp} that is caused by SETs at the VCO and CP is proportional to the depostion charge Q_{DEP} . The ϕ_{disp} values for the digital part maintain a constant value for more than 10 fC because critical charge (Q_{crit}), which is the minimum charge to flip data in D-FF, is 10 fC. Similar to Q_{crit} for the D-FF ($Q_{\text{crit,DFF}}$), Q_{crit} for the PLL ($Q_{\text{crit,PLL}}$) can be determined in terms of ϕ_{disp} . For example, we can consider jitter specifications of 5% in cycle-to-cycle jitter. The jitter specifications of 5% are equivalent to ϕ_{disp} of a 0.314 radian. If a charge of around 70 fC is injected into the VCO or the CP's node, PLL starts generating an erroneous clock that violates the 0.314 radian. The critical charge of the VCO (Q_{VCO}) and the CP (Q_{CP}) is 70 fC in this example. The PFD and the divider's critical charges ($Q_{\text{crit,PFD}}$ and $Q_{\text{crit,div}}$) are equal to $Q_{\text{crit,DFF}}$. Thus, the PLL's critical charge ($Q_{\text{crit,PLL}}$) is determined by the digital sub-circuit's critical charges ($Q_{\text{crit,PFD}}$ and $Q_{\text{crit,div}}$). It can be seen that some of the digital part is much more critical than the analog part in radiation-induced vulnerability.

Figure 4.14 plots the recovery time t_{rec} and ϕ_{disp} when radiation-induced errors occur at each sub-circuit. The t_{rec} is broadly proportional to ϕ_{disp} except for some cases. The radiation strike at the CP has larger t_{rec} than the VCO even if the ϕ_{disp} of the VCO and CP are identical. The UP signal due to the radiation strike leads to the longest t_{rec} despite moderate ϕ_{disp} in this figure. Consequently, this evaluation identified the PFD as the sub-circuit that was most vulnerable to radiation.

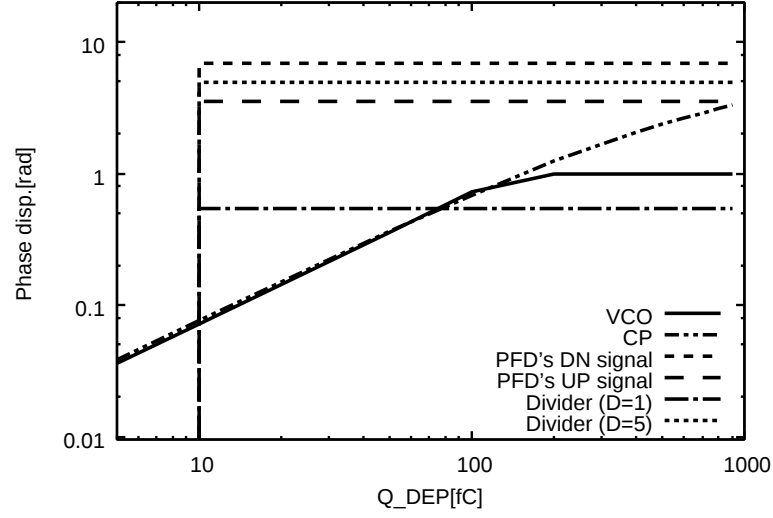


Figure 4.13: Phase displacement ϕ_{disp} caused by radiation-induced errors for each sub-circuit versus deposition charge Q_{DEP} .

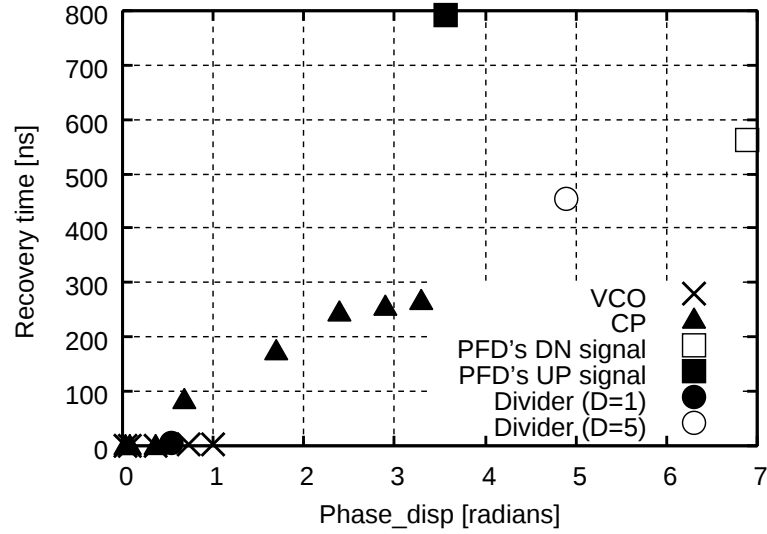


Figure 4.14: Recovery time t_{rec} and ϕ_{disp} when radiation-induced errors occur at each sub-circuit.

4.5 Experiment to Validate Results from Evaluation

Experimental testing was carried out using a set of two PLLs and an alpha-particle source (3 MBq ^{241}Am) to validate the evaluation results presented in the previous section. Figure 4.15 has a photograph of the set-up used for the radiation test with the alpha-particle source. Figure 4.16 has a micrograph of tested PLLs that were designed and fabricated with a $0.18\ \mu\text{m}$ CMOS process.

The critical charge of the digital sub-circuits ($Q_{\text{crit,PFD}}$ and $Q_{\text{crit,div}}$) was 10 fC according to the

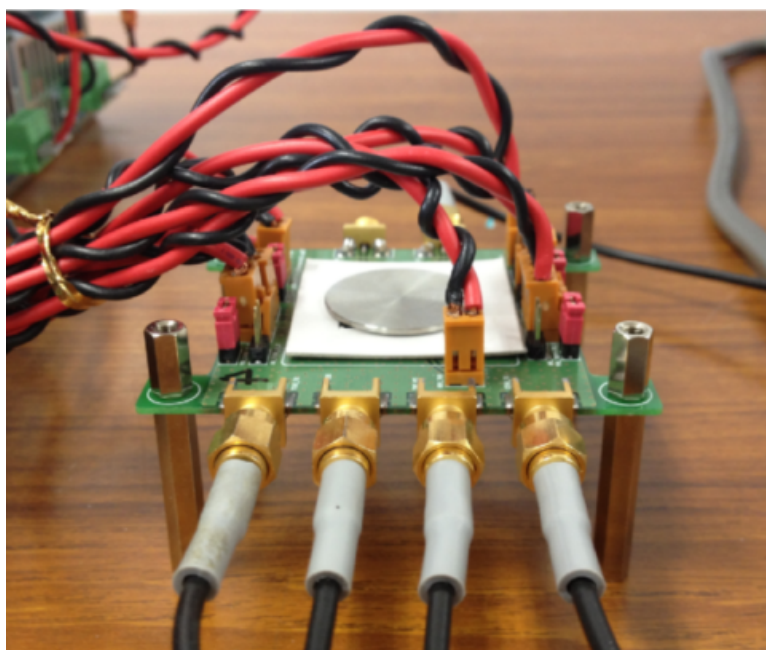


Figure 4.15: Set up for radiation test with alpha-particle source

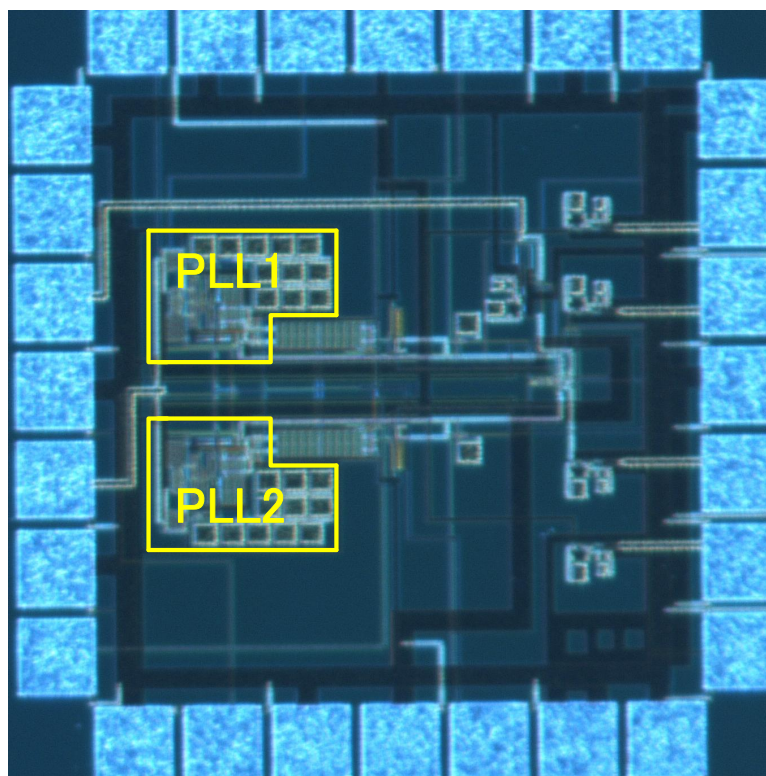


Figure 4.16: Microphotograph of PLLs designed with $0.18\ \mu\text{m}$ CMOS process. (©2013 IEEE)

results from the evaluation but the critical charge of the analog sub-circuits ($Q_{\text{crit,VCO}}$ and $Q_{\text{crit,CP}}$) was much higher. The critical charge of the analog sub-circuits was around 70 fC in 5% of the cycle-to-cycle jitter specifications. The alpha particles used for this experimental testing are low energy particles, which creates Q_{DEP} lower than about 30 fC. If the results from evaluation were appropriate, the alpha-particles would only cause gradual perturbation in the digital part. The results from the experiment indicated only gradual perturbation occurred in practice. Thus, our experimental results were consistent with those from the evaluation. Furthermore, it was confirmed the simulated behavior of gradual perturbation on actual silicon. Figure 4.17 is one example of gradual perturbation captured from an oscilloscope. The clock waveforms in Figure 4.17 illustrate the outputs of the two PLLs with the same reference clock. The first and second waveforms (PLL1 and PLL2) illustrate a perturbed clock by a radiation-strike and a normal clock at the outputs of the two PLLs (PLL1 and PLL2). The third and the fourth waveforms are the locking detector's outputs of PLL1 and PLL2. The locking detector checks whether the PLL is locked or not in every rising edge of the reference clock, as illustrated in Figure 4.18 [49]. If the PLL loses its locking condition, the locking detector's output signal (locking signal) changes from HIGH to LOW. The locking signal of PLL1 (the third waveform) in Figure 4.17 changes from HIGH to LOW, but that of PLL2 remains HIGH. This means PLL1 has lost its locking condition due to a radiation strike. The clock perturbation of PLL1 (the first waveform) was actually observed. The experimental results in Figure 4.17, especially, indicate a radiation strike at the PFD. If a radiation strike occurs at the divider, the locking signal and clock perturbation should almost simultaneously be emitted because both the incorrect pulse, which causes clock perturbation, and the locking signal are synchronized with the rising edge of the reference clock. The incorrect pulse caused by the radiation strike at the PFD, on the other hand, appears regardless of the rising edge moment. The clock perturbation due to the incorrect pulse is first propagated, and then the locking pulse is emitted at the rising edge of the reference clock. Thus, the clock perturbation in Figure 4.17 is attributed to the radiation strike at the PFD.

It was found through the evaluation and validation that critical part in the demonstrated PLL design was in digital sub-circuits. Digital sub-circuits in the partial-hardening technique should be preemptively protected rather than other sub-circuits. Use of TMR-based design or radiation-hardened D-FF is a good choice to protect digital sub-circuits. If use of these techniques can protect digital sub-circuits, the critical charge of PLLs ($Q_{\text{crit,PLL}}$) would increase from a $Q_{\text{crit,PFD}}$ and $Q_{\text{crit,div}}$ of 10 fC to a $Q_{\text{crit,CP}}$

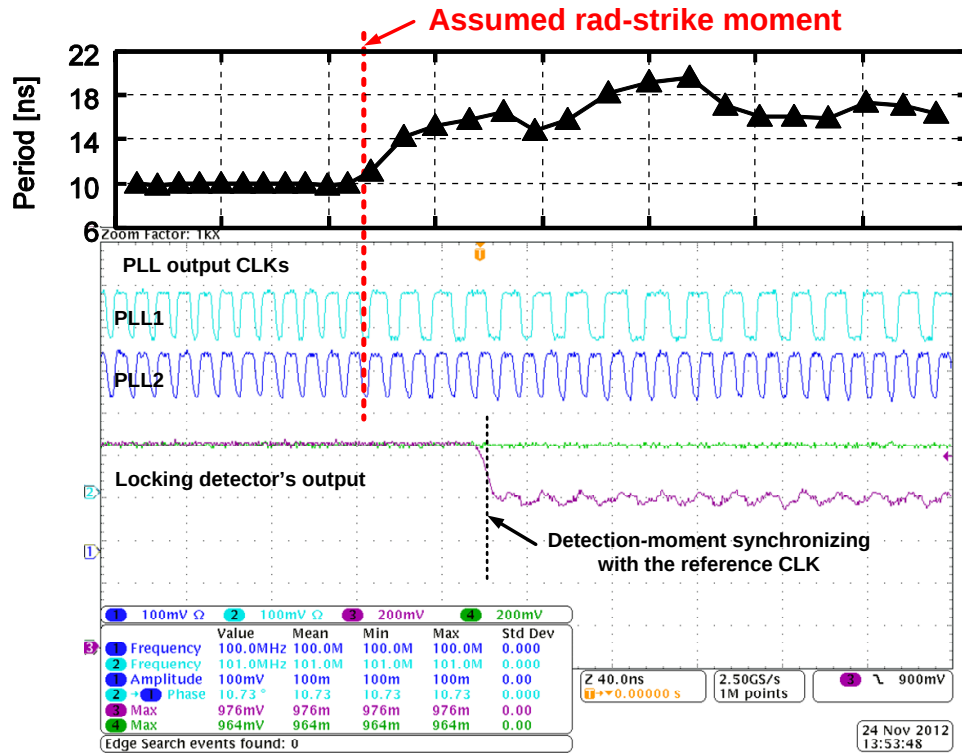


Figure 4.17: Experimental results from alpha-particle test on PLL. Simulated behavior of gradual perturbation was actually observed on a real silicon

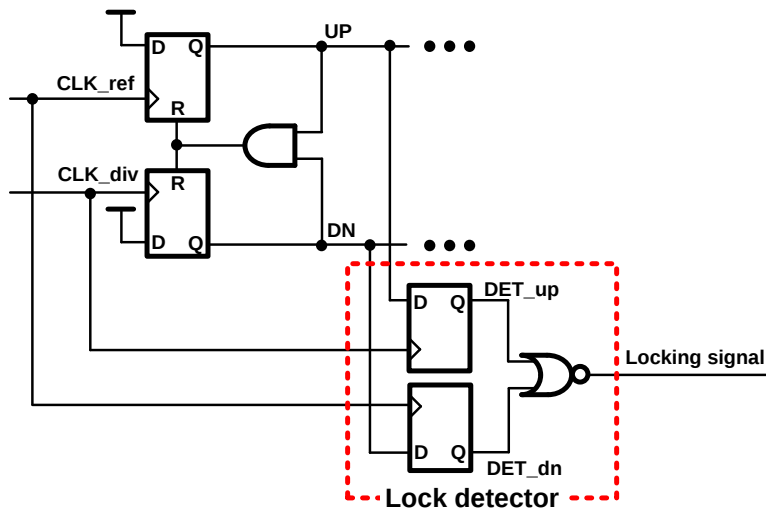


Figure 4.18: Lock-detection circuit to detect radiation strikes on PLLs.

and $Q_{\text{crit,VCO}}$ of 70 fC.

4.6 Summary

This chapter discussed modeling of PLL's recovery behavior from radiation-induced perturbation. The PLL's recovery behavior from the radiation-induced perturbation was quantified as recovery time. To evaluate the recovery time, behavioral models of radiation-induced errors, which were categorized in Chapter 2, were presented. The error behavioral models were embedded into the sub-circuit behavioral models that composing the PLL behavioral model. The error behavioral models are activated by setting input parameters and the PLL behavioral model is simulated under a radiation condition. For the analog sub-circuits, the inputs of the error behavioral models are the phase displacement for the VCO and the injection current for the CP. To activate the error behavioral model for the digital circuits, the locations and the timings of radiation strike are required. The inputs and outputs of the error behavioral models are summarized in Table 4.1. The behavioral models of the radiation-induced errors and the PLL were implemented with Verilog-A. The transient characteristics of the control voltage from the behavioral model were compared to that from the transistor-based model to verify the behavioral model. The result from the behavioral model had a good agreement with that from the transistor-based model. The recovery time has 80 ns of the maximum different between the results from the behavioral model and those from the transistor-based model. This discrepancy is reasonable because the recovery time is usually several hundreds nano-seconds. Furthermore, the behavioral model achieved to improve simulation speed that was about 200 times faster than that of transistor-level simulation in CPU time.

The evaluation of a conventional PLL's vulnerability to radiation was demonstrated with the behavioral model and the analytical model. It was found through the evaluation that digital sub-circuits are more vulnerable than analog sub-circuits. The radiation strike at the PFD revealed the largest phase displacement and the longest recovery time. The errors at the digital sub-circuits causes the violation of 5% cycle-to-cycle jitter if a charge of 10 fC is injected. However, the analog sub-circuits need 70 fC of the injection charge to violate the jitter specifications. To validate this evaluation results, the experimental testing of radiation has been performed with an alpha-particle source. The results from the experiment indicated only gradual perturbation occurred in the alpha-particle testing. This means the alpha-particle, which generates Q_{DEP} lower than about 30 fC, has caused the error only at the digital sub-circuits. Thus, the evaluation result is confirmed from the experiment.

Chapter 5

High-Reliability RH-PLL Design

5.1 Introduction

This chapter proposes radiation-hardened PLL (RH-PLL) with a switchable dual modular redundancy (DMR) structure that is immune to clock perturbation. The basic concept of the proposed RH-PLL is ‘detecting’ clock perturbations and ‘switching’ to a non-perturbed clock instead of ‘recovering’ from clock-perturbations. If one of dual PLLs has a clock perturbation due to a radiation strike, detectors detect the clock perturbation and switch the RHPLL’s output from the perturbed PLL to unaffected PLL shown in Figure 5.1. In RH-PLL design, the basic premise is the time interval between radiation-induced errors is large enough to recover from the preceding error. This premise ensures that one PLL of the dual PLL always generates the normal clock without any perturbation. Actually, the radiation-induced rate of flipflops (FFs) was known as 0.001 FIT/FF at sea level. Failure in Time (FIT) is equivalent to one error per a billion hours of a device operation. This means one error occurs at a FF in a 10^{12} hours. PLLs include several FFs in the PFD and the Divider. Assuming that a PLL includes 10 FFs, one error occurs at the PLL in 10^{11} hours. If we consider applications used in more serious radiation environment, the time interval is still large enough. The radiation flux strongly depends on altitude – the neutron flux at airplane altitude is 360 times higher than at sea level [2]. One error arises in around 10^8 hours at airplane altitude. Although the time interval decrease in the space, the time interval would between errors is large enough to recover because the recovery time of PLLs is around several hundreds nanosecond.

The main issue in this strategy to accomplish robust immunity to clock perturbation is the speed

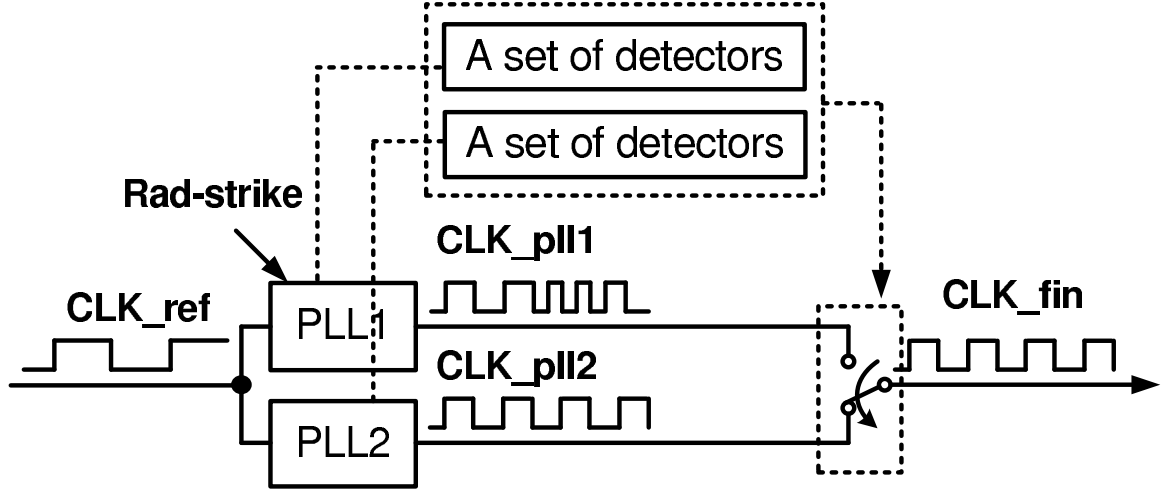


Figure 5.1: Basic concept of proposed RHPLL based on dual modular redundancy (DMR) with detectors. (©2013 IEEE)

of detection. Not all clock perturbations appear immediately after radiation strikes occur in a PLL. Although a radiation strike in analog sub-circuits causes an ‘instant clock perturbation’, a radiation-strike in digital sub-circuits causes a data-flip, which then results in a ‘gradual clock perturbation’. This is because error, which means the data-flip, goes through the LF’s large time constant and then reaches PLL output. Since both types of perturbations have their own characteristics, the detection methods for each type need to be carefully selected. Therefore, the proposed RH-PLL consists of dual PLL and two sets of detectors to detect instant and gradual perturbation. The main contribution of our proposal is to accomplish robust immunity against clock perturbations with high speed detection. Additionally, this strategy does not require any compromises regarding PLL performance such as jitter because high-performance unhardened PLL can be used as its core circuit without the use of radiation-hardened sub-circuits that may have sub-optimal performances. Also, the silicon area overhead is less than that of TMR-based PLLs.

5.2 Proposed Switchable Dual Modular Redundancy Structure

The most important issue to achieve robust RH-PLL that is immune to perturbation is the speed at which clock perturbations are detected. Clock perturbations must specifically be detected immediately after they occur. It is therefore necessary to investigate clock perturbations due to radiation strikes to achieve this. Two types of clock perturbations were identified in analog and digital sub-circuits in

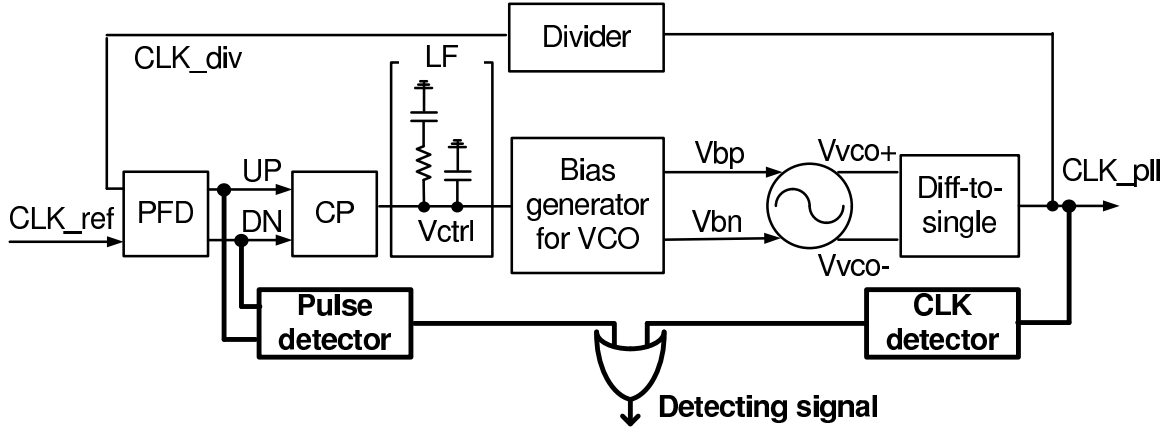


Figure 5.2: Overall strategy in proposed methods of detection. (©2013 IEEE)

Section 2.4. Both clock-perturbation types are difficult to detect by a single circuit. The detector for detecting gradual clock perturbation should be capable of detecting slight clock perturbations because clocks are gradually perturbed after a radiation strike. Clock perturbation should be detected as soon as possible to detect instant perturbation because the perturbed clock is instantly emitted to the output of a PLL. Therefore, different detection methods are necessary for both types of clock perturbations.

The proposed RH-PLL is composed of dual PLLs and two sets of detectors, as shown in Figure 5.1. A conventional low-jitter PLL is selected for the design of the dual PLLs [33] in this research. There is a set of two detectors that consist of a clock and pulse detector in Figure 5.2. The clock detector is used to detect instant perturbation and the pulse detector is used to detect gradual clock perturbation. Since these detectors play key roles in the proposed RH-PLL, the details on each of these will be described in the sections that follow.

5.2.1 Clock Detector with Temporal Redundancy

A clock detector with temporal redundancy placed at the output of a PLL is proposed to detect instant clock perturbation. The key idea behind instantly detecting clock perturbation is to compare the clocks before and after radiation strikes occur. The constant period of the PLL clock changes after a radiation strike, as shown in Figure 5.3 (a). Hence, if the clock before the radiation strike (past clock) and that after the radiation strike (present clock) differ, the PLL has suffered clock perturbation. If the past and present clocks are identical, the PLL is operating normally, on the other hand. Then, the past and present clocks are compared using an exclusive OR (XOR-) gate to determine whether they are

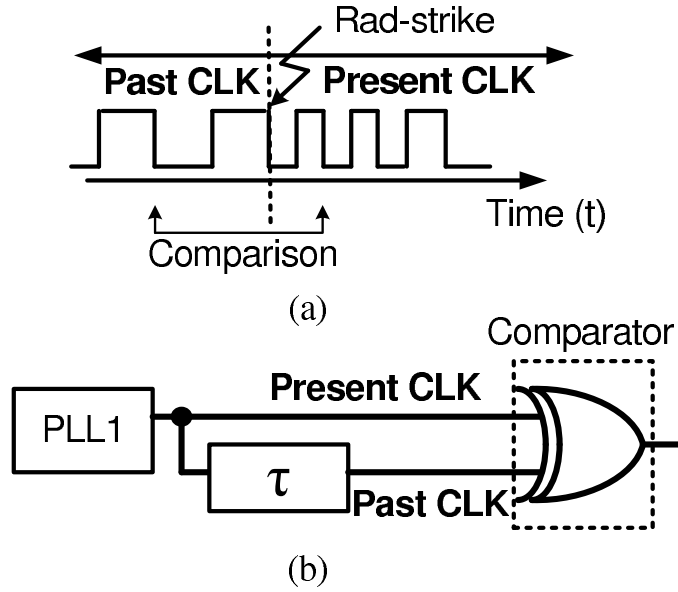


Figure 5.3: (a) Basic concept of proposed clock detector using temporal redundancy. (b) Implementation of temporal redundancy. (©2013 IEEE)

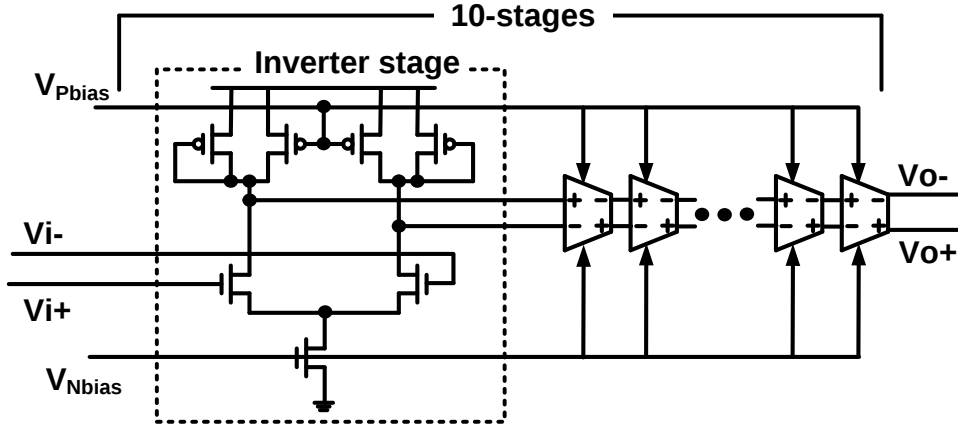


Figure 5.4: Implemented delay-line circuit.

identical or not, as seen in Figure 5.3 (b).

A delay line that generate a delayed clock by one period is used in this research to generate a past clock. The delay line is realized as an identical differential inverter used in the VCO. The topology of the differential inverter is basically a current-starved inverter with symmetric loads [33]. Since the VCO consists of a five-stage inverter, the delay line is implemented with a ten-stage inverter to attain a clock delayed by one period, as seen in Figure 5.4.

Figure 5.5 illustrates the waveforms when a radiation strike occurs on the dual PLL. While the past

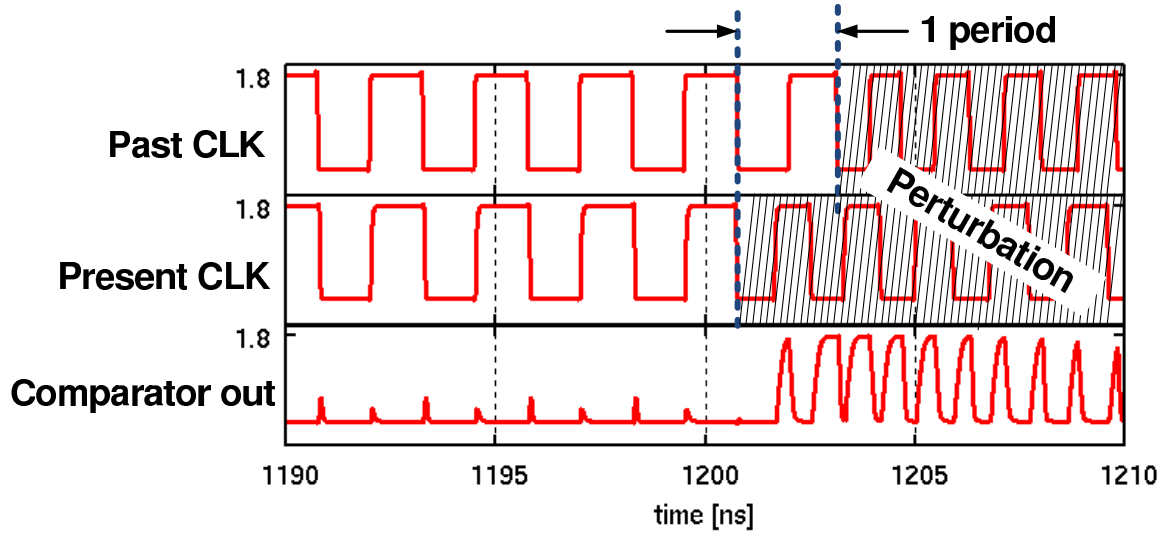


Figure 5.5: Simulation results: ‘Past CLK’ has one period of delayed waveform compared to ‘Present CLK’. Comparator (XOR gate) generates pulses due to clock perturbation. (©2013 IEEE)

clock emits a perturbed clock after one period of a radiation strike, the present clock immediately emits a perturbed clock after the radiation strike has occurred. The difference between the past and present clocks produces a detection signal at the output of the XOR gate. The RH-PLL’s output is switched based on this signal.

5.2.2 Pulse Detector based on SE-Failure Model

A pulse detector based on the radiation effect analysis is proposed to detect clock perturbations, as discussed in Chapter 2. Each clock cycle in gradual perturbation gradually differs cycle by cycle by very small amounts as discussed in Chapter 2. Since the clock detector compares the present to the past clock delayed by one period, it is difficult for it to quickly detect that small difference between these two clocks. Thus, this approach is used to detect a data flip at the PFD’s output rather than detecting clock-perturbation.

While the reference clock and the divider’s output-clock, which is divided by 2^5 , are identical, the PFD creates a locking signal that has a low voltage level for UP and DN signals, as shown in Figure 5.6. The PLL’s output emits constant clocks in the locking state. A radiation-strike in the digital part, however, leads to an incorrect pulse at the PFD’s output even though the PLL’s output emits constant clocks. The pulse detector in this approach detects the incorrect pulse at the PFD’s output.

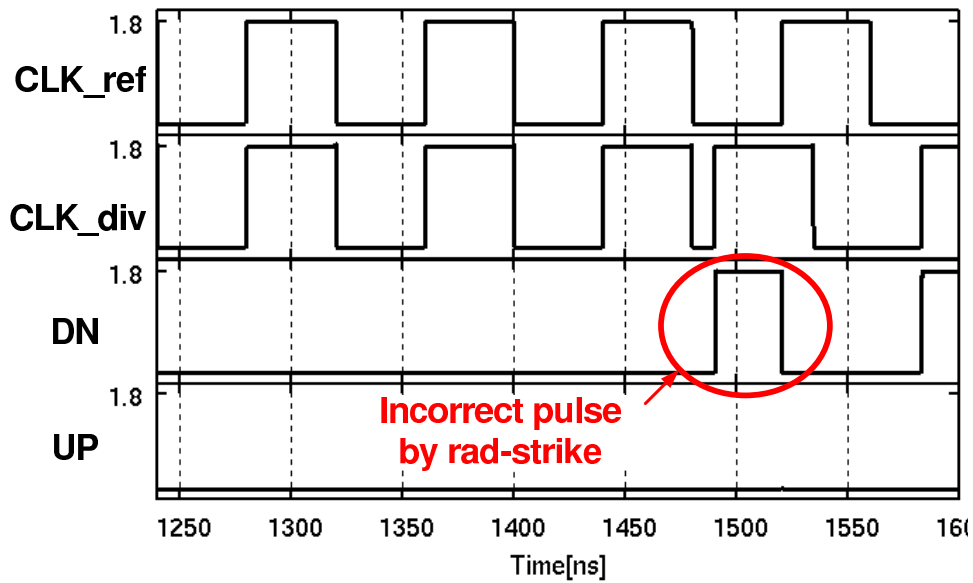


Figure 5.6: Example of incorrect pulse caused by radiation strike at divider. CLK_ref is reference clock and CLK_div is 2^5 -divider's output clock. (©2013 IEEE)

A lock-detection circuit is one option for detecting incorrect pulses and was actually used, as was discussed in Section 4.5. Although the lock-detection circuit is an adequate choice for determining whether PLL is locked or not, it is not a proper choice for generating a switching signal. Since the detection is performed at the rising edge of the reference clock, its detection signal is emitted after several cycles of clock perturbation. This means that the lock-detection circuit may allow a perturbed clock to appear at the RH-PLL's output.

Figure 5.7 shows an implementation of the pulse detector for immediate detection. An OR gate combines both UP and DN signals when an incorrect pulse appears on an UP or DN signal according to a radiation strike in digital sub-circuits. Figure 5.8 compares the detection capabilities of the pulse detector and clock detector when a radiation strike occurs at the PFD in PLL2. Since the difference in the clock cycle between the present clock (CLK_pll2) and the clock delayed by one period is small, the pulse detector generates the detecting signal faster than the clock detector. Thus, the pulse detector is more efficient for detecting gradual perturbations.

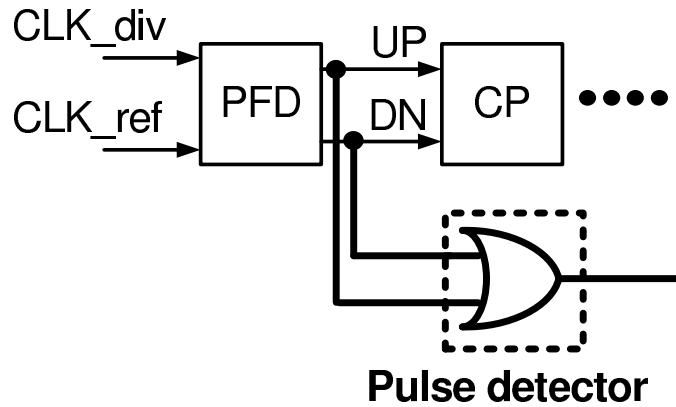


Figure 5.7: Proposed pulse detector for detecting ‘incorrect pulse’ caused in digital part of PLL. (©2013 IEEE)

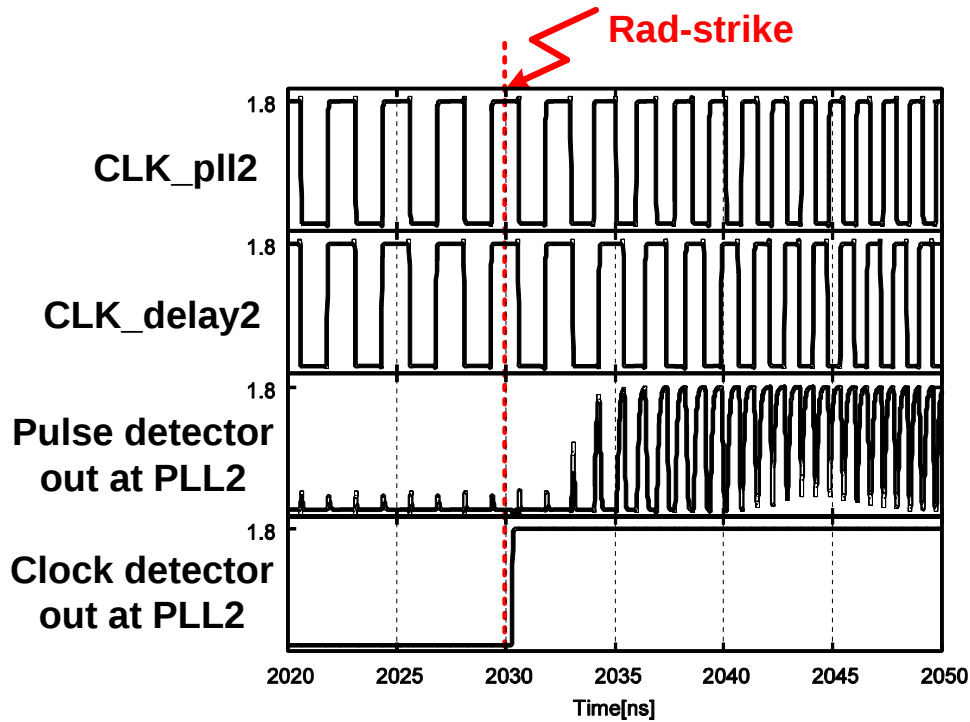


Figure 5.8: Comparison of detection capabilities of pulse and clock detectors.

5.2.3 Full Structure of Proposed RH-PLL

Figure 5.9 is a circuit diagram of the full structure of the proposed RH-PLL, including the switching part. The detecting signals of the pulse and clock detectors are combined via an OR gate. Two detecting signals of the dual PLLs comprise a switching signal via a set-reset(SR) latch. Then, a 2X1 multiplexer (MUX) switches the RH-PLL’s output according to the SR latch’s output signal.

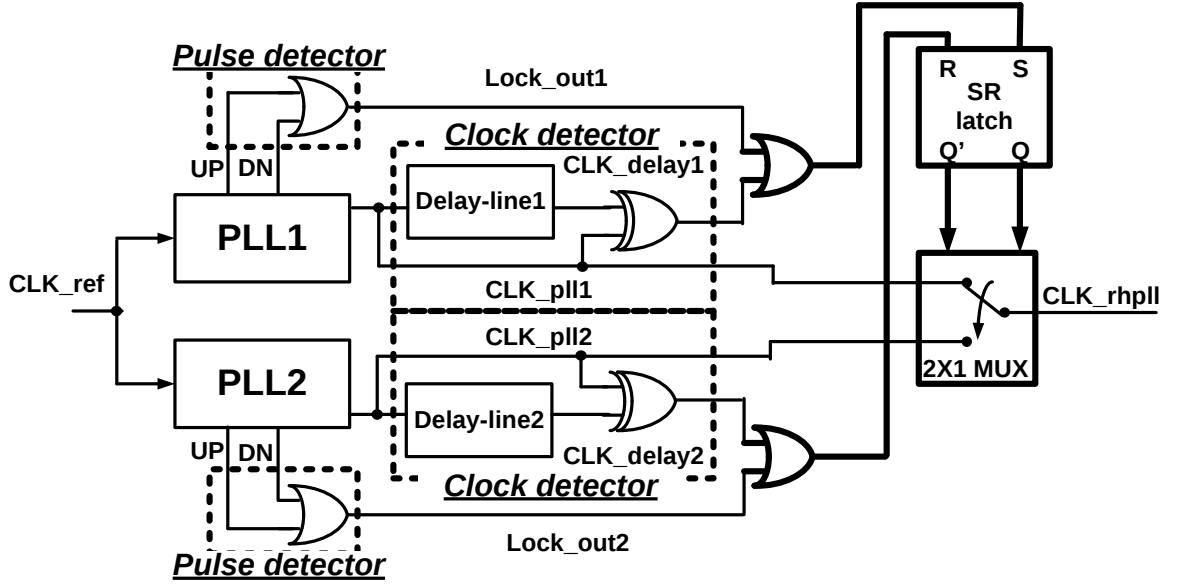


Figure 5.9: Full structure of proposed RH-PLL. (©2013 IEEE)

5.3 Simulation Results

Radiation-immunity for both type of clock perturbation is demonstrated based on transistor-level simulation with SPICE.. The proposed RH-PLL for the simulation was designed with a 0.18- μm CMOS process. Figure 5.10 shows a case of instant clock perturbation and how it is corrected in the proposed RH-PLL. Figure 5.10 (a) illustrates the instant perturbation at one side of the PLL. The charge of 500 fC is injected into a CP output node (V_{ctrl}) to emulate the instant perturbation and the charge injection is an nMOSFET-hit. Instant perturbation is detected with the clock detector at the PLL's output. The switching signal is created based on the signal coming from the clock detector, as seen in Figure 5.10 (c). The switching signal changes the clock path from the perturbed PLL to the other PLL of the dual PLLs. Consequently, the RH-PLL's output has normal clocks without any perturbation, as can be seen from Figure 5.10 (b).

The overall operation of the RH-PLL with gradual clock perturbation is similar to instant clock perturbation, except for the method of detection. Figure 5.11 depicts the gradual clock perturbation and how it is corrected in the proposed RH-PLL. The gradual perturbation arises due to an SEU at the UP latch that is attributed to a charge injection of 50 fC. The pulse detector detected the incorrect pulse, which induces the gradual perturbation, at the PFD's output and then emits a detecting signal into the switch via the OR gate and the SR latch. The RH-PLL's output path is switched by the switching

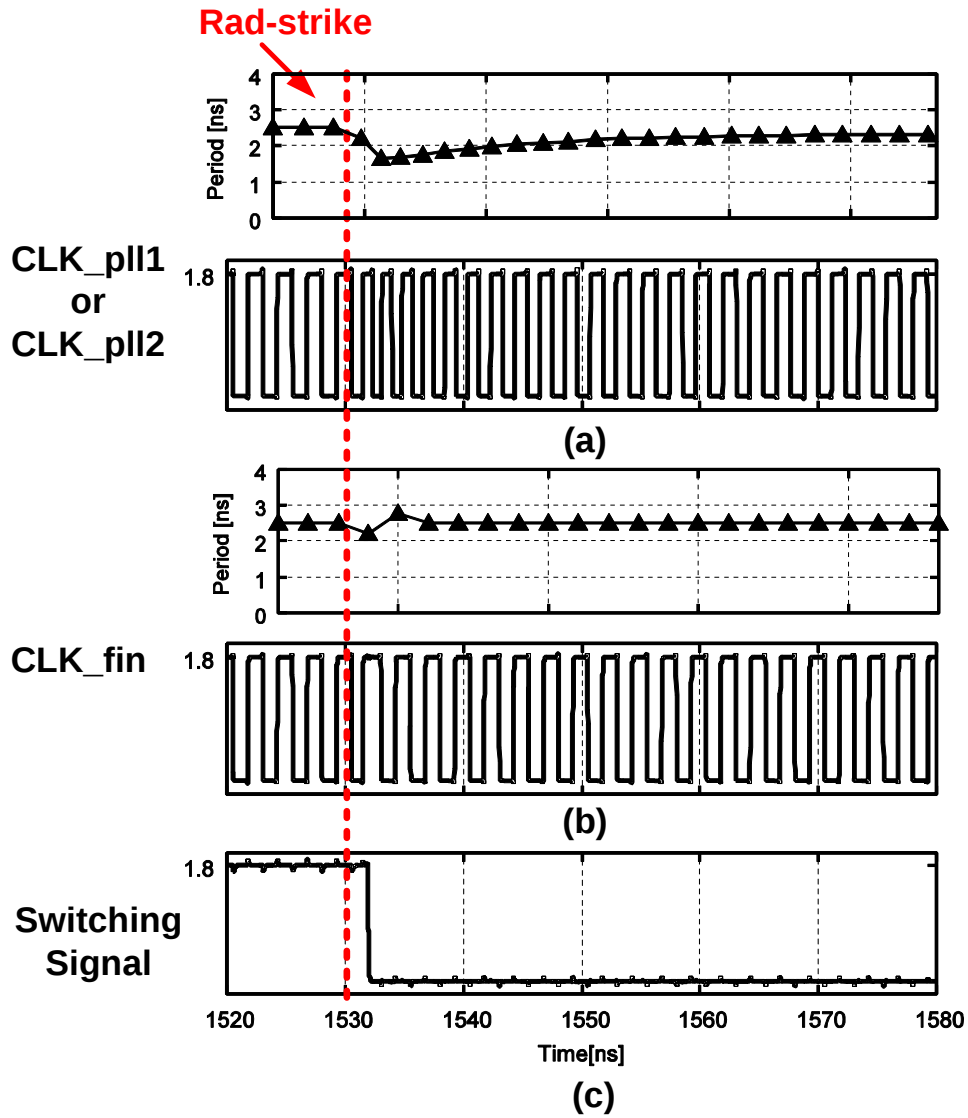


Figure 5.10: Waveforms when instant clock perturbation occurs. (a) One PLL's output in dual PLLs with perturbation. (b) Clocks at output of proposed RH-PLL. (c) Switching signal to change clock path from perturbed clock to non-perturbed clock.

signal generated from the perturbed PLL to the other PLL of the dual PLLs, as shown in Fig. 5.11. This simulation result also indicates perturbation-free clocks at the RH-PLL's output.

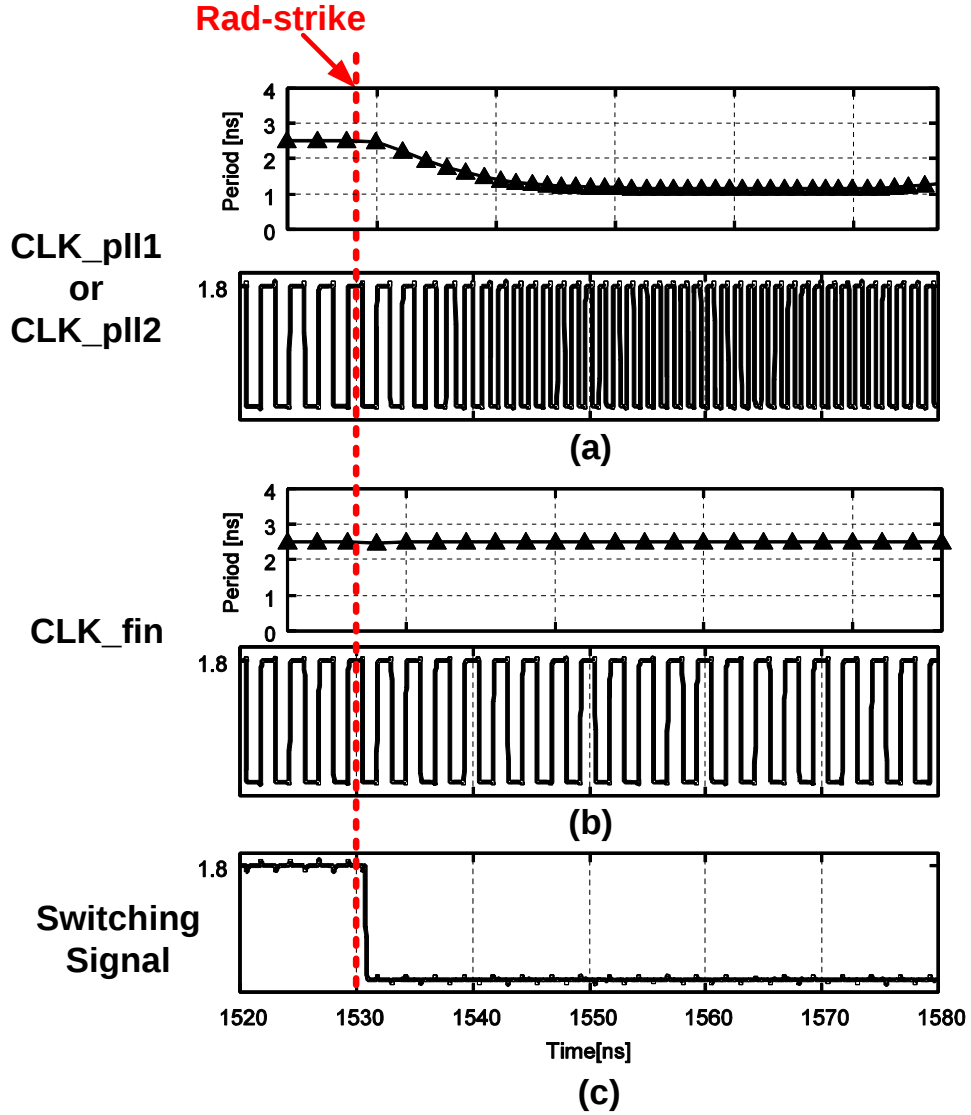


Figure 5.11: Waveforms when gradual clock perturbation occurs. (a) One PLL's output of dual PLLs with perturbation. (b) Clocks at final output of proposed RH-PLL. (c) Switching signal for changing clock path from perturbed clock to non-perturbed clock.

5.4 Experimental Results

The proposed RH-PLL was fabricated with a 0.18- μm CMOS process, as shown in Fig. 5.12. The radiation test for the fabricated RH-PLL was performed using an alpha-particle source (3 MBq ^{241}Am) for 1.2 V of supply voltage. A small-swing radio frequency (RF) output buffer was embedded to enable the PLL output's clock to be directly observed. The buffer monitors the high-speed clock in a range of hundreds of megahertz. The buffer attained impedance matching with a 50-ohm transmission line on a

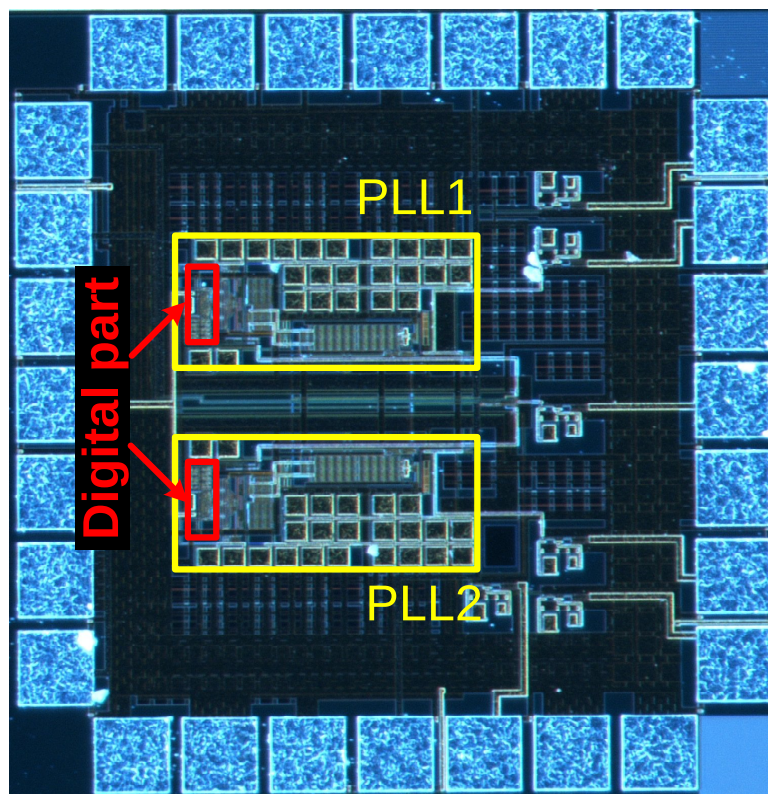


Figure 5.12: Micrograph of proposed RH-PLL.

test board.

An alpha-particle source that emits low-energy radiation particles was used in this experiment. Alpha-particles hit randomly transistors in RH-PLL. The effects of radiation strikes only appears in the PLL design when particles hit the digital part because low-energy particles, such as alpha particles, do not create sufficient amounts of charges to result in errors at the analog part. The size of the transistors for the analog circuits was determined to be about three times the minimum channel length in the technology process.

Figure 5.13 presents the results from a radiation test when the PLL1's clock is perturbed by a radiation strike. There are four signals - that of the PLL1 pulse detector, that of RH-PLL output (CLK_rhpll), that of PLL1 output (CLK_pll1), and that of the switching signals. The pulse detector of PLL1 emits an incorrect pulse as the result of a radiation strike. Gradual perturbation was observed at PLL1 output (CLK_pll1) from the onset of the incorrect pulse. However, RH-PLL output (CLK_rhpll) maintains a constant clock cycle. The initial switching signal is at the LOW level, which means that the RH-PLL output (CLK_rhpll) was connected to PLL2 output (CLK_pll2). Since the radiation strike

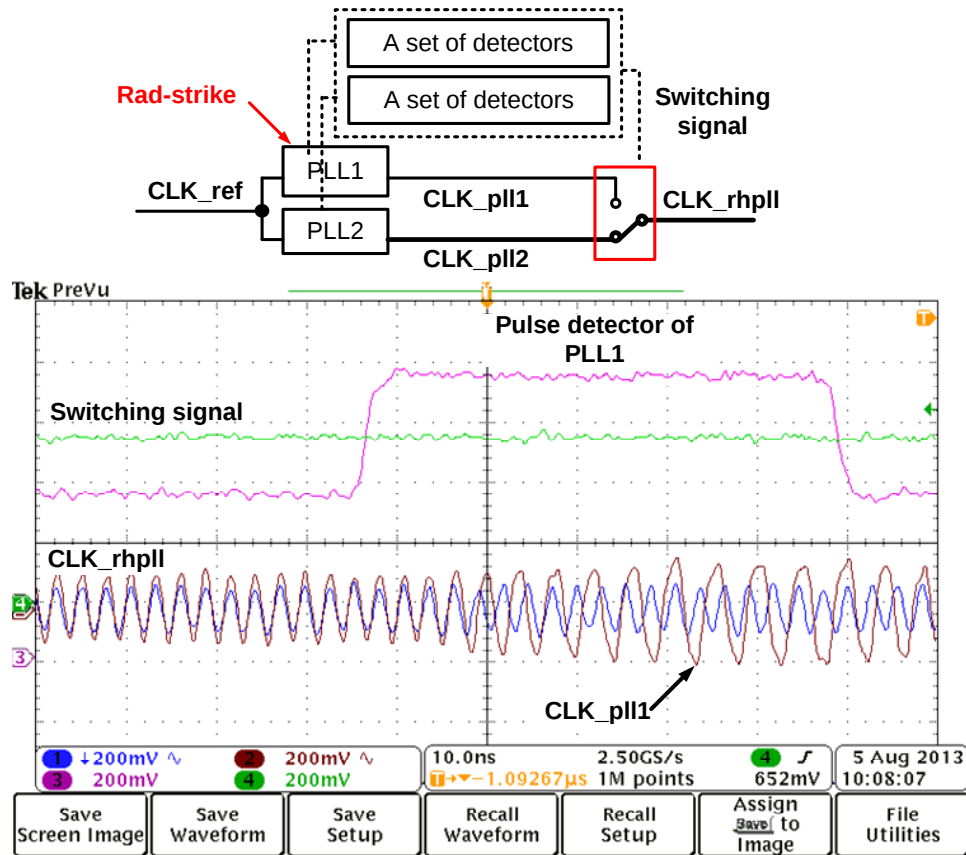


Figure 5.13: Results from radiation test when radiation strike occurred at PLL1 of fabricated RH-PLL.

occurred at PLL1, there was no change in the switching signal.

Figure 5.14 depicts the results from a radiation test when the PLL2's clock is perturbed by a radiation strike. When the RH-PLL output is switched from PLL2 to PLL1, four output signals, which are that of PLL1, that of PLL2, that of RH-PLL, and the switching signal, were simultaneously captured on a four channel oscilloscope. It is necessary to compare the RH-PLL clock with each PLL clock to find a PLL that is perturbed. The PLL1 and PLL2 clocks are separated as seen in Figure 5.14 (a) and Figure 5.14 (b). Figure 5.14 (a) displays PLL2 and RH-PLL whereas Figure 5.14 (b) shows PLL and RH-PLL. Only difference is whether it includes PLL1 output or PLL2 output. The switching signal in this case has changed from LOW to HIGH level due to the radiation strike. The clock waveform of PLL2 is perturbed in Figure 5.14 (a) from that of the RH-PLL's clock. The RH-PLL's clock maintains a constant cycle because RH-PLL output drives PLL1's clock by switching to HIGH. Figure 5.14 (b) indicates that RH-PLL's clock is identical to PLL1's clock. This experiment confirmed the proposed RH-PLL is immune to clock perturbation. Table 5.1 shows measurement summary of the RH-PLL

Table 5.1: Measured summary of RH-PLL performance.

Process Technology	0.18 μm CMOS
Supply Voltage	1.2 V ($V_{\text{DD,digital}}$), 1.8 V ($V_{\text{DD,analog}}$)
Total Occupied Area	0.48 x 0.53 mm ²
Frequency range	30 – 520 MHz
Current Dissipation	19.9 mA @ 360 MHz
Cycle-to-cycle jitter	25 ps (rms)

performance. Figure 5.15 illustrates the jitter histogram plotted with measurement data.

5.5 Summary

An RH-PLL with a switchable DMR structure was proposed. The basic concept underlying the proposed RH-PLL is to detect clock perturbation and switch RH-PLL's output instead of waiting for recovery. The key design feature is a set of detectors - a clock and a pulse detector to eliminate clock perturbations. The detectors enable clock perturbation to be immediately detected after a radiation strike occurred. The proposed RH-PLL was fabricated with a 0.18- μm CMOS process. Clock perturbation that is induced by radiation at PLL output and the detecting signal at the pulse detector's output were observed in a radiation test. The fabricated RH-PLL demonstrated a clock that is immune to perturbation at its output due to switching.

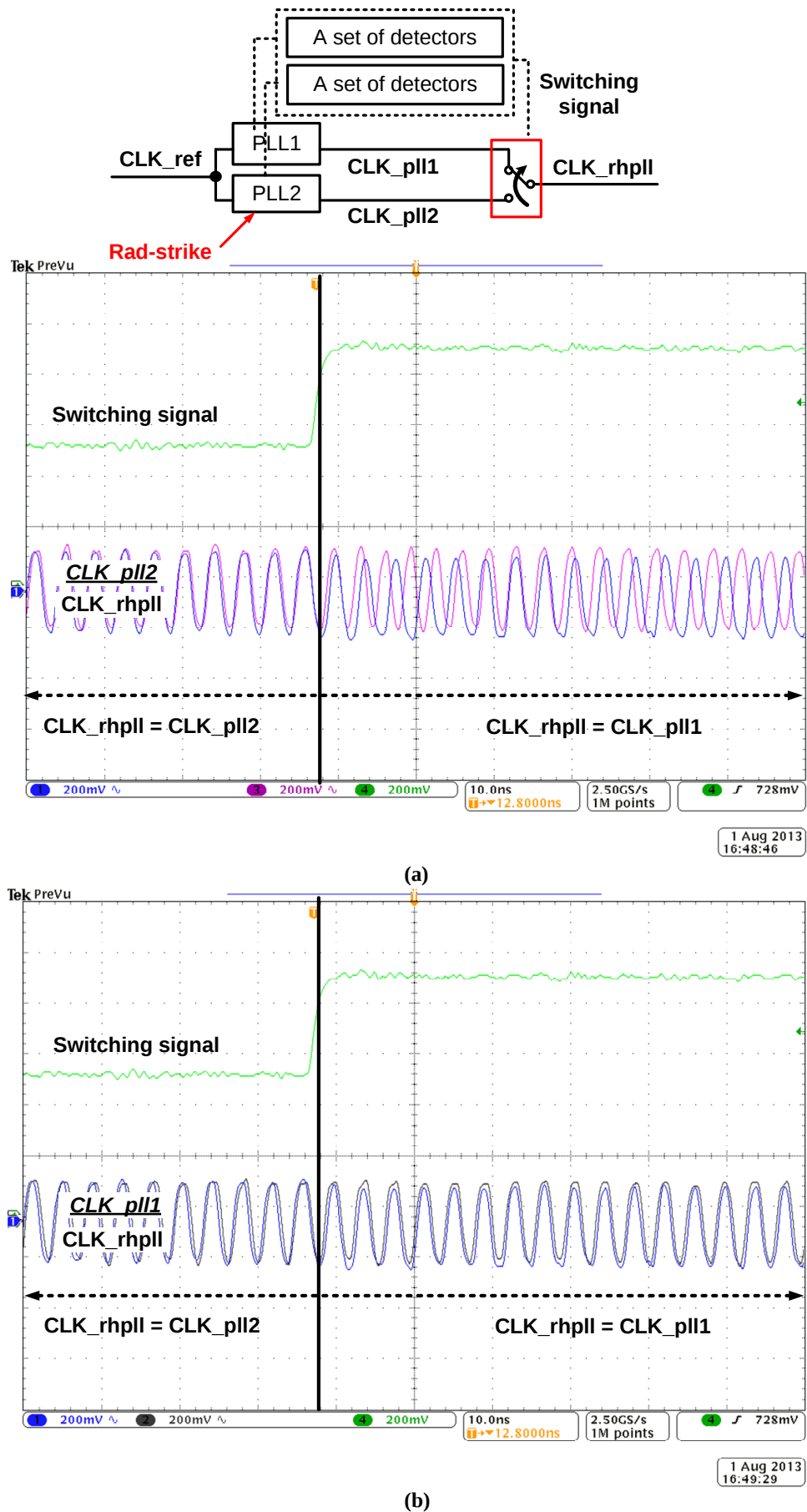


Figure 5.14: Results from radiation test when radiation strike occurred at PLL2 of fabricated RH-PLL.

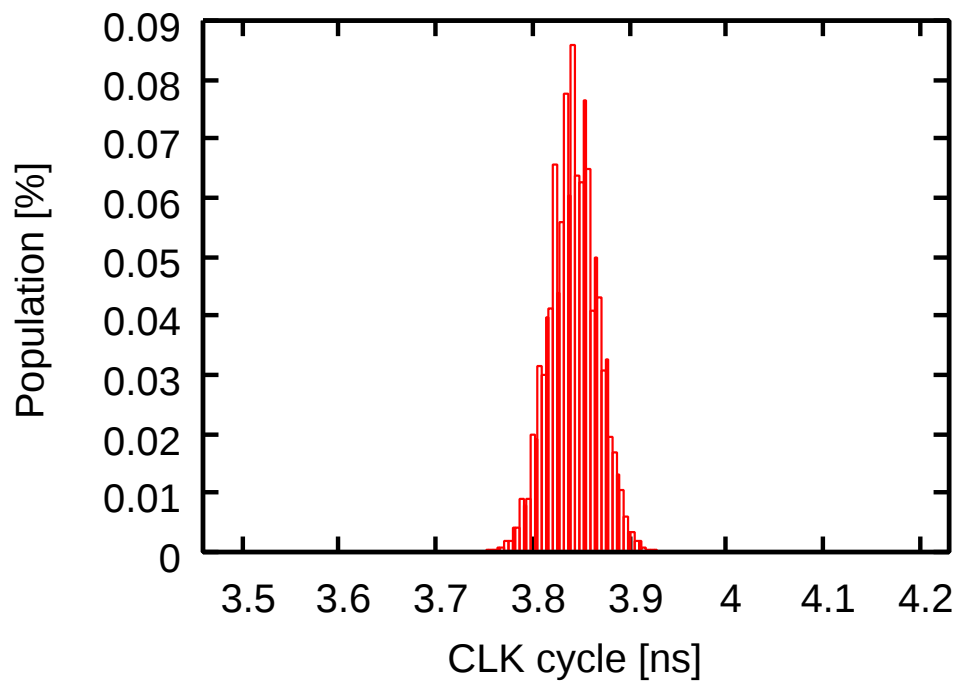


Figure 5.15: Jitter histogram plotted with measurement data.

Chapter 6

Conclusion

Phase-locked loop (PLL) is a clock generator. A radiation strike of high-energy particles on PLL causes clock perturbation. The perturbed clock is propagated to all over the digital system, which is attributed to a malfunction in the system. Thus, the performance related to radiation effect of the PLL is important to ensure the reliability of various applications which are used in the space environment such as satellite system and in earth's surface environment such as super computer. In this dissertation, an analysis of radiation effect on PLL and a radiation-hardened PLL (RH-PLL) design to guarantee clock-perturbation immunity are presented.

First of all, an analysis of radiation effect on PLL was discussed. In this analysis, all possibilities, which are related to locations and timings of radiation strikes, were examined. As a result, radiation-induced errors were categorized for each sub-circuits: Voltage-Controlled Oscillator (VCO), Charge Pump (CP), Phase Frequency Detector (PFD), and Divider. Furthermore, how the categorized errors propagate to PLL output was identified. The radiation-induced errors eventually lead to clock perturbations at PLL output. Since the errors occurring at sub-circuits have different propagation mechanisms, the clock perturbations also have different types. The clock perturbations were divided into two types, which are the gradual perturbation and the instant perturbation. The gradual perturbation and the instant perturbation are originated from errors occurring at the digital sub-circuits and the analog sub-circuits, respectively.

Second, an analytical modeling of clock phase displacement under radiation was discussed. The analytical model provides the phase displacement as its output. The input parameters to obtain the phase displacement are the deposition charge, the locations and timings of radiation strike. The analyt-

ical model consists of four sets of model equations because it was modeled based on the categorization results presented in Chapter 2. In modeling, the categorized errors were firstly quantified. Then the model equations of the phase displacement were formulated from the quantified errors. The analytical model was verified through comparison with SPICE simulation results. For this, a conventional low-jitter PLL operated in 400 MHz (2.5 ns period) was designed in a 0.18 μm process. Phase displacement values computed using the analytical model have good agreement with the SPICE simulation results. The discrepancy is less than 0.56 radian in the phase displacement and 220 ps in clock period.

Third, the behavioral modeling to evaluate the clock recovery time under radiation was discussed. The modeling presents the behavioral models of radiation-induced errors categorized in Chapter 2. The behavioral error-models were embedded into the behavioral model of each sub-circuit composing the PLL behavioral model. The behavioral error-models are activated by entering input parameters and then generate the radiation-induced errors at sub-circuit outputs. The PLL behavioral model produces clock perturbations and shows its recovery behavior at its output. The input parameters of the behavioral error-models are the deposition charge, the locations and timings of radiation strike, which are the same with the analytical model. The behavioral models were implemented with Verilog-A. To verify the behavioral model, the results from the behavioral model were compared to that by the SPICE simulation. The transient characteristics on the control voltage obtained from the Verilog-A simulation were in good agreement with those from the SPICE simulation. As a result of recovery time evaluation, the discrepancy between the result from the SPICE simulation and that from the Verilog-A simulation is less than about 80 ns. This discrepancy is reasonable considering that the recovery time is several hundreds nanosecond. Furthermore, the behavioral model achieved to improve simulation speed that was about 200 times faster than that of transistor-level simulation in CPU time. The evaluation of the conventional PLL's vulnerability to radiation was demonstrated with the behavioral model. It was found through the evaluation that digital sub-circuits are more vulnerable than analog sub-circuits. The digital sub-circuits in the conventional PLL causes the violation of 5% cycle-to-cycle jitter if a charge of 10 fC is injected but the analog sub-circuits need 70 fC to violate the jitter specifications. This identification was validated through the experimental testing of radiation with an alpha-particle source. The alpha-particle, which generates Q_{DEP} lower than about 30 fC, can cause the error only at the digital sub-circuits. The results from the experiment indicated only gradual perturbation has occurred.

Fourth, an RH-PLL with a switchable DMR structure was proposed. The basic concept underlying

the proposed RH-PLL is to detect clock perturbation and switch RH-PLL's output instead of waiting for recovery. The key design feature is a set of detectors - a clock and a pulse detector to eliminate clock perturbations. The detectors enable clock perturbation to be immediately detected after a radiation strike occurred. The proposed RH-PLL was fabricated in a 0.18 μm CMOS process. Clock perturbation that is induced by radiation at PLL output and the detecting signal at the pulse detector's output were observed in a radiation test. The fabricated RH-PLL demonstrated a clock that is immune to perturbation at its output due to switching. Additionally, the proposed RH-PLL does not require any compromises on PLL performance such as jitter because a high performance unhardened PLL can be used as its core circuit without the use of radiation-hardened sub-circuits that may have sub-optimal performances. Also, silicon area overhead is less than that of TMR-based PLLs.

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