

Digital-twin-compatible Optimization of Switching Characteristics for SiC MOSFETs using Genetic Algorithm

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Abstract

Active gate drive (AGD) is one of the key techniques to utilize SiC power devices' fast-switching capability without compromising the drawbacks. However, the increasing complexity in the circuit design makes it hard to have an optimized operation without expert know-hows or considerable design efforts. This paper demonstrates a digital-twin-compatible metaheuristic optimization system for a digital AGD. It offers a totally-digital control of switching characteristics of power devices through genetic-algorithm-based optimization. An individually developed digital AGD is adopted to generate a genetically expressed gate-voltage waveform by a multi-bit gate signal sequence. The optimization system is verified in simulation and experiment by successfully obtaining the optimum Pareto-front solutions, which clarify the relationship between the selected gate voltage levels and the device characteristics. The optimization is also performed for variable operating conditions and for different SiC MOSFETs. The results of this paper offer feasibility for a software-based optimization of gate drive design.

Keywords: digital active gate drive, digital-twin, genetic algorithm, I - V curve, combinatorial optimization, SiC MOSFET

I. Introduction

The gate drive circuit is an essential element of a power conversion system. Recent development in the technology of wide-bandgap semiconductor power devices, including SiC MOSFETs and GaN FETs, put a high demand on gate drive circuits to make the most of their fast-switching capability [1, 2]. Active gate drive (AGD) is one of the promising techniques to enhance the application of such power devices [3–6]. The fundamental idea of AGD is to control the slew rate of the power device actively during the switching transient to suppress unwanted overshoots in device voltage/current and resulting EMI, while achieving a fast switching. This can be done either by actively changing the gate resistance [4, 5, 7, 8], applying a variable gate-source

voltage (V_{GS}) [6, 9–14], or limiting/boosting the gate current [15–17]. Initially proposed to drive Si IGBTs [11, 15], AGD has been intensely studied for SiC MOSFETs in recent years, with typically nano-second order control due to the increased switching speed. They have demonstrated superior trade-offs between voltage/current overshoot and switching loss compared to the conventional method, such as the use of large gate resistors and snubber circuits or filters [4, 7]. AGD has also shown promising potential for improved current/voltage balancing between parallel- or series-connected SiC MOSFETs [12, 13]. Practical applications to inverters for PV and EV have also been investigated [7, 8].

Digitized AGDs have been investigated primarily to benefit from digital control using FPGAs or programmable chips [5, 9, 17]. There is another aspect of this technology; they cut into the interface between the digital signal regions and the analog phenomenon of power switching. Analog AGDs commonly optimize their operation through parameter tuning and design improvement, including developing a model for their calculation [4, 6]. They are designed to be significantly effective in a particular condition and for a specific device. However, such an increased complexity in the circuit design requires a considerable design effort with an expert knowledge and experience, which makes it hard to adjust the operation flexibly, especially when the conditions can change. On the contrary, digitized AGDs could be wholly optimized by the signal adjustment using the software [17]. This could fundamentally transform the nature of the approach to designing the gate drive circuit from hardware to software, making it easier to deal with the changes in the operating conditions and device characteristics. Such flexibility might not be necessary for low-cost applications; however, by realizing such a system, it will open up the possibility for the advanced power conversion where the best-effort performance is achieved in the presence of those dynamic uncertainties.

With this concept, the authors have investigated the potential of the digitized AGD and proposed the digital active gate driver (DAGD) [14]. The operation of DAGD is inspired by a digital-to-analog converter (DAC) architecture, which designates a gate-voltage value successively by a multi-bit gate signal sequence. It has been verified that DAGD can control the slew rate of SiC MOSFET and sup-

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press the surge voltage in boost converter application [18].

With DAGD, the gate signal is no longer considered a single-bit signal; rather, it is a string of binary digits that directly represents the desired V_{GS} waveform. Moreover, as every signal adjustment corresponds to a direct selection of gate voltage, the optimum pattern can physically explain the voltage-related characteristics of MOSFET, which plays a critical role in the development of variable-voltage AGDs. In other words, it can force the MOSFET to be in certain gate bias state during the transient, which is not possible in variable-resistor type AGDs. These aspects differentiate this work from other types of pattern-search-based digital AGDs [5, 9, 16, 17].

With digital AGDs, the analog phenomena of power switching can be controlled by means of digital signal adjustment. This suggests that the switching characteristics of power devices can potentially be controlled through a digital-twin system; one can test and optimize the control signal in both the simulation and experiment in exactly the same manner. The genetic algorithm (GA) [19], one of the well-known metaheuristics, is found preferable for optimizing DAGD's operation because of its binary nature. GA has been widely applied to various combinatorial optimization problems in circuit designs [20, 21]. Just like them, we can genetically express the gate signal sequence and optimize it. The authors have already investigated the applicability of GA-based optimization into DAGD in simulation [22]. This paper takes this into the form of digital-twin-compatible system by constructing and verifying an optimization platform interfacing both the SPICE simulation and experimental setup. A recently-published work [23] has also reported the application of GA to the optimization of AGD for GaN FETs. It uses a current-source type AGD with variable driving resistance, and optimization is performed in simulation. In [16], another metaheuristics approach of simulated-annealing is applied to the optimization of current-source digital AGD for Si IGBTs. They require the physical application circuit to optimize the AGD operation. The conceptual difference of our work from these related works is that the optimization platform is oriented toward establishing a digital-twin compatible link, where the performance of an AGD sequence would be evaluated in simulation and then applied to the experiment. This structure will be the key to bring out the systematic advantage of digital AGDs to utilize the preliminarily available data for the computation of the actual AGD sequence eventually. The detailed system configuration and its verification results are presented.

II. Overview of the digital active gate driver

As preparation to the introduction of digital-twin system, this section describes the concept and basic features of DAGD. DAGD converts the gate signal sequence into the desired V_{GS} waveform.

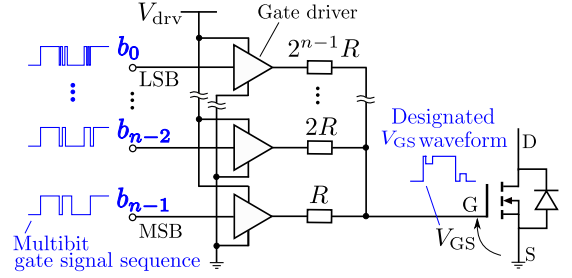


Fig. 1: Configuration of n -bit digital active gate driver.

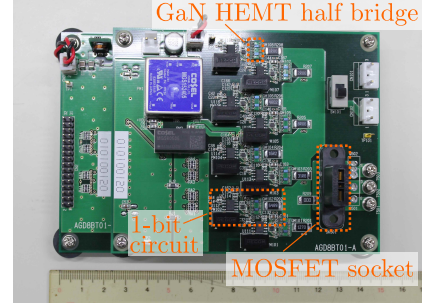


Fig. 2: Photograph of GaN-HEMT-based 8-bit DAGD.

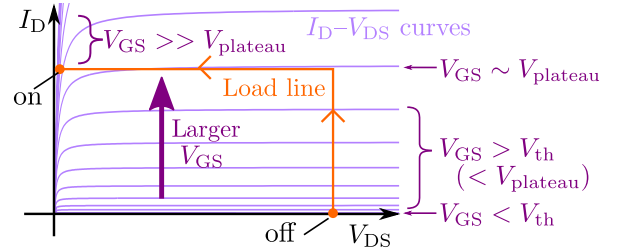


Fig. 3: Example of I_D - V_{DS} (drain current vs. drain-source voltage) curves of MOSFET and load curve.

A. Circuit design and operating principles

Figure 1 shows the schematic diagram of n -bit DAGD [14]. It is designed from the architecture of the binary-weighted resistor DAC [24]. n single gate drivers with gate resistances of $R, 2R, \dots$, and $2^{n-1}R [\Omega]$ are connected in parallel, producing the voltage level at V_{GS} given by (1).

$$V_{GS} = \frac{\sum_{j=0}^{n-1} b_j 2^j}{\sum_{j=0}^{n-1} 2^j} V_{drv} \quad (1)$$

By changing the gate signals successively during the switching transient, the desired V_{GS} waveform is designated.

B. GaN-HEMT-based DAGD

The gate current of DAGD must be large and quick because of its operating principle and the larger gate charge required to drive SiC MOSFETs. Switching frequency of an order of ten MHz will be required for a precise control of gate voltage and the rise/fall time should be as small as possible to realize a fast transition from one V_{GS} level to another. Therefore, GaN HEMT is adopted as the switching device inside the gate driver [25]. Figure 2 shows the prototype of

GaN-HEMT-based DAGD. Eight half-bridge legs of GaN HEMTs (EPC2014C, Efficient Power Conversion), which correspond to the gate drivers in Fig. 1, are integrated with gate resistances of 1, 2, ..., 128 Ω . Its operation can be switched between 4-bit and 8-bit modes; in the 4-bit mode, the four legs with smaller gate resistors are used.

C. Gate driving strategy for voltage-based AGDs

In variable-voltage type AGDs, it is essential to consider the voltage-related characteristics of MOSFETs, such as I_D - V_{DS} curves, gate threshold voltage (V_{th}), and Miller plateau voltage ($V_{plateau}$). The relationship between the V_{GS} level and the state of the MOSFET is discussed on the I_D - V_{DS} plane [26]. Figure 3 shows several I_D - V_{DS} curves of a MOSFET and a load curve for a pure inductive load. As shown in this figure, the transient behavior of the switching trajectory is strongly related to V_{GS} levels, especially V_{th} and $V_{plateau}$.

DAGD directly manipulates its trajectory by means of shaping the V_{GS} waveform. When V_{GS} is set to a certain value specified by a gate signal, it is equivalent to choosing an I_D - V_{DS} curve corresponding to the V_{GS} value. Therefore, selecting a gate signal during the switching transient is equivalent to setting a particular operating point, which is an intersection between the corresponding I_D - V_{DS} curve and the load curve.

III. Optimization of gate signal sequence using genetic algorithm

In GA, the target of optimization is a population, which is a set of individuals with their own genes and fitness. The individuals with better fitness are searched by using genetic operators, namely the selection, crossover, and mutation, through the generations [27]. DAGD is a preferable application for GA because of the binary nature in its operating principle. While the gate signal sequence itself can be directly used as a gene, we convert it to a genotype to set a constraint on V_{GS} waveform, which will help clarifying the relationship between the optimum patterns and the switching characteristics.

A. Genetic expression of V_{GS} waveform

Figure 4 shows the adopted V_{GS} waveform and the corresponding genotype. These types of V_{GS} waveform are called as the three-level waveform in some literature [6, 11]. At the beginning of the turn-off process, the gate is quickly discharged for the duration of t_1 until the transition of I_D begins. Then, V_{GS} is set to an intermediate voltage level V_{int} for the duration of t_2 to slow down the transition of I_D and V_{DS} . Similar strategy is applied to turn-on as well. A 12-bit binary string is used as the gene to express this target V_{GS} waveform, which is divided into three parts of

4-bit strings: b_{t1} , b_{t2} , and b_{int} . The first two parts designate the duration of t_1 and t_2 by multiplying them by 5 ns. The gene is set as a 12-bit binary string divided into three parts of 4-bit strings: b_{t1} , b_{t2} , and b_{int} . The first two parts designate the duration of t_1 and t_2 in the V_{GS} waveform by multiplying them by 5 ns. b_{int} , which designates the voltage level V_{int} , is considered to be the most important part of the three, as it determines the operating point of the MOSFET. We can effectively analyze which voltage level and timing would improve the switching characteristics with this waveform. Hereafter, b_{int} is expressed using a hexadecimal number. The gene is encoded to a time-series gate signal sequence as shown in Fig. 4.

The performance of this AGD waveform strongly depends on the resolution of the input signals. Considering the response speed of the SiC MOSFETs, such as delay time and rise/fall times, are several ten nano-seconds or smaller, nano-second-order control is required. To realize such a fine tuning of V_{GS} waveform, the controller needs to be an FPGA with the clock frequency of several hundred MHz. In addition, a pulse width of less than 15 ns is found challenging considering the response of the switching devices and the signal isolators used inside the gate driver. Therefore, we set a rule that t_1 and t_2 must be more than 10 ns, except for the case of 0 ns.

The following two values are used for the fitness to be optimized. One is the amount of overshoot, which is the peak of V_{DS} at the turn-off and that of I_D at the turn-on. The other is the switching loss, calculated by integrating $I_D \times V_{DS}$ for 200 ns from the start of turn-off/on. This duration is decided considering the convergence of ringings.

B. Optimization process using Python

The optimization algorithm is constructed based on the non-dominated sorting GA II (NSGA-II) [27], which is a well-known and widely-used multi-objective GA, using a Python framework called DEAP [28]. The flowchart of optimization process is shown in Fig. 5. The left-hand part describes the Python program that runs on user PC, which has two interfaces for the SPICE simulation in SIMetrix software and experimental instruments. The gate signal data and commands are sent from left to right, and the waveform data is sent from right to left, through respective means. This structure makes the optimization tool a digital-twin-compatible system. A switching test is supposed in this paper, but similar structure can be configured for other applications, such as converter operation. The detailed procedure is described in the following.

Firstly, an initial population consisting of 60 individuals with randomly-selected genes is created. Their genes are then encoded into the time-series gate signal sequence data, and the switching tests are performed for all genes. In the simulation, it is done by running a SIMetrix script that simulates the predefined netlist file containing the cir-

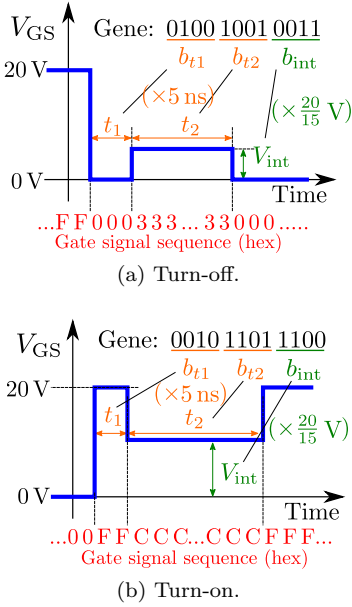


Fig. 4: Genotype and phenotype of gate signal sequences and corresponding V_{GS} waveforms.

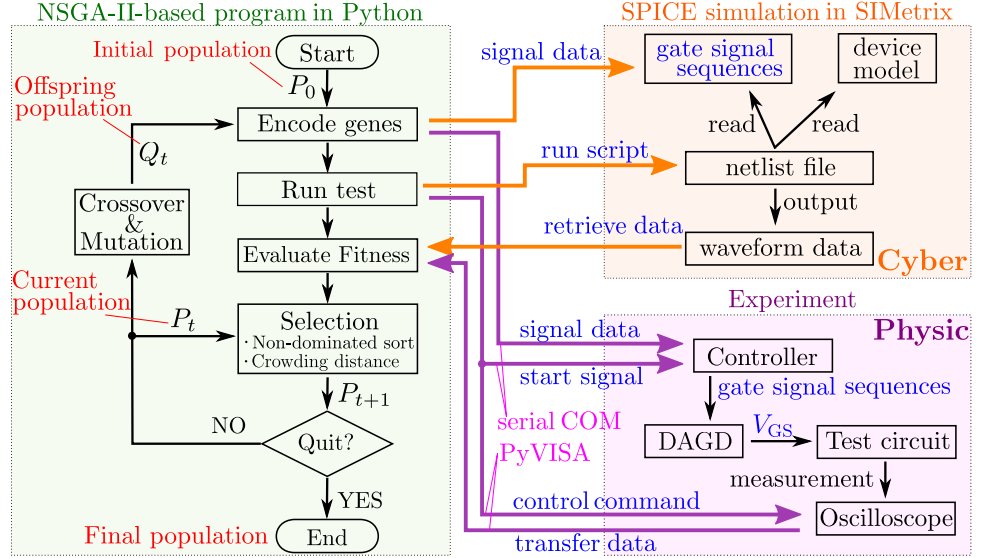


Fig. 5: Flowchart of optimization process interfacing SPICE simulation (orange area) and experiment (purple area). Orange and purple arrows denotes the data or command transfer between the program in PC and simulation soft/experimental apparatus.

Algorithm 1 Selection procedure.

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 $R_t = P_t \cup Q_t$ 
 $\mathcal{F} = \text{fast-non-dominated-sort}(R_t)$ 
 $P_{t+1} = \emptyset$  and  $i = 0$ 
while  $|P_{t+1}| + |\mathcal{F}_i| < N$  do
    assign-crowding-distance( $\mathcal{F}_i$ )
     $P_{t+1} = P_{t+1} \cup \mathcal{F}_i$ 
     $i = i + 1$ 
sort( $\mathcal{F}_i$ ) # according to crowding distance
 $P_{t+1} = P_{t+1} \cup \mathcal{F}_i[0 : (N - |P_{t+1}|)]$ 

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cuit information and device model references. It reads the gate signal sequence, saved as text file, as the input signals of DAGD. The outcome of simulation is saved as the output file, and the necessary data such as device voltage and current waveforms are read by the Python program. In the experiment, it is done by sending the signal sequence data and start command to the controller through serial communication. Then the switching test is performed and the device current and voltage waveforms are measured by an oscilloscope. The waveform data is transferred back to the Python program. No user interaction is needed as the oscilloscope is totally controlled by the program through PyVISA commands.

Based on the waveform data, the fitness of each gene is calculated. The selection is performed consequently using the non-domination rank and crowding distance [27], whose details are described in Appendix A. This procedure is given

by Algorithm 1, where P_t is the population of t -th generation, Q_t is its offspring, $\mathcal{F} = \{\mathcal{F}_0, \mathcal{F}_1, \dots\}$ is a group of fronts classified by their non-domination rank, and N is the size of the population. With this algorithm, the next generation individuals are selected from the closest to the Pareto-front, with descending order in crowding distance. Further details can be found in [27, 28]. The second loop starts here by generating an offspring population of the same size from the current population by two-point crossover and one-bit flip mutation with probabilities of 0.9 and 0.1, respectively. Its individuals are encoded, tested, and evaluated in the same manner. From the second loop, the selection is performed from the set of current (parent) and offspring populations. The search ends after going through this process for 15 loops, which we confirmed to be sufficient for the search to converge, and the final population is obtained.

This is a system that preliminary simulates or tests the gate signal sequences for the power device to obtain the Pareto-front solutions. One can select the solution that meets the requirements for switching characteristics afterwards. The key advantage of such a system is that the whole optimization is handled by a software. The expert know-hows or time-consuming try-and-error do not exist in the design procedure.

IV. System verification in simulation and experiment

The proposed optimization system is applied to the standard double-pulse switching test with an inductive load.

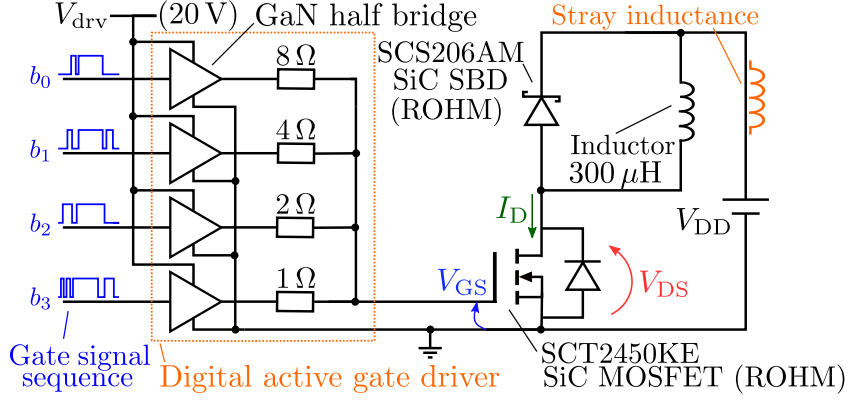


Fig. 6: Schematic diagram of GaN-HEMT-based 4-bit DAGD and double-pulse test circuit.

The optimization is performed in the simulation and in the experiment respectively.

A. Test circuit and simulation setup

Figure 6 shows the schematic diagram of the test circuit. In the simulation, it is represented as a netlist file with stray inductances assumed at each terminal of the power devices and the wire from V_{DD} , which are 5 nH and 60 nH, respectively. We adopt a physically-based simulation model for SiC MOSFET based on its surface potential [29]. It can reproduce the accurate I_D - V_{DS} characteristics even in the high-power region, which helps the analysis of the AGD strategy based on I_D - V_{DS} curves. Device models for the other parts are adopted from the manufacturer's database. The operating condition is set at 240 V and 4 A, which is the same as in the experiment.

B. Simulation results

Figure 7 shows the results of optimization at turn-off, and Figure 7 (a) shows the fitness map of the solutions in the initial and final generation population. The color bar on the right-hand side denotes which value of b_{int} is selected for each solution. The fitness without AGD, which corresponds to a solution with a gene "0000.0000.0000", is also shown for comparison. This figure confirms that the Pareto-front solutions are successfully obtained by the optimization.

We choose some of the solutions in the Pareto-front to analyze their transient behavior. Figure 7 (b) shows the transient switching waveforms of the selected four solutions. Table I shows the representative trade-off relationship between $V_{DS,\text{peak}}$ and transition times of V_{DS} and I_D between their 10% and 90% of the rated value. In sol. iii and iv, $b_{\text{int}} = 0x6$ is selected and $V_{DS,\text{peak}}$ is well-suppressed, while the transition time is longer and so do the switching loss. In sol. iv, the discharge of the gate is slowed from the start by setting t_1 at 0 ns, which further increases the switching loss. In sol. ii, a smaller value of $b_{\text{int}} = 0x5$ is selected, which increases the overshoot but decreases the transition

time and the loss. Figure 7 (c) shows the switching trajectories of sol. i and iv. Here, we checked the possible 15 V_{GS} levels corresponding to the 4-bit gate signal, and drew the I_D - V_{DS} curves at these V_{GS} values. From this figure, it is understood that $b_{\text{int}} = 0x6$ corresponds to a V_{GS} level right above V_{th} , whose operating point is also slightly above the off state. The trajectory approaches this operating point during the duration of t_2 , thereby suppressing the surge voltage, and then converges into the off state.

Figure 8 shows the optimization results at turn-on. From Fig. 8 (a), the Pareto-front is successfully obtained at turn-on as well. We can clearly recognize the sets of solutions with the same value of b_{int} , which gets larger as $I_{D,\text{peak}}$ increases. This trade-off relationship is also confirmed in Table I. The selected b_{int} is 0xA for the solutions around $I_D = 4.75\text{A}$ and 0xB for those around $I_D = 5.2\text{A}$. From Fig. 8, it is understood that these bits designate the V_{GS} levels just above V_{plateau} . In sol. viii, the trajectory first moves toward the operating point on the I_D - V_{DS} curve corresponding to $b_{\text{int}} = 0xB$, suppressing the overshoot of I_D . This result indicates that V_{int} must be above V_{plateau} to suppress the surge current at turn-on, and the overshoot increases as V_{int} becomes higher than V_{plateau} .

Tab. I: Trade-off between overshoot and transition time of V_{DS} and I_D for selected solutions at turn-off and turn-on.

turn-off solutions	sol.i	sol.ii	sol.iii	sol.iv
$V_{DS,\text{peak}}$ (V)	317	301	278	273
V_{DS} fall time (ns)	5.4	5.4	9.0	13.2
I_D rise time (ns)	7.2	7.4	20.8	23.6
turn-on solutions	sol.v	sol.vi	sol.vii	sol.viii
$I_{D,\text{peak}}$ (V)	6.97	6.11	5.60	5.13
V_{DS} rise time (ns)	10.8	14.0	16.6	21.6
I_D fall time (ns)	3.2	4.0	4.6	5.4

C. Experimental setup

We now apply the GA-based optimization system for DAGD to the experiment, utilizing the bottom-right part

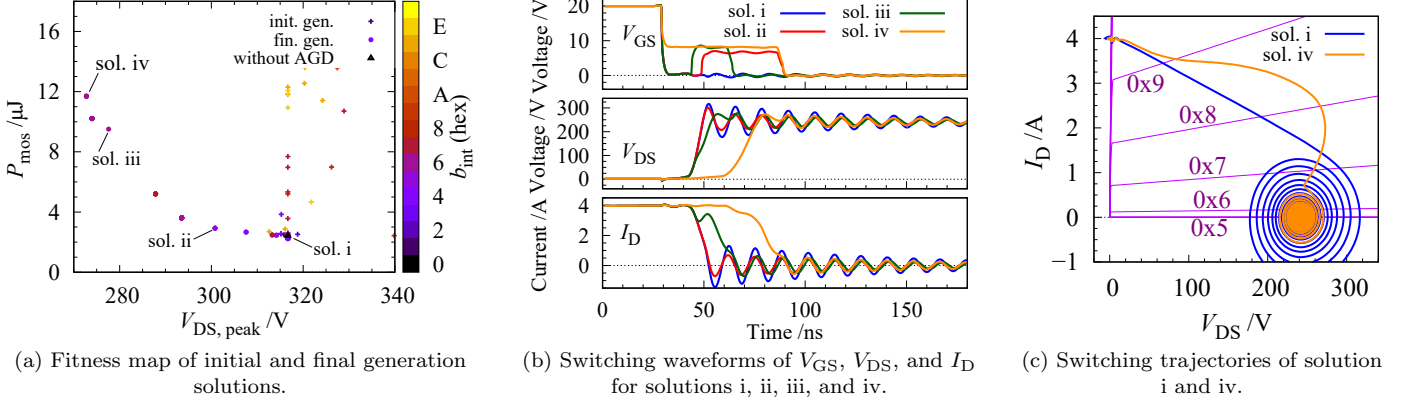


Fig. 7: Optimization results at turn-off in simulation.

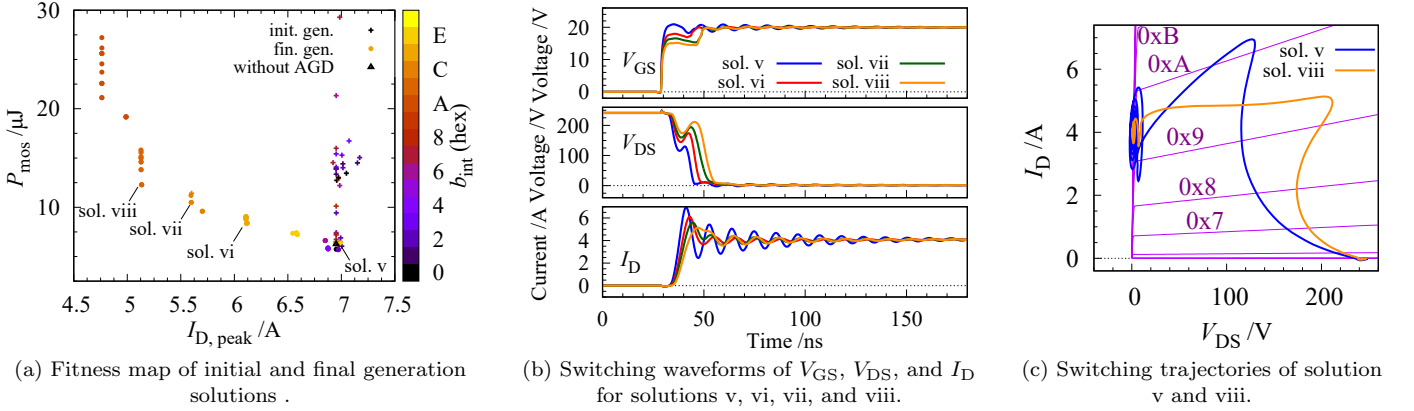


Fig. 8: Optimization results at turn-on in simulation.

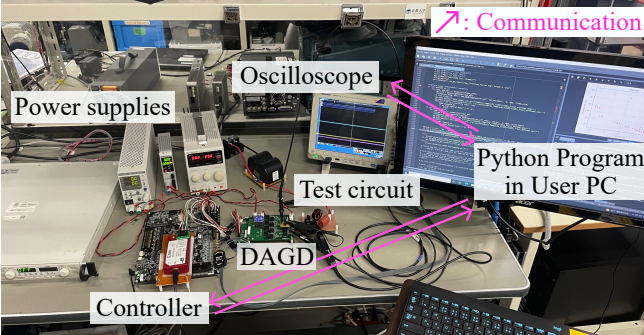


Fig. 9: Photograph of laboratory experiment setup.

in Fig. 5. Figure 9 shows the photograph of experimental setup. The experimental apparatus comprises a PC, a controller (FPGA: Zynq UltraScale+ MPSoCs, Xilinx), GaN-based DAGD, double-pulse test circuit, an oscilloscope (MDO4014-3, Tektronix) with probes, and power supplies. The 4-bit gate signal is generated inside FPGA by replacing the falling/rising edge of PWM signal with the turn-off/turn-on signal sequence given for each bit, as illustrated in Fig. 10. The Python program in the user PC communicates with the controller and the oscilloscope as described in Fig. 5. The waveforms of V_{GS} , V_{DS} , and I_D are measured by the oscilloscope and transferred to the PC

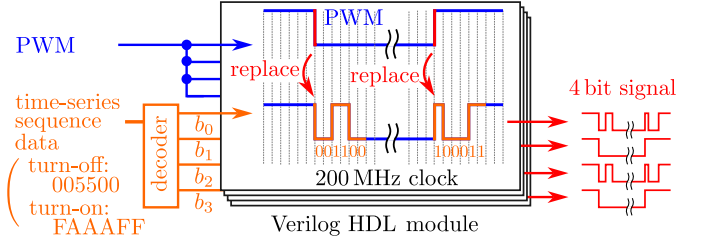


Fig. 10: 4-bit gate signal generation inside FPGA.

for the calculation of the fitness.

D. Experimental results

Figure 11 shows the optimization results at turn-off. It can be observed that the algorithm generally works as expected in the experiment. Due to the inevitable measurement errors and the resulting loss calculation errors, the Pareto-front solutions are spread compared to simulation results. For this reason, the fitness of the solution without AGD may be located above the Pareto-front. The selected values of b_{int} are typically 0x6 for the solutions with smaller surge voltage, yielding a very similar result to the simulation. Also, the transient switching waveforms and trajectories in Fig. 11 (b) and (c) are similar to the simulation results. It

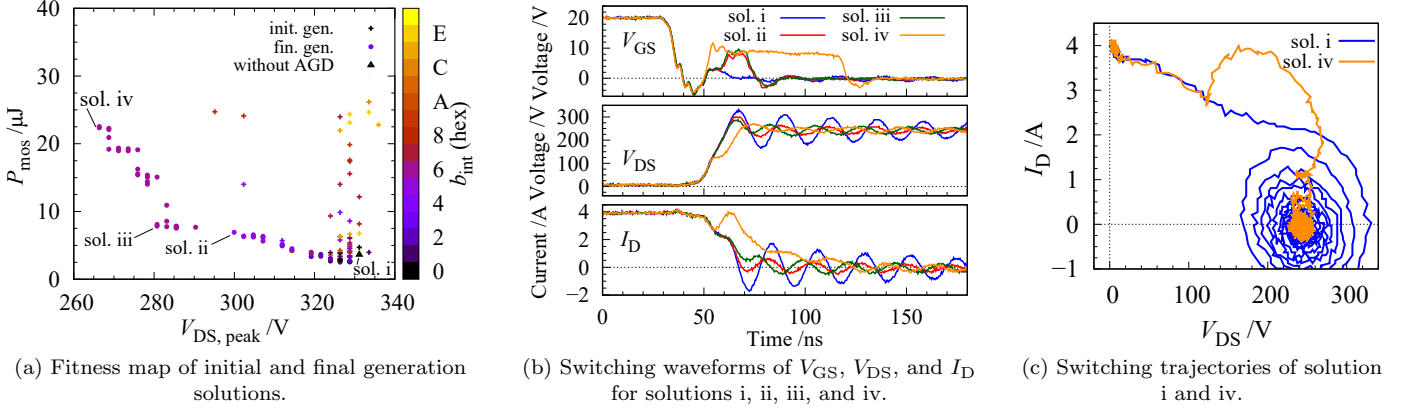


Fig. 11: Optimization results at turn-off in experiment.

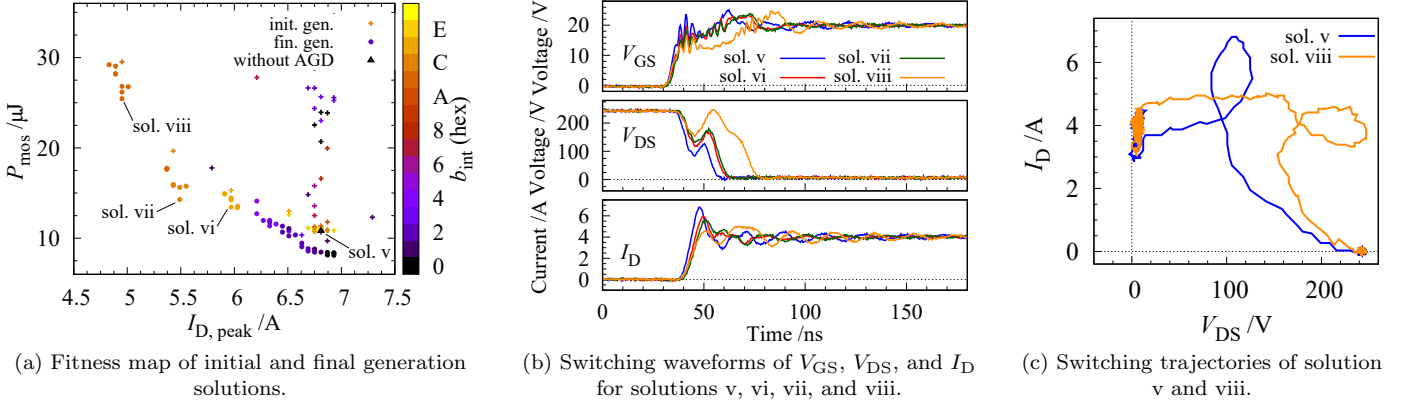


Fig. 12: Optimization results at turn-on in experiment.

is understood that the surge voltage is suppressed by the same physics as observed in the simulation. Table II compares the calculated switching transition times among the selected solutions, which also indicates the same trade-off relationship is established as in simulation.

Figure 12 shows the optimization results at turn-on. The sets of solutions with the same value of b_{int} are obtained, and $b_{\text{int}} = 0\text{xB}$ is selected for solutions with the least $I_{\text{D, peak}}$. From Fig. 12 (b), a fluctuation of V_{GS} is encountered, making it hard to read what voltage level is actually designated. Nonetheless, from Fig. 12 (c), it is understood that sol. viii designated the operating point right above V_{plateau} , as observed in simulation.

Lastly, Fig. 13 compares the selected b_{int} and the amount of resulting overshoot in Pareto-front solutions between simulation and experiment. The trend shows good match both at turn-off and turn-on, indicating that the relationship between b_{int} and the resulting overshoot could be predicted in simulation. These results confirm that the proposed optimization system works similarly both in the simulation and experiments, verifying its digital-twin compatibility. The selected bits are quite similar but slightly different to the simulation results in both cases. In particular, the variables t_1 and t_2 do not match in simulation and

Tab. II: Trade-off between overshoot and transition time for selected solutions at turn-off and turn-on in experiment.

turn-off solutions	sol.i	sol.ii	sol.iii	sol.iv
$V_{\text{DS, peak}}$ (V)	331	300	281	269
V_{DS} fall time (ns)	11.6	11.2	17.6	18.0
I_{D} rise time (ns)	16.0	34.8	49.2	54.0
turn-on solutions	sol.v	sol.vi	sol.vii	sol.viii
$I_{\text{D, peak}}$ (V)	6.85	5.97	5.43	4.95
V_{DS} rise time (ns)	11.0	20.2	22.8	44.8
I_{D} fall time (ns)	3.4	5.2	5.2	6.8

experiment. This is partly because the gate dynamic characteristics is hard to reproduce accurately in device model, and also partly because it is susceptible to change due to many influences, such as parameter variation among devices and temperature, as well as external circuitry configuration. For these reasons, it is not yet possible to use the predicted signal sequences directly in the experiment. The help of local-search-based algorithm can be integrated to realize a link between them as a future work.

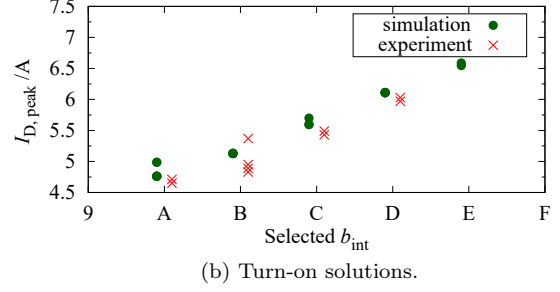
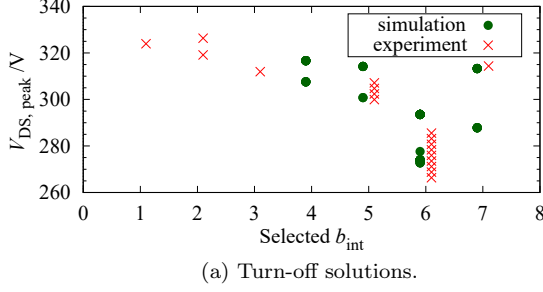


Fig. 13: Comparison of selected b_{int} and resulting overshoot of Pareto-front solutions between simulation and experiment.

V. Optimization in other operating conditions and for different SiC MOSFETs

So far in this paper, the digital-twin-compatible optimization is verified for a single operating condition and a single device. This section provides some additional experimental results in different operating conditions and using different SiC MOSFETs to ensure the versatility of the proposed optimization method without changing the hardware itself, which is one of the main advantages of the proposed gate-drive system.

A. Results in different operating conditions

The optimization is performed for different operating conditions (O.C.). Firstly, different I_D of 2 A, 4 A and 6 A are applied whereas V_{DS} is kept at 240 V. This assumes an application that deal with variable load operation. Figure 14 (a) and (b) show the Pareto-front solutions at turn-off and turn-on, respectively. It is confirmed that the optimization works in all of these conditions. From Fig. 14 (b), it is found that the selected b_{int} becomes larger as the operating current increases. This trend corresponds to the observation in Section IV that the effective value of b_{int} at turn-on is strongly tied with V_{plateau} , which becomes larger as I_D increases.

Secondly, three V_{DS} values of 120 V, 240 V, and 400 V are applied with the same operating current of 4 A. The former two voltage levels are within the range of home appliances while the latter is within the range of electric vehicle charger [30]. Figure 15 (a) and (b) show the optimization results. The Pareto-front solutions are obtained in all the conditions. In Fig. 15 (b), almost the same b_{int} is selected for all V_{DS} conditions, which is a clearly different trend compared to Fig. 14 (b). This can be attributed to the device physics that the V_{plateau} does not change with the applied V_{DS} value.

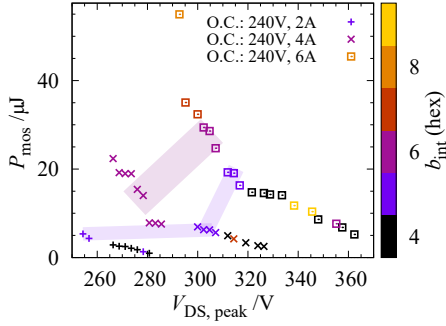
B. Results for different device

Lastly, the optimization is performed for two additional SiC MOSFETs of similar ratings from different manufacturers

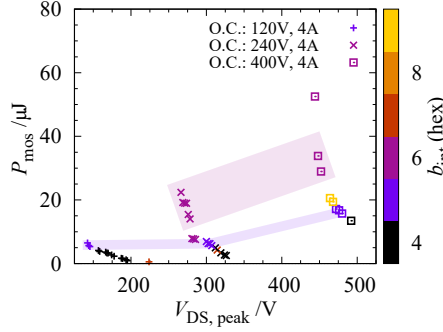
(SCT10N120, STMicroelectronics NV and C2M0280120D, Wolfspeed Inc.) at the operating condition of 240 V and 4 A. Figure 16 shows the obtained Pareto-front solutions for these devices with comparison to those for SCT2450KE. We can recognise some differences in the selection of b_{int} among devices, which is presumed to have arisen from the difference in device characteristics. These results confirm that the proposed optimization approach is applicable regardless of the target device, and also that DAGD can immediately realize it.

VI. Conclusion

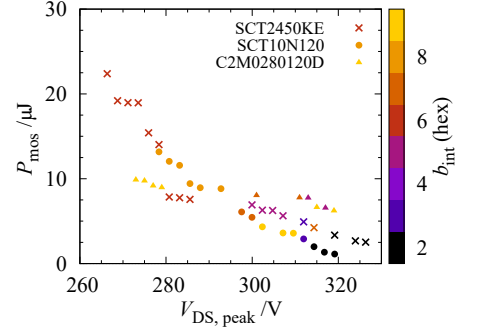
This paper investigated the digital-twin-compatible GA-based optimization system for a digital gate driver to control the switching characteristics of SiC MOSFETs. The main contribution of this paper is summarized as follows. Firstly, the V_{GS} waveform is transformed into the target of combinatorial optimization problem by adopting DAGD and a V_{GS} waveform shape with three variables. Secondly, a digital-twin-compatible optimization system is configured, which interfaces both the simulation software and the experimental instruments. The GA is adopted as the optimization method out of metaheuristics approaches because of its compatibility with the adjustment of gate signal sequence. Python-based program enables the flexibility to construct such a system and for further expansion. Finally, the system is verified both in the simulation and in the experiment. The optimized solutions are analyzed in relation to the I_D - V_{DS} curves of the device, which clearly described the effectiveness of the designated V_{GS} level on the switching characteristics. As DAGD directly controls the gate bias state of SiC MOSFET, the physical model and experimental results showed a good match. Such an orientation toward developing a digital-twin platform utilizing the physically-associated simulation opens up the possibility for a conceptually new approach for adjusting the AGD operation, which is never feasible with analog technique. The optimization is also performed for several different operating conditions and for different devices, verifying the flexibility to be applied to other applications without changing the



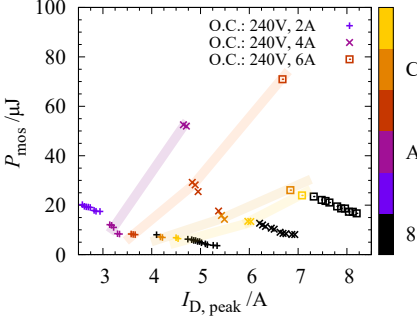
(a) Pareto-front solutions at turn-off.



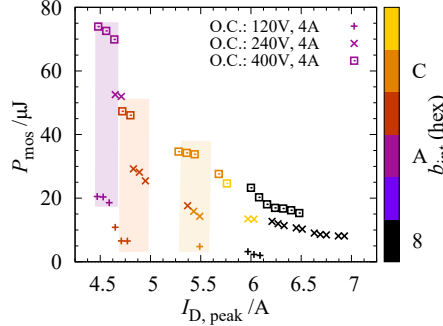
(a) Pareto-front solutions at turn-off.



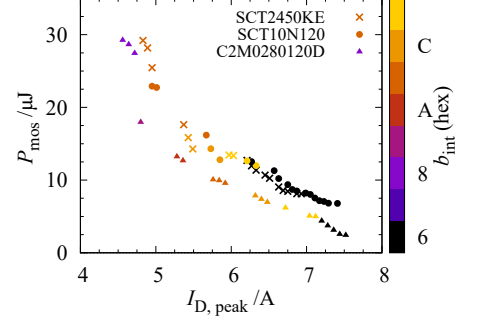
(a) Pareto-front solutions at turn-off.



(b) Pareto-front solutions at turn-on.



(b) Pareto-front solutions at turn-on.



(b) Pareto-front solutions at turn-on.

Fig. 14: Optimization results under variable-current conditions.

Fig. 15: Optimization results under variable-voltage conditions.

Fig. 16: Optimization results for different SiC MOSFETs.

hardware itself. These results pioneered the concept that the design of gate drive circuit, which usually requires a considerable amount of human effort, can now be a target of digital-twin optimization using a software.

On the other hand, there remains a small but inevitable difference between the optimum solutions in simulation and experiment. The accuracy of the device model, especially the gate C–V characteristics, is critically important for minimizing the difference. Also, the closed-loop or feed-forward structure will need to be added for the usefulness and potential practicality of this study. A local-search algorithm may be combined to the system to compensate the unpredictable difference, such as variations in device parameters, providing a link between the physical-system and the simulation. In addition, the proposed scheme can only be applied to a switching circuit with one SiC MOSFET, such as DC-DC converter application, in its current form. The expansion of the algorithm needs to be worked on to apply the concept into higher-order topologies, such as full-bridge configuration and multi-level converters, considering additional fitnesses such as overall efficiency of the converter and timing constraints. Pursuing these topics will eventually realize a true digital-twin-based optimization of power switching.

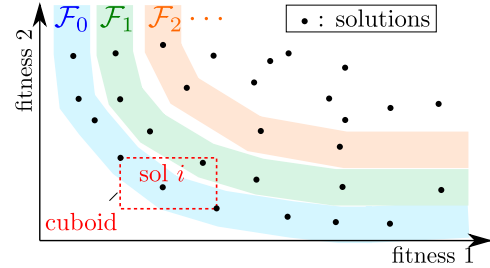


Fig. VI.1: Illustrations of solutions sorted by non-domination rank and example of cuboid for sol. i in $\mathcal{F}_0$.

Appendix

A. Additional description of selection algorithm

A solution being non-dominated refers to a state where there is no solution whose at least one of the fitness values are better than those of the solution. The solutions in $\mathcal{F}_0$ (rank 0) are non-dominated by any other solutions, while those in $\mathcal{F}_k$ (rank k) are non-dominated if ignoring the solutions belonging to all the fronts with lower ranks, as shown in Fig. VI.1. Crowding distance of a solution is calculated by taking the sum of side length of a cuboid composed between the two neighboring solutions of the same front, as also shown in Fig. VI.1 [27].

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